FAMU-FSU College of Engineering
Department of Electrical and Computer Engineering

SYSTEM-LEVEL DESIGN REVIEW

EEL4911C – ECE Senior Design Project II

Project Title: **Synthetic Active Array Radar Aperture (SAR)**

Team #: E11

Student Team Members:

- **Matthew Cammuse**, Electrical Engineering (Email: mgc11@my.fsu.edu)
- **Joshua Cushion**, Electrical Engineering (Email: jlc10e@my.fsu.edu)
- **Patrick Delallana**, Electrical/Computer Engineering (Email: pnd10@my.fsu.edu)
- **Julia Kim**, Electrical Engineering (Email: jk09k@my.fsu.edu)
- **Malcolm Harmon**, Mechanical Engineering (Email: mjh11f@my.fsu.edu)
- **Benjamin Mock**, Industrial Engineering (Email: bam11g@my.fsu.edu)
- **Mark Poindexter**, Mechanical Engineering (Email: mpp12b@my.fsu.edu)
- **Jasmine Vanderhorst**, Industrial Engineering (Email:Vanderhorst_91@yahoo.com)

Senior Design Project Instructor: Dr. Michael Frank
Electrical/Computer Engineering Department Advisors: Dr. Simon Foo and Dr. Shonda Bernadin
Industrial Engineering Department Advisor: Dr. Okoli
Mechanical Engineering Department Advisor: Dr. Collins

Submitted in partial fulfillment of the requirements for
EEL4911C – ECE Senior Design Project II

February 9, 2015

Executive Summary

The purpose of the electronic Synthetic Active Aperture Radar (SAR) Imager project, sponsored by Northrop Grumman, is to design and develop a low-cost detection system capable of providing a low, but useful, imagery resolution as a learning experience. In theory, the application of the electronic SAR Imager focuses on security applications and its ability to detect potentially threatening objects such as handguns. This project is sponsored through the FAMU-Foundation with a $50,000.00 budget with an expected time line of eight months to completion.
A radar is an object detection system that uses radio waves to measure characteristics of certain objects and is typically composed of antennas in which transmit pulses of radio waves bounce off the target in the designated range. The wave is reflected off the target and returns a wave to the receiving end of the system which is usually a dish, horn, or some form of waveguide usually located at the same site as the transmission of the wave. In a typical radar, the antenna which usually acts as a transmitter and/or receiver is in a static position. The electronic SAR Imager is a more complicated scenario of radar imaging which allows for the detection of a much greater range by movement of the transmission antenna. This can be seen such applications as aircraft topography; the antenna on the plane would transmit signal to a landscape while the antenna is moving. To create a fixed electronic SAR imager, the design will be constructed with multiple stationary antennas that emit or receive pulses to emulate the theory of an SAR.

This project will consist of twenty horn antennas: sixteen receive and four transmit. The antenna structure will consist of two linear antenna apertures. Each aperture will contain eight receive antennas placed between two transmit antennas. Two antenna apertures will be utilized and laid across each other creating a T-shaped design with each horn directed towards the target. Besides the center horn antennas, each horn will be angled directionally towards the target. Overall, the design will create four rows of five antennas being placed orthogonal to each other, creating sixteen phase centers per linear antenna aperture and thirty-two phase centers for the whole design. A phase center is the half-way distance between one transmit and one receive antenna in an aperture and represents a receive antenna's center absorbance point or maximum absorbance point. One transmit is responsible for eight phase centers. When placing receive antennas next to each other, additional maximum absorbance points are created. One aperture may only have eight receive antennas but eight additional phase or maximum absorbance points are created. More phase centers results in a better chance to receiving a return signal. For this project, radar system is required to reach a target twenty feet away and cover a human's body.

The system will be controlled via an FPGA which will sequentially transmit pulse from an antenna and then turn on the receiving antennas/turn off the transmitting antenna pulse to receiving a signal bouncing off the target. This will be done from every orthogonal direction one after the other to give the most data possible. The data would get sampled on a scope and get recorded. If time permits, the FPGA can do more complicated tasks such as storing some of the data that can be output and operated on. This sampled data could then be captured and sent to a PC for image processing. This would most likely be done using software such as Simulink. Overall the goal of this project is to apply engineering design practices and technical knowledge to create a physical schematic of an SAR Imager which would transmit and receive pulse from at least one row of antennas out of the four orthogonal rows.

Table of Contents

Table of Figures and Tables

1 Introduction

1.1 Acknowledgements

The electronic Synthetic Active Aperture Radar (SAR) Imager team would like to extend thanks to the stakeholders of this project from Northrop Grumman and the FAMU-FSU College of Engineering sponsors. First and foremost to the corporate sponsors at Northrop Grumman, we are most grateful for the generous $50,000 financial contribution to the FAMU Foundation to support research, equipment procurement, and work efforts on the project. In addition to financial contributions, the team also thanks Northrop Grumman for resource support from Peter Stenger, who continually provided technical support, guidance, and direction throughout the duration of the project. We would like to thank Dr. Michael Frank, Dr. Simon Foo, Dr. Shonda Bernadin, Dr. Bruce Harvey, and Dr. Rajendra Arora from the Electrical & Computer Engineering Department for their continued efforts to advise the team in making practical engineering design decisions. Also, we would like to thank Dr. Nikhil Gupta, Dr. Scott Helzer, Dr. Emmanuel Collins, Ricardo Aleman, and Samuel Botero from the Mechanical Engineering department for their contributions in developing professionalism, providing continuous feedback for improvement, and supporting the mechanical design of the SAR Imager system. Finally, we thank Dr. Okenwa Okoli, Dr. James Dobbs, Emily Hammel, and Margaret Scheiner from the Industrial Engineering department for their help in project management, scheduling, and quality engineering.

1.2 Problem Statement

1.2.1 General Problem Statement

The number one priority of this project is to create a physical schematic of a radar system with synthetic-aperture radar theory using COTS (commercial off the shelf) components. The theory behind an SAR Imager requires a mobile transmission and receiving antenna to capture a greater range and/or clearer image of what is being targeted. Since a mobile antenna would require a device which moves the antenna and the team does not have the capability or timeframe to make such a device, we will supplement the framework of a single moveable antenna with a system having multiple antennas to emit and receive signal from different locations. The theory behind emitting and receiving signals on a single target from multiple locations will still be implanted, but instead of using one moving antenna the team will use multiple stationary antennas that emit and receive signals from different locations.

1.2.2 General Problem Solution

The solution will be tackled in several steps. There are three disciplines to this project: Electrical/Computer Engineering, Mechanical Engineering, and Industrial Engineering.

The Electrical/Computer Engineers will design a stationary schematic of a radar system which has twenty antennas overall with sixteen being receive antennas and four being transmit antennas. These antennas will be separated into four rows of five antennas each. Each of these four rows will be placed orthogonal to each other, and there will be an epicenter between these four rows which is where the target will be. The rows of five will be separated by twenty feet in

each direction from the target, and the system that controls the emitting and receiving of signal from the antennas will be controlled via an FPGA. It is the job of the Electrical/Computer engineers to design a workable schematic of the system that receive and emit signals from at least one row of antennas. This also includes the programming of the FPGA board, signal processing, and possibly even image processing of data if the project goes further than expected. The Electrical/Computer Engineers will be the ones to determine almost all of the theory and components of the system, thus making them the base of the project.

The Mechanical Engineers will design the physical structure of the antennas and the associated horns that go with them. The Mechanical engineers will work very closely with the Electrical engineer who specializes in antennas to design the proper horn shape and the spacing between each of the antennas. The Mechanical Engineers also have a role in helping the Electrical Engineers set up all of the components and equipment of the system and making sure that they are working properly as well. It is vitally important for the Mechanical and Electrical Engineers to work in close contact since the Mechanical portion of this project deals with the physical design of the antennas which transmit and emit signal.

The Industrial Engineers have a primary role in managing the human factors, risk analysis, the project schedule, and the overall budget of the system. The Industrial Engineers will also be in charge of helping the Electrical Engineers acquire and order the specific components needed for the system. Industrial Engineers will also be in close contact with the school and the sponsor since they will be the ones who actually go and submit the orders for purchase. Industrial Engineers will also be of utmost importance when making administrative decisions within the team due to their knowledge of cost engineering and optimization.

1.3 Operating Environment

The operating environment will be those locations of primary concern for homeland security applications such as airports, public schools, museums, etc. These locations will demand that the SAR Imager properly functions at average room temperature (293.15 – 298.15 K) and within average humidity (30 – 50%) [1]. The SAR Imager should be able to operate in the presence of other electronics and RADARs and not be influenced by them in their main operation: determining the hidden threat of hidden weaponry. This system should be able to operate at a nonstop pace when needed and also be equipped with adjustments to be set-up in the specified location on interest.

1.4 Intended Use(s) and Intended User(s)

1.4.1 Intended Use

The intended use for the SAR Imager will be for theoretical implementation and testing. Tests to check for the transmission and receiving of pulse by the antennas of this project will be the primary use for the system. A mannequin will act as the target to abide by FSU campus medical standards. If time allows, more complicated aspects such as image processing can be used to generate an image.

1.4.2 Intended Users

The intended users for the SAR Imager will primarily be the student members of the team. Any advisors or the sponsor may want to test out the system for themselves to check progress and that is a viable option as well. As a research project, this project only intends for an operating physical schematic of the project, not a fully functional prototype. The end result should have a physical system that transmits and receives signal that is controlled/timed via an FPGA.

1.5 Assumptions and Limitations

1.5.1 Assumptions

This project is based upon the following assumptions:

- The radar should operate at frequencies safe for human interaction.
- The radar must be capable of detecting metal and/or threatening objects on a person's body from a distance.
- The radar must be operating at near real-time.
- The data from the receiver should generate polynomial images on a display screen. Then based on color identification, it should be easy to pin point an object's location. A selected color would represent a received signal, and if that color appears on the screen, an object has been located.
- The field programmable gate array (FPGA) board must have a clock of 100 MHz.
- The FPGA board should have Peripheral Module (Pmod) connectors to add analog-to-digital (A/D) and digital-to-analog (D/A) converters.

1.5.2 Limitations

The decisions in this project are confined by the following limitations:

- The distance to the scene to be imaged must be 20 feet. (REQF-002)
- The area to be imaged, also known as scene extent, must cover the width of a person and should ideally cover the person's torso and legs. However, the scene extent will be based on the type of horn antennas selected. (REQF-003)
- The frequency range should be within the X- or Ku- band operating frequency, which is a range of 8 to 12 GHz for X-band and 12 to 18 GHz for Ku-band. (REQF-001)
- The cross range and down range resolution are determined based on the employed beamwidth and distance between the antennas and target. (REQF-004)
- The down range resolution must be low so it does not take a thorough image of the body, but has enough depth. (REQF-005)
- The pulse width should be at about 20 nanoseconds so the pulse can travel to and from the scene. (REQF-006)
- The number of phase centers for the system is sixteen. (REQF-010)

- The number of antennas to be used for the system is sixteen receive antennas and four transmit antennas. (CONS-001)
- Antennas must be placed close together at equal distances apart and be precisely pointed at target. (CONS-002)
- To use the system for testing, the room must be bigger than 20 feet x 15 feet.

1.6 Expected End Product and Other Deliverables

1.6.1 Synthetic Active Aperture Radar Imager

The SAR Imager system will be designed and physically implemented by April 2015. The sponsor in particular does not have a deadline, but the College of Engineering's deadline for completion of projects is April 2015. The end product of this project will be a testable conceptual design of an electronic SAR Imager. The electronic SAR Imager will have the ability to receive and transmit pulses on at least one row of antennas out of the four orthogonal rows on the whole schematic. A summary of the radar system's components are listed below:

- 1 Power Amplifier
- 2 Low Noise Amplifiers
- 3 Variable Attenuators
- 18 Fixed Attenuators
- 2 Band Pass Filters
- 1 Field Programmable Gate Array (FPGA) Board
- 2 Analog to Digital Converters (ADC)
- 2 Pmod Test Point Headers
- 4 Receive Antennas
- 16 Transmit Antennas
- 1 Voltage Control Oscillator Demo Board
- 1 Single Pull Four Throw Non-Reflective Switch (SP4T)
- 1 Single Pull Double Throw Non-Reflective Switch (SPDT)
- 1 Single Pull Sixteen Throw Non-Reflective Switch (SP16T)
- 1 Wideband Amplifier
- 22 Coaxial Waveguide Adapters
- DC Power Supply
- 15 50Ohm Loads (Male)
- 5 5Ohm Loads (Female)
- 15 Varied SMA Connectors
- 20 Varied SMA-BNC Adapters
- 46 Varied RF Cables
- 1 Super Ultra Wideband Amplifier
- 2 Ultra Wide Bandwidth Amplifiers
- 2 Frequency Multipliers

1.6.2 Documentation and Configuration Flash Drive

1.6.2.1 Electronic Circuit Schematics

The electronic circuit model developed will be saved in different formats to the Documentation and Configuration flash drive. This will be completed by April 2015.

1.6.2.2 Antenna Structural Schematics

The structural design of the antennas and the supporting system will be be saved to the Documentation and Configuration flash drive. This will be completed by April 2015.

1.6.2.3 Code and Configuration Files

The VHDL code and configuration files developed for the electronic SAR imager will be organized in a .zip file and saved into the Documentation and Configuration flash drive. This will be completed by April 2015.

2 System Design

2.1 Overview of the System

The goal of the project is to create a functioning, two-dimensional, static Synthetic Aperture Radar (SAR) and have it detect metal in a scene extent of 30x30 inches. A typical SAR is active, utilizing the movement of one antenna to simulate multiple receive antennas after transmitting a signal, generating multiple phase centers. A phase center is the midpoint between transmit and receive antennas. Based on the time the signal takes to return and the phase center the reflected signal collides with will determine the phase of the signal. From the signal's phase, the location and formation of the object can be established with advanced signal processing. The radar system for this project is static, meaning immovable and relies on the moment of the object. To create a static SAR, multiple horns antennas will be aligned together, similar to the layout of a phased array system. Then, one of the end horn antennas will transmit a signal and have the neighboring horn antennas switch on and off to create the multiple phase centers, similar to an active SAR. If multiple radar components are configured correctly and the signal processing is efficient, the static SAR design for this project will be able to determine where an object with a high radar cross section is located on a screen, based on two-dimensional imaging.

2.1.1 Electrical System Overview

The diagram in Figure 1 shows the electrical system of the multiple antenna radar system. The electrical system is responsible for generating the radio frequency signal that transmits into the scene extent; this is accomplished using a voltage controlled oscillator along with a power amplifier to amplify the power and the 4 transmit antennas to emit the signal. The electrical subsystem is also responsible for receiving the reflected waveform scatterings of the return signal from the target and converting them to digital voltages in order to do the signal processing. This is accomplished through the use the 16 receive antennas, the IQ demodulator, the analog to digital converters, the FPGA and the other components in the receive chain. Another responsibility of this

subsystem is to perform the signal processing to generate the imagery. This will be conducted by the computer using signal processing software. Lastly the electrical subsystem will display the imagery on the VGA display.

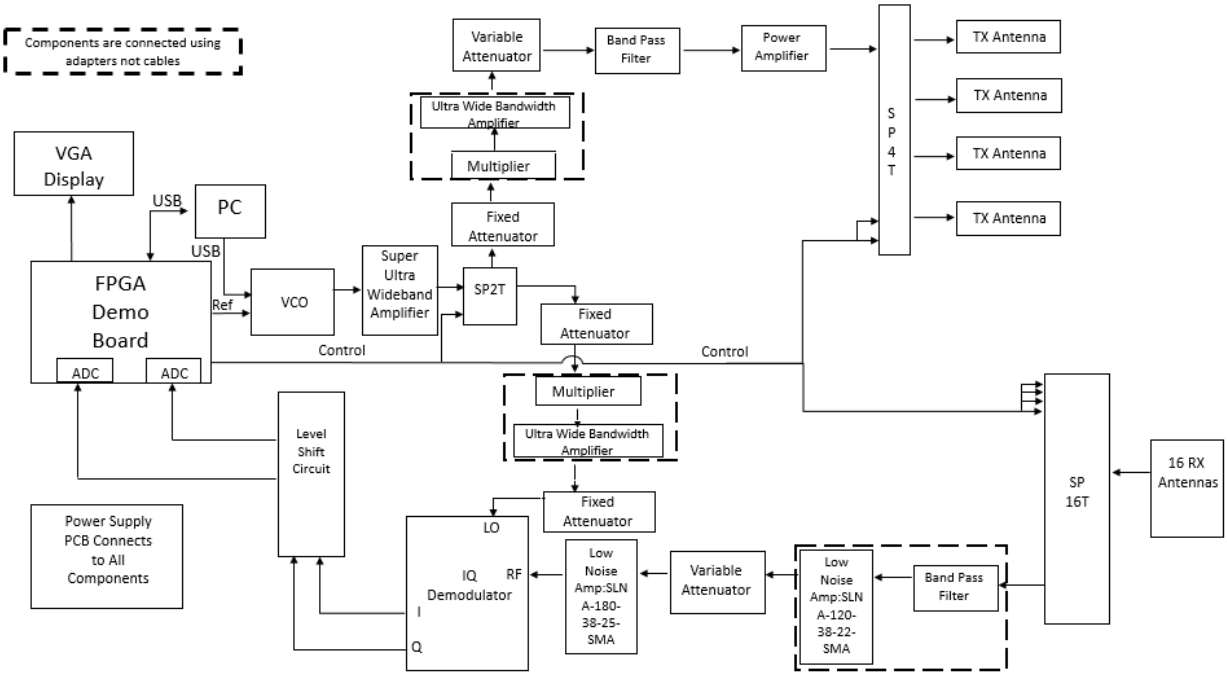


Figure 1: Electrical System

2.1.2 Antenna Design Overview

The antenna design will consist of two linear antenna arrays. Each array will have two transmit antennas located at the ends of each array with eight receive antennas between the transmit antennas. The two arrays will then cross each to form a T-shaped design illustrated in Figure 2. X-band, 17 dB gain, rectangular horn antennas will be utilized for the design. Spacing between transmit and receive antennas will be three lambda (3λ), and spacing between receive transmit antennas is six lambda (6λ). The spacing distances will prevent grating lobes from entering into the scene extent as the main lobe scans the scene. When the antenna is transmitting, the design will allow the beam to cover an area of nine feet by nine feet, which is more than the 30 by 30 inch scene extent. Each antenna will connect to a waveguide adapter, changing a signal between coaxial to waveguide. Coaxial cables will connect to each waveguide adapter and communicate to the rest of the radar system.

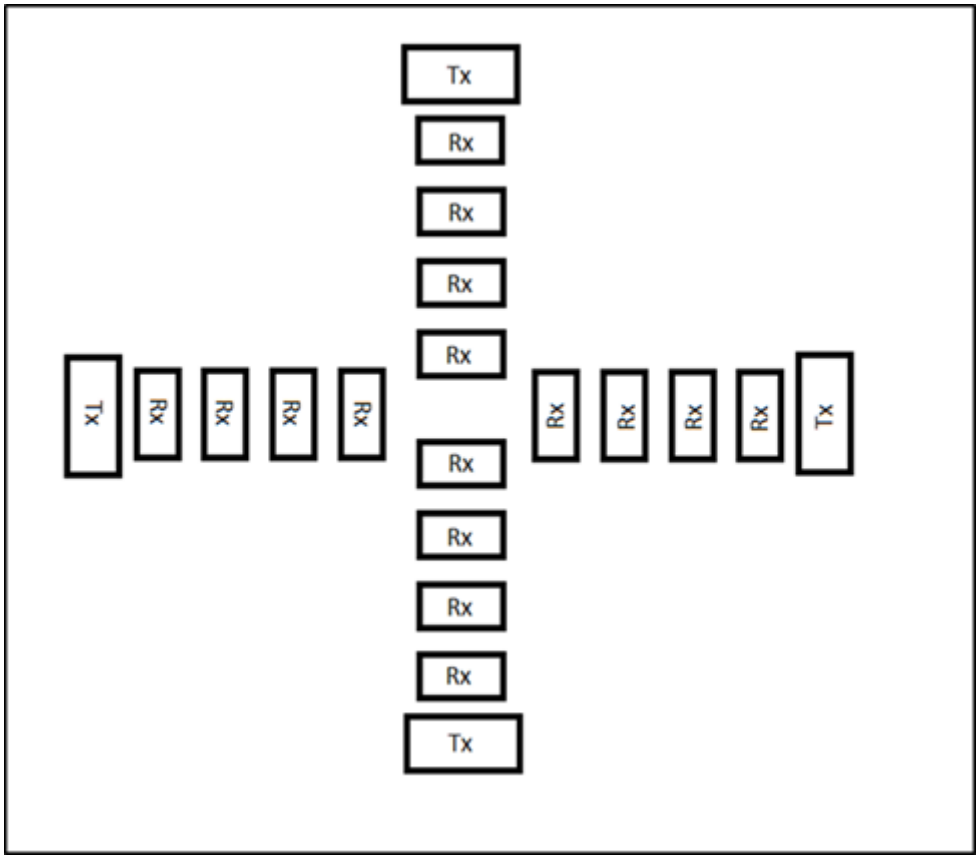


Figure 2: T-Shaped Linear Array Antenna Design

2.1.3 Antenna Structure Overview

The horn antenna structure will be made of an aluminum based metal for light weight and machinability. The structure will be made in separate sections to piece together because of its width and height being 5.5 ft. x 5.5 ft. The goal is to have four separate quadrants which will be connected together with a divider to allow enough space in between quadrants for the horn antennas to be placed. Below in Figure 3 shows how the horn antennas are held together by two quadrant panels and how the connector/divider hold the two quadrant panels.

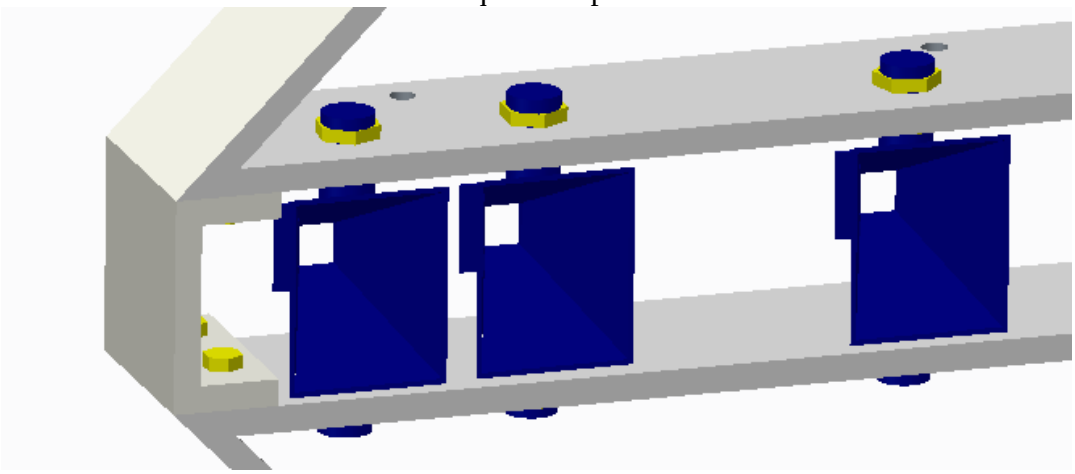


Figure 3: 3-D Model Showing Horn Placement on Structure

The horns will be flush with the front of the structure so no interference could come from the aluminum metal and disrupt the signal. Four horn covers will be bolted onto the back of the structure to cover the horns and the wires running to the horns. The covers will also add extra support for the structure. Below in Figure 4 shows the full design of the horn structure without the stand and component box.

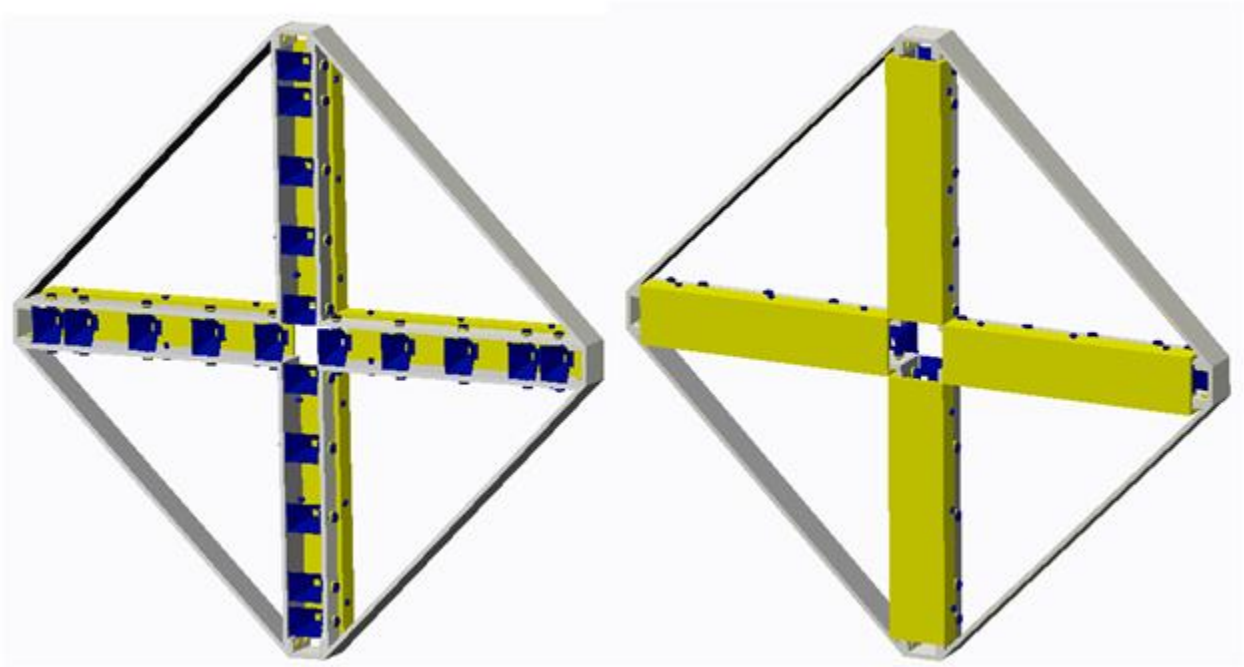


Figure 4:3-D Model of the Horn Antenna Structure without Stand and Component Box

2.1.4 Signal Processing Overview

Figure 5 shows the sixteen phase centers from each transmit and receive antenna pair to the scene. The variable d is the distance between phase centers, θ is the angle from a line with origin at center of array that is 90º to antenna ray to a line from the origin at the center of the array to a point elsewhere in the scene, and θ_n represents the sixteen θs that go to sixteen points in the scene. For each θ, a function with 16 points is generated. The following Table 2 is generated with each of the functions.

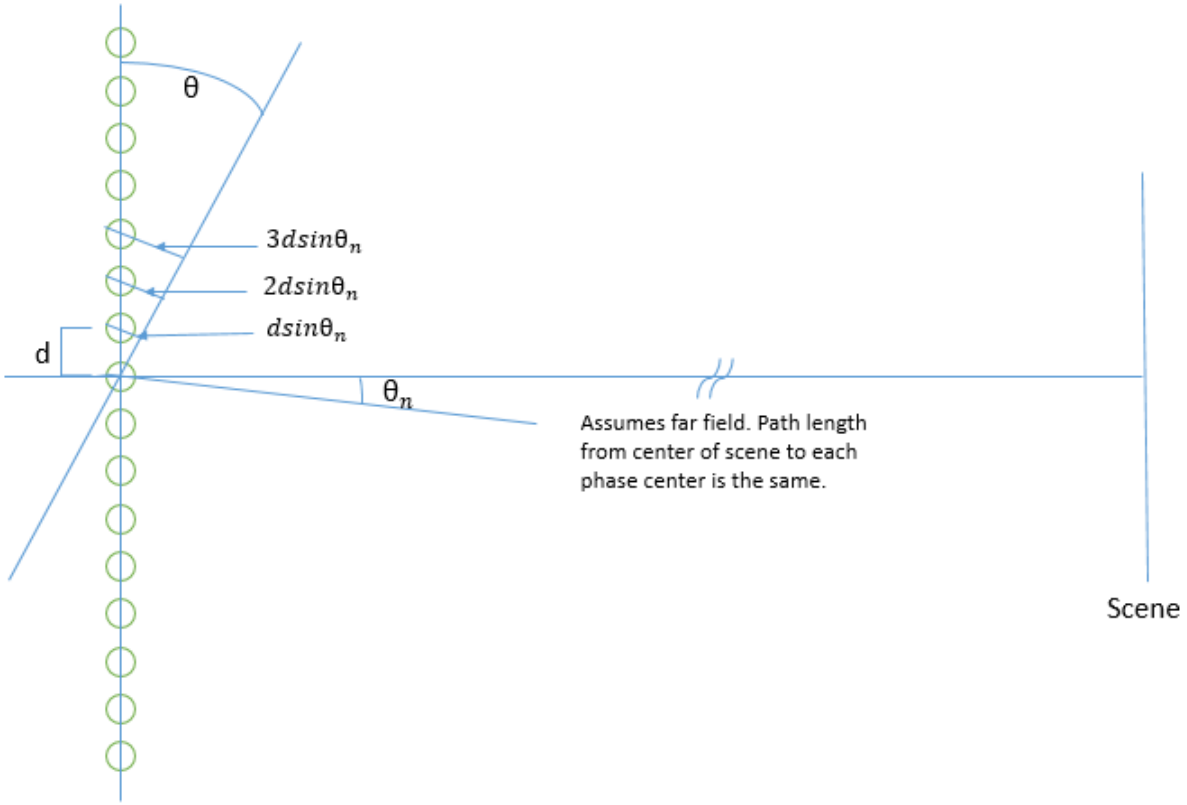


Figure 5: Sixteen Phase Centers from each Tx/Rx Pair to Scene

Table 1: Sixteen Function

	1	2	3	…	15	16
$f(\theta_1)$	$1*d*\sin\theta_1$	$2*d*\sin\theta_1$	$3*d*\sin\theta_1$	…	$15*d*\sin\theta_1$	$16*d*\sin\theta_1$
$f(\theta_2)$	$1*d*\sin\theta_2$	$2*d*\sin\theta_2$	$3*d*\sin\theta_2$	…	$15*d*\sin\theta_2$	$16*d*\sin\theta_2$
$f(\theta_3)$	$1*d*\sin\theta_3$	$2*d*\sin\theta_3$	$3*d*\sin\theta_3$	…	$15*d*\sin\theta_3$	$16*d*\sin\theta_3$
…	$1*d*\sin\theta_n$	$2*d*\sin\theta_n$	$3*d*\sin\theta_n$	…	$15*d*\sin\theta_n$	$16*d*\sin\theta_n$
$f(\theta_{15})$	$1*d*\sin\theta_{15}$	$2*d*\sin\theta_{15}$	$3*d*\sin\theta_{15}$	…	$15*d*\sin\theta_{15}$	$16*d*\sin\theta_{15}$
$f(\theta_{16})$	$1*d*\sin\theta_{16}$	$2*d*\sin\theta_{16}$	$3*d*\sin\theta_{16}$	…	$15*d*\sin\theta_{16}$	$16*d*\sin\theta_{16}$

Each of these functions generates a linear phase slope versus frequency that can be evaluated in Excel. Then each of the functions can be taken and broken into real and imaginary parts. Table 3 is generated with each of the functions for the real part and Table 4 is generated for the imaginary part.

Table 2: Real Part for the Sixteen Functions

	1	2	3	…	15	16
f($real\theta_1$)	cos(d*sinθ_1)	cos(2*d*sinθ_1)	cos(3*d*sinθ_1)	…	cos(15*d*sinθ_1)	cos(16*d*sinθ_1)
f($real\theta_2$)	cos(d*sinθ_2)	cos(2*d*sinθ_2)	cos(3*d*sinθ_2)	…	cos(15*d*sinθ_2)	cos(16*d*sinθ_2)
f($real\theta_3$)	cos(d*sinθ_3)	cos(2*d*sinθ_3)	cos(3*d*sinθ_3)	…	cos(15*d*sinθ_3)	cos(16*d*sinθ_3)
…	cos(d*sinθ_n)	cos(2*d*sinθ_n)	cos(3*d*sinθ_n)	…	cos(15*d*sinθ_n)	cos(16*d*sinθ_n)
f($real\theta_{15}$)	cos(d*sinθ_{15})	cos(2*d*sinθ_{15})	cos(3*d*sinθ_{15})	…	cos(15*d*sinθ_{15})	cos(16*d*sinθ_{15})
f($real\theta_{16}$)	cos(d*sinθ_{16})	cos(2*d*sinθ_{16})	cos(3*d*sinθ_{16})	…	cos(15*d*sinθ_{16})	cos(16*d*sinθ_{16})

Table 3: Imaginary Part of the Sixteen Functions

	1	2	3	…	15	16
f($imag\theta_1$)	sin(d*sinθ_1)	sin(2*d*sinθ_1)	sin(3*d*sinθ_1)	…	sin(15*d*sinθ_1)	sin(16*d*sinθ_1)
f($imag\theta_2$)	sin(d*sinθ_2)	sin(2*d*sinθ_2)	sin(3*d*sinθ_2)	…	sin(15*d*sinθ_2)	sin(16*d*sinθ_2)
f($imag\theta_3$)	sin(d*sinθ_3)	sin(2*d*sinθ_3)	sin(3*d*sinθ_3)	…	sin(15*d*sinθ_3)	sin(16*d*sinθ_3)
…	sin(d*sinθ_n)	sin(2*d*sinθ_n)	sin(3*d*sinθ_n)	…	sin(15*d*sinθ_n)	sin(16*d*sinθ_n)
f($imag\theta_{15}$)	sin(d*sinθ_{15})	sin(2*d*sinθ_{15})	sin(3*d*sinθ_{15})	…	sin(15*d*sinθ_{15})	sin(16*d*sinθ_{15})
f($imag\theta_{16}$)	sin(d*sinθ_{16})	sin(2*d*sinθ_{16})	sin(3*d*sinθ_{16})	…	sin(15*d*sinθ_{16})	sin(16*d*sinθ_{16})

When the real part is graphed, each function plots out as sinusoidal functions of different frequencies, and these are 90° out of phase with the imaginary part. The real and imaginary functions become the basis functions and they will be stored in the VHDL code. They will need to be converted from decimal to fixed point so that they can be operated on.

The hardware provides sixteen I and Q values based on measured data from each of the sixteen phase centers. The IQ demodulator generates sixteen Is at sixteen points, which are the real part, and sixteen Qs at sixteen points, which are the imaginary part, and they are analog voltage values that represent real and imaginary parts of measured return from the scene where the energy is coming in from different angles.

For each angle θ, the image energy at θ can be calculated doing the complex multiply using the following Equation 1:

$$\left[\left(R_{n,\theta n}\right) - j\left(I_{n,\theta n}\right)\right] \times \left[\left(I_{nd}\right) + j\left(Q_{nd}\right)\right]$$

Equation 1: Complex Multiply for Basis Function and I and Q Data

This equation can be applied sixteen times for each of the sixteen points with all θs. It can be simplified in the following manner with Equation 2 for the real part and Equation 3 for the imaginary part:

$$f(realcomp\theta_n) = \left(R_{n,\theta 1} \times I_{nd}\right) + \left(I_{n,\theta n} \times Q_{nd}\right)$$

Equation 2: Complex Multiply for the Real Part

$$f(imagcomp\theta_n) = \left(-I_{n,\theta n} \times I_{nd}\right) + \left(R_{n,\theta n} \times Q_{nd}\right)$$

Equation 3: Complex Multiply for the Imaginary Part

In order to get the amplitude for each of the sixteen functions, the real part of each of the sixteen functions for each of the thetas will have to be summed and the total sum will be squared, and the same will be done for the imaginary part of each of the sixteen functions for each of the θs. Then these squared values obtained, named $real_{\theta n}$ and $imag_{\theta n}$ in this case, will be used to finally calculate the amplitude to be graphed with the following Equation 4:

$$A_n = 20 \times \log[(real_{\theta n} + imag_{\theta n})^{1/2}]$$

Equation 4: Amplitude for Each Angle

For image formation, the sum of the energy from some of the scatterers is taken and they are decomposed by multiplying them by the basis functions. The basis function represents the energy that will come in from a different angle, so if it is multiplied by the total energy, it decomposes it into just that part.

With Fourier transform, the amplitude versus time is being calculated; however, in this case, the amplitude versus angle is being calculated. Fourier transform is used to decompose the waveform into the amounts of energy that come in from different angles. Instead of having a coefficient that represents energy at a frequency, the coefficient of energy that come in at a certain angle is being represented. All of these calculations are part of the long version of the complex Fourier transform at a more physical sense. Appendix 10.1 shows an example done for the signal processing for further explanation.

2.2 Major Components of the System

2.2.1 Electrical System

2.2.1.1 Signal Transmit Chain

The transmit signal chain is responsible for generating the radio frequency (RF) signal that will propagate throughout the entire radar system. The transmit chain is designed such that the frequency of the signal will be in the X band frequency range, 10 GHz. In order to generate the RF signal a voltage controlled oscillator was used in the design. The VCO however generates a low frequency and low power signal. In order to compensate for the low power signal a couple of amplifiers are used in the transmit chain as well as a frequency multiplier. The transmit chain also has two switches, a SPDT and a SP4T switch. The SPDT allows the system to switch between transmit and receive mode. The SP4T switch in allows the system to switch between the four transmit antennas.

2.2.1.2 Receive Signal Chain

The receive signal chain is responsible for receiving the reflected RF signal scatterings from the target objects in the scene extent. This will be accomplished by using the 16 receive antennas of which will be sampled from one at a time through the use of the SP16T switch. The

receive signal chain is also responsible for passing the signal to PC where the signal processing will take place. In order for the signal processing to take place the necessary phase and amplitude of the signal must be obtained. This is handled by the IQ demodulator. However before the phase and amplitudes of the received signal can be processed they have to be converted to digital voltages, this is done by the analog to digital converters onboard the FPGA. Once those voltages are converted they are sent to the PC for signal processing. The PC then returns the processed imagery to the FPGA and it is sent to the VGA to be displayed.

2.2.1.3 IQ Demodulator Chain

The IQ demodulator is a very important component in the electrical subsystem. As stated earlier, it is responsible for interpreting the phase and amplitude of the received signal and converting that information into voltages. The IQ demodulator is connected to both the transmit and receive chains. In short, this is based on the fact that the phase and amplitude are generated when a signal is applied to the LO channel; so each time the system switches to receive mode as in when a signal is input into the LO channel, the IQ demodulator outputs the phase and amplitude information from the I and Q channels.

2.2.1.4 Dual Level Shift Circuit

The level shift circuit was designed to convert the output voltage from the I and Q channels (±340mV) of the IQ demodulator to the range of 0 to 3.3V. The level shift circuit is needed to due to the fact that the analog to digital converters only accept voltages within that range. Shifting the voltages from the IQ demodulator will be accomplished using a comparator circuit.

2.2.1.5 Power Supply Board

The majority of the components in the electrical system require a source of power to operate. The power supply board was designed to distribute and maintain a constant source of power for those components to operate. The main source of power for the power supply board will be nine DC power supplies that plug into the standard wall outlet (120V 60 Hz). The power delivered to the board will then be regulated using multiple linear voltage regulators. Once the necessary voltages are generated they will then be distributed to the corresponding components in the electrical subsystem.

2.3 Subsystem Requirements

2.3.1 Electrical System

2.3.1.1 Transmit Signal Chain

The purpose of this subsystem is to generate and transmit a radio frequency (RF) signal that will be emitted into the area to be scanned by the radar. This subsystem is also responsible for establishing an operating frequency for the entire radar. The signal generation starts with the voltage controlled oscillator (VCO). The VCO used in the design has an output power of -4dBm

(0.398 mW) and operates at a frequency range of 4.38 GHz – 5.1 GHz. The next component in the signal transmit chain is the super ultra wideband amplifier. This amplifier was placed here because it was needed to provide enough input power into the frequency multiplier. The gain of this amplifier is 26dB. An important concept that was taken into consideration is the 1dB compression point (P1dB). This is the point in which the gain for linear amplifiers is no longer fixed for that specific frequency range. It is at this point where the output power becomes compressed and is no longer linearly proportionate to the input power. The P1dB for this component is 24 dBm, thus while completing the analysis the output power from the wideband amplifier was confined to less than 24 dBm. Also it is good engineering practice to leave a margin of error when calculating the output power therefore the output power from this component was designed to be 21.88 dBm (149.97 mW). The VCO and wideband amplifier are connected by a cable of which the calculated gain is -0.12 dB. The next component in the chain is single pole double throw (SPDT) switch. This component allows the radar to switch between transmit and receive modes. The SPDT switch has a P1dB value of 27 dBm and a gain of -2 dB; with an input power of 21.76 dBm the output power from the SPDT was calculated to be 19.76 dBm. The next major component in the signal transmit chain was the frequency multiplier. The purpose of the frequency multiplier is to double the input frequency. As stated before, the frequency generated by the VCO is in the range of 4.38 GHz – 5.1 GHz, once the signal reaches the frequency multiplier it is then doubled to the desired range of approximately 10 GHz. Due to the restriction of the input power to the frequency multiplier being 12 dBm, a fixed attenuator was added to the signal transmit chain between the SPDT and the frequency multiplier. The attenuation level set in the calculations is -10 dB; this is considered a loss to the overall gain of the chain.

The next component in the transmit signal chain is a variable attenuator. The attenuation was set to -12dBm. The input power into this component was 8.82 dBm results in an output power of -1.18 dBm. This attenuator precedes a band pass filter as well as power amplifier. This meant that the output power from the amplifier had to be less than 30 dBm which it was calculated to be 29 dBm. The band pass filter was used to provide a more accurate frequency for the transmit signal chain. Its center frequency value is 10.5 GHz which is aligned with the frequency that the customer specified. The band pass filter contributes a loss of 3dB to the chain. Next is the power amplifier. The power amplifier has a gain of 30 dB and a P1db compression value of 30 dBm. The output power of the amplifier is 25.5 dBm. After the power amplifier follows the single pole four throw (SP4T) switch. The SP4T is used to switch the output signal from being emitted by the four transmit antennas. It has an input P1db compression point of 24 dBm and a gain of -2 dB. The output power calculated from this component was 20.38 dBm and was followed by a cable loss of 1.41 dB. The final transmit power generated by this chain was 18.97 dBm. The overall goal in the analysis of the transmission chain is to calculate the power progressed through the path up until the antennas. This is the value that was used in the signal to noise ratio equation. This was accomplished by accounting for the gains and losses of the components in the chain. The transmit power of this signal is to be within the limits of safety as set by the rules regarding safe human exposure to electromagnetic RF fields, set forth by the Federal Communications Commission (FCC). The limit is 10 W/m^2, at the distance of 6 meters our peak transmit power of 18.97 dBm (78.89 mW) is well within the safety limits.

2.3.1.2 Receive Signal Chain

The purpose of this subsystem is to receive the RF signal scatterings that are reflected from the target and convert those signals to digital voltages to be used in the signal processing. The analysis for this chain includes calculating the power of the signal that it transmitted through this chain as well as the noise figure and noise temperature contributed by each component. The noise figure for components that have a negative gain (loss) is equal to that gain in dB. For components with a positive gain the noise figure is given in the datasheet. Equation 5 for noise temperature for all components is shown below:

$$\boldsymbol{nt = 290°K(10^{\frac{nt(dB)}{10}} - 1)}$$

Equation 5: Noise Temperature

The actual signal power received by the receive antenna is discussed in a later section; for now this value is to be considered as -51.825 dBm. The value seen by the input to the single pole 16 throw (SP16T) switch is added to the gain of -1.41 dB from the cable that connects the SP16T switch to the receive antennas. In total the calculated input power to the SP16T was -53.235 dBm. The SP16T switch has a gain of -4.7 dB and a P1db compression point of 24 dBm. The calculated output power of the SP16T switch is -57.935 dBm which is well below the 24 dBm compression value. Also because the SP16T switch has negative gain the noise figure is equal to 4.7 dB. The next component in the receive signal chain is the band pass filter. The band pass filter is used to provide precision to the frequency of the received signal scatterings reflected off of the target. The calculated received power for this component is -58.085 dBm, the gain is -3 dB and the output power is -61.085 dBm. The next component in this chain is a low noise amplifier. This component is used to amplify the power of the receive signal and amplify the noise as least as possible. The gain of this amplifier is 38 dB which results in a calculated output power of -23.085 dBm. The calculated output power of this component is less than the P1dB compression point which is 24 dBm. The noise figure listed in the data sheet is 2.2 dB. A variable attenuator was placed in the chain after the low noise amplifier. The purpose of using a variable attenuator is to allow for the power in the chain after this point to be adjusted. In the calculations the attenuation used was -4 dB. This will limit the input power to the RF channel of the IQ demodulator. The next component in the chain is another low noise amplifier. This was added to increase the signal power input into the RF channel of the IQ demodulator. In short the reason that the input power of the RF channel of the IQ demodulator deals with the output DC voltage that will be generated by the IQ demodulator. This concept will be elaborated on later in the paper. The point to note now is that the output power of this low noise amplifier was calculated as 10.675 dBm due to the gain of 38 dB.

The overall goal of the analysis for the receive chain was to calculate the noise power received from the reflections off of the target. This value is with respect to the analog to digital converters which act as the receiver for the entire radar system. In order to calculate this value the noise figure for the entire receive chain was needed as well as the gain. Calculating the gain was straightforward the value was 55.380 dB. However for the entire noise figure the analysis required more thought. In order to calculate the chain noise figure a cascade model was used. This involved calculating the noise figure of the chain as each additional component was added to the chain. At the end of the last component which was the IQ demodulator the noise figure for the entire chain was equal to that value calculated. The equations are shown below:

$$nf_N \text{ (magnitude)} = nf_1 + \frac{nf_2 - 1}{gain_1} + \ldots + \frac{nf_N - 1}{gain_1 * \ldots * gain_{N-1}}$$

Equation 6: Cascaded Noise Figure

$$nt_N \text{ (magnitude)} = nt_1 + \frac{nt_2 - 1}{gain_1} + \ldots + \frac{nt_N - 1}{gain_1 * \ldots * gain_{N-1}}$$

Equation 7: Cascaded Noise Temperature

$$N \text{ (dBm)} = N_n \text{ (dB/Hz)} + G_{Rx} \text{ (dB)} + NF \text{ (dB)} + B_L \text{ (dB)}$$

Equation 8: Noise Power at the Receiver

N_n: Thermal noise due to nature = -174dBm/Hz
G_{Rx}: Gain of the receive signal chain = 55.380 (dB)
NF: Noise figure of the receive chain using the cascaded approach = 11.620 (dB)
B_L: Limiting bandwidth of receiver = 275 MHz

When calculating the cascaded noise figure it was noticeable that after the first low noise amplifier the cascaded noise figure did not change much. This was due to the relatively high gain of the low noise amplifier in comparison to the other components in the chain. After performing the calculations the noise figure for the receive chain was 14.521 (magnitude) or 11.620 dB.

The next step in the calculations was to calculate the noise power at the receiver. This is shown in equation 9 above. After inputting the values, the noise power calculated at the receiver was -22.607 dBm (5.487e-3 mW).

2.3.1.2.1 Signal to Noise Ratio

$$\frac{S}{N} = \frac{Received\ Power\ at\ Receiver}{\text{Noise Power at Receiver}}$$

Equation 9: Signal to Noise Ratio

$$P_r = \frac{P_t G_t G_r \sigma}{4\pi R^2} \text{ (mW)} = 10 * \log\left(\frac{P_t G_t G_r \sigma}{4\pi R^2}\right) \text{ (dBm)}$$

Equation 10: Received Power

The signal to noise ratio (SNR) is the measure of the ability of a radar to detect a target at a distance away from the radar. Equation 10 is a way in which the target, the radar, the range of the target, and the properties of the medium through which the signal will travel are related mathematically. The physical properties of the target that affect the SNR is the target's radar cross section. The radar cross section is the measure of how detectable the object is by a radar. In the analysis the radar cross section was calculated for a trihedral corner reflector. This shape was chosen by the customer; it would have been much simpler to use a sphere however the trihedral was chosen. The lengths of its sides are 0.0508 meters. Equation 11 is used to calculate the maximum radar cross section this trihedral is shown below:

$$\sigma_{max} = \frac{12\pi L^4}{\lambda^2} (m^2) = 10*\log(\frac{12\pi L^4}{\lambda^2}) \text{ (dBsm)}$$

Equation 11: Maximum radar cross section of a trihedral corner reflector

The value solved for the radar cross section used in the SNR equation was -5.5446 dBsm. The radar characteristics that were used in the SNR equation included the power transmitted and the characteristics of the antenna aperture. As explained before the transmitted power (P_t) was determined by the components in the signal transmission chain and the value calculated was 18.97 dBm (78.886 mW). The properties of the antenna aperture that are used in this equation are the gain of both transmit and receive antennas. The gain for the transmit and receive antennas are 17 dB.

The signal to noise ratio as shown in Equation 9 uses the signal power at the input of the receiver which in this case is the output power from the IQ demodulator (5dBm). The SNR equation also uses the noise power at the input of the receiver which was calculated using equation 10 shown above (-25.4dBm). Since these values are calculated in dBm, SNR (dB) = S(dBm) – N(dBm), which results in a value of 30.4 dB.

Table 4: Receive Chain Noise Characteristics

Component	NF (dB)	NF	NF (cascade)	Noise Temp (K)	Noise Temp cascade (K)
Cable (from RX antenna)	1.41	1.384	1.384	111.234	108.800
SP16T	4.7	2.951	4.083	565.851	452.536
Cable	0.15	1.035	4.227	10.191	477.479
Band Pass Filter	3	1.995	8.433	288.626	1731.775
LNA:SLNA-120-38-22-SMA	2.2	1.660	12.454	191.280	4812.410
Cable	0.12	1.028	12.454	8.125	4812.420
Variable Attenuator	4	2.512	12.454	438.447	4812.998
Cable	0.12	1.028	12.454	8.125	4813.011
LNA:SLNA-180-38-25-SMA	2.5	1.778	14.520	225.701	7921.623
Cable	0.12	1.028	14.520	8.125	7921.645
RF (IQ Demodulator)	7	5.012	14.521	1163.443	7922.915

2.3.1.3 IQ Demodulator Chain

The IQ demodulator is a key component in the electrical system. It is used to relay the amplitude and phase of the incoming RF signal to the analog to digital converters. The IQ Demodulator converts the amplitude and phase information to DC voltages. This is done based on the theory of the IQ demodulator. In short this process involves generating a amplitude from the I(t) and Q(t) signals. The amplitude is generated using the equations shown below:

$$A(t) = \sqrt{I^2(t) + Q^2(t)}$$

Equation 12: Amplitude of RF signal input to IQ Demodulator

$$\phi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right)$$

Equation 13: Phase of RF signal input to IQ Demodulator

The input power to the RF channel of the IQ demodulator was calculated to be 10.555 dBm, the IQ demodulator has a conversion loss of 7 dB, resulting in an output power of 3.555 dBm (2.267 mW). The output impedance of this component is 50Ω. The next step in the analysis was to calculate the voltage range of the I and Q outputs. This was done by using the equation below:

$$V_{dc} = \sqrt{Pout(W) + Zout(\Omega)}\ (V)$$

Equation 14: Output voltage range

This led to a calculated value for the maximum voltage output by the IQ demodulator as 336.7 mV, which occurs when the phase angle is 45° between signals I(t) and Q(t). However when the phase angle between the two signals is -45° the output voltage of the IQ demodulator is -336.7 mV, which results in an output voltage range of approximately -345 mV to 345 mV. The DC offset error of this particular model IQ demodulator at the extreme is +/-8mV. As stated before the large increase in gain in the receive path due to the two low noise amplifiers is necessary to increase the power of the input signal in order to allow the IQ demodulator to produce a DC voltage that is high. The DC output voltage needs to be high in order to make the DC offset error negligible. At 8 mV to 400 mV the DC offset error 2% of the output voltage. This is causes the DC offset to be negligible which is desirable.

This process occurs when a signal is input into the LO channel of the IQ demodulator or in other words when the SPDT switch is not driving the transmit signal chain. This is the reason for the SPDT switch which switches the radar between transmit and receive modes. The input signal must have a power of 5 dBm. This is the reason for the variable attenuator that comes after the SPDT switch, it is necessary to decrease the signal power that is amplified by the wideband amplifier to 5.55 dBm.

2.3.1.4 Dual Level Shift Circuit

As stated earlier the output voltage range of the IQ demodulator is ± 340 mV, however the analog to digital converters can only read positive voltages in the range of 0 to 3.3V. The solution to this problem was to use a level shift circuit for I and Q channels of the IQ demodulator. The level shift circuit is designed to convert input voltages within the range of ±340 mVdc to the range of 0 to 3.3V.

2.3.1.5 Power Supply Board

The power supply board was designed to generate and distribute the necessary operating voltages and currents to the components in the electrical system. The table below lists the requirements for the components.

Table 5: Power Supply Output Requirments

QTY	Part Name	V+(Vdc)	I+ (mAdc)	V- (Vdc)	I- (mAdc)
1	VCO	3.3	45	-	-
1	FPGA Board	3.3	200	-	-
1	SPDT Switch	5	1.4	-	-
1	SP4T Switch	5	160	-5	50
1	SP16T Switch	5	550(max)	-12	200(max)
1	IQ Demodulator	5	110	-5	-
1	Super Ultra Wideband Amplifier	12	400(max)	-	-
2	Ultra Wide Bandwidth Amplifier	12	62	-	-
1	Low Noise Amplifier SLNA-120-38-22-SMA	12	250	-	-
1	Low Noise Amplifier SLNA-180-38-25-SMA	12	280	-	-
1	Power Amplifier	15	900	-	-
2	Level Shift Op Amp (V+)	3.5		-	-
2	Level Shift Op Amp (VRef)	1.65	-	-	-

2.3.2 Antenna Hardware

The necessary hardware for the antenna design must be able to handle X-band frequencies and propagate a signal with a beamwidth that will cover a scene extent of at least 30 inches from a distance of 20 feet away. The highest gain value to create the precise beamwidth is 26 dBi. Attached to each horn antenna will be a Waveguide-to-coaxial adapter, which will convert analog signal and transform it to become electromagnetic waves ready for propagation. Selecting the proper hardware is critical to confirm the X-Band impedance matching process occurring within the horn antennas. The design will utilize X-Band horn antennas from Advanced Receiver and waveguide adapters (Part Number 90-462) from ARRA Inc.

2.3.2.1 MA86551 X-Band Horn Antennas

The MA86551 X-Band horn antennas are from Advanced Receiver. Each horn has a gain level of 17 dBi that will create a beamwidth of 25°, covering a scene extent of 9 feet squared, which will cover the minimum scene extent of 30 inches squared. The antennas will mate with a WR90 waveguide adapter and has a UG-39/U flange. WR90 represents horns or transmission lines functioning at X-Band frequencies, and the UG-39/U signifies the horn antenna will be brass. Table 6 is the MA86551 X-Band horn antenna's data sheet, and he dimensions for the MA86551 horn antennas are list in Table 7 and illustrated in Figure 6.

Table 6: MA86551 Horn Antenna Data Sheet

Horn Antenna Specifications Data Sheet	
Center Frequency	10.525 GHz
Frequency Range	8 – 12.4 GHz
Nominal Gain	17 dBi
H-Plane (Azimuth) Beamwidth	25°
E-Plane (Elevation) Beamwidth	25°
Scene Extent	9' x 9'
RF Connection	UG-39/U
Price	$20.00 per antenna

Table 7: Horn Antenna Dimensions

MA86551 Horn Antenna Dimensions	
Length	3 in.
Width	3 in.
Height	3.688 in.
Waveguide Entry	1.280 in.
Flange Size	1.625 in.

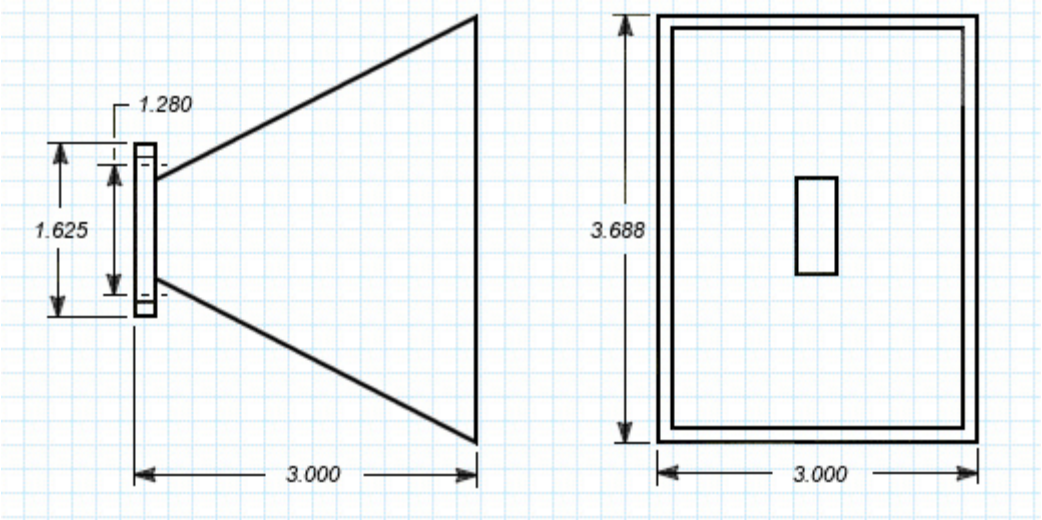


Figure 6:MA86551 Horn Antenna Dimensions

2.3.2.2 Waveguide Adapter

The ARRA Inc. waveguide adapter part number 90-462 covers the X-Band frequency range and will be sufficient for transforming the analog signal from a coaxial cable to waveguide and eventually out the horn antenna. The adapter will also be able to perform the transformation in reverse, converting a received signal wave into an analog voltage. To be noted, each horn antenna is required to be connected to a waveguide adapter, making this component a high need. Table 8 lists the specifications for the P/N 90-462 waveguide adapter.

Table 8: Waveguide Adapter Specification Sheet

Specification Sheet
P/N 90-462
Cover Flange / UG39-U Flange
SMA Female Connector
Standard label
ARRA standard blue color
SMA Connector
Frequency 8.2-12.4Ghz
VSWR 1.25
Price $170

2.3.3 Software Design

From the design of the SAR Imager, recall this requires the FPGA to output a 20 ns pulse (20 ns on and 20 ns off) for a target 20 feet away since the speed of the signal is around 1 ns per foot in air. This report will describe the aspects of the coding design process that will take place and also note any changes from the previous design and the reasoning behind this.

The first thing that was changed was the actual timing for the switches on the primary timing diagram. Note that for all the switches and signals in this project, a logic 1 will be considered on and a logic 0 will be considered off. A new period of 160 ns was used for the signals

controlling the transmit signals. The first part of the explanation of the timing will be the transmit mode. Since the timing for the transmit mode being on must be 20 ns, the signal SPDT (transmit mode signal), the SP4T signal (transmit antenna signal) and the pulse signal (output of the pulse, signal actually leaving the transmit antenna) all should have the same timing. This yields the SPDT (switch to alternate between transmit and receive mode), SP4T (switch which controls which of the four transmit antennas is the one emitting the signal) and the pulse (actual signal getting transmitted from the selected transmit antenna) signals all having a 20 ns logic 1 (on) when the system is in transmit mode.

For the receive mode, the SPDT signal, the SP4T signal, and the pulse signal should all be logic 0 (off). A time period of 140 ns was used for receive mode to allow plenty of time for settling, switching, and component delay. A total period of 160 ns was picked because this allows for the 20 ns of transmit mode (when pulse, spdt, and sp4t are all logic 1) and 140 ns of receive mode (where the transmit mode signals are all off).

For the receive mode, the only switches which should be on (have logic 1) should be the receive antennas. The receive antennas are controlled by a signal called SP16T, which will control which of the receive antennas will receive logic 1 at a certain time period, as the receive antennas with a logic 1 signal are the only antennas receiving signal. Note that the SP16T will be on for 20 ns, which would receive the entire 20 ns pulse that was from the transmit antenna. The SP16T signal will be logic 1 20-40ns after the pulse transmit mode is turned off. This is because at 20 ns when the transmit signal is finally finished and turned off, the beginning of the 20 ns signal is already hitting the target 20 feet away while the end of the signal is still leaving the transmit antenna. 20 ns later the signal that was previously hitting the target is now hitting the receive antennas, and the signal that was previously leaving the transmit antenna is now hitting the target. This is when the receive antenna is turned on (via logic 1 on the SP16T signal), and for the next 20 ns it would be receiving to encompass the entire signal that was hitting the target.

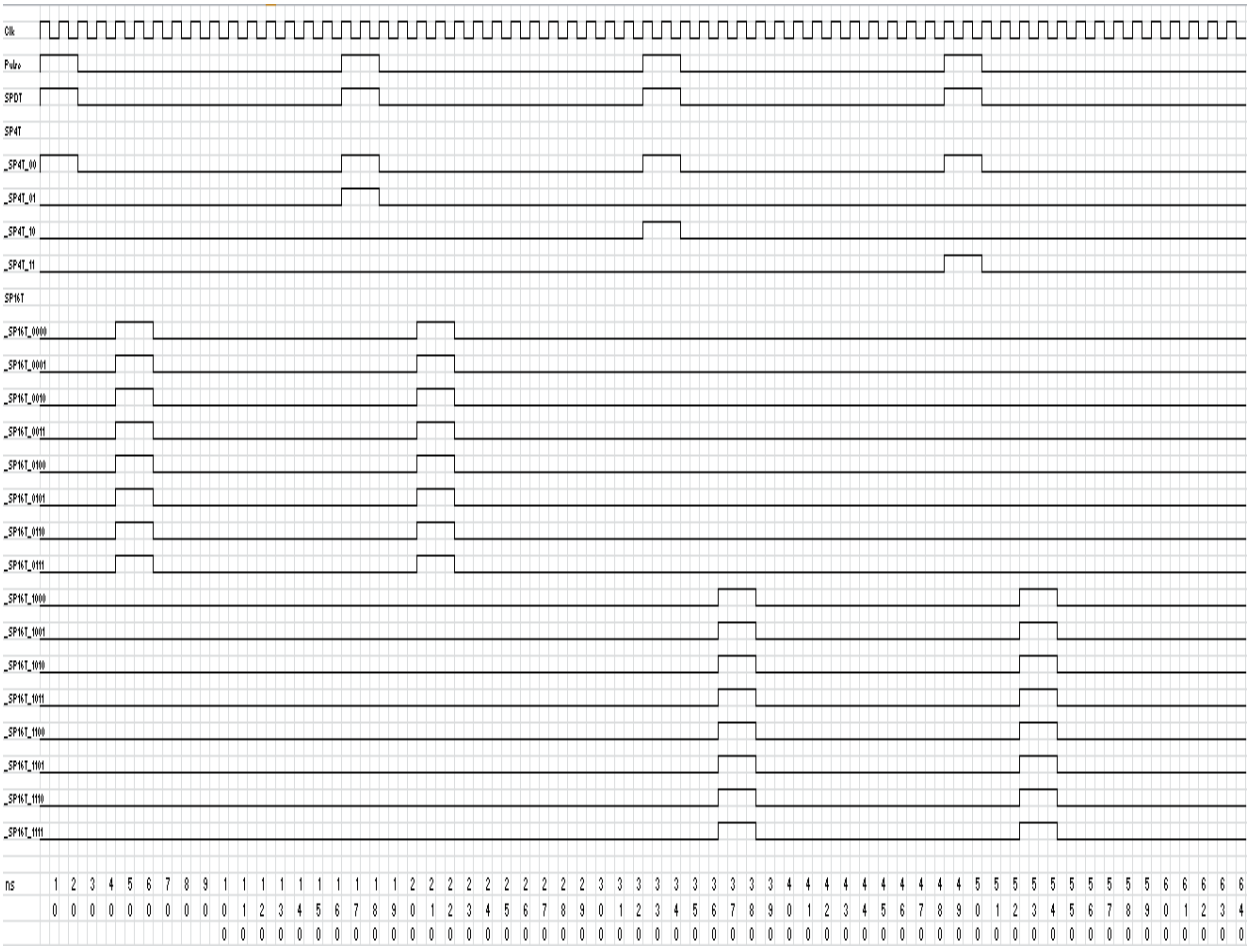


Figure 7: Revised Timing Diagram of the SAR Imager system

2.4 Performance Assessment

2.4.1 Functional Assessment

The number of phase centers for the static SAR system is 32 total. Each antenna array accounts for 16 phase centers and each end transmit antenna is responsible for 8 phase centers (REQF-010). The amount of phase center is the amount of half way points exist between transmit and receive antennas. The distance between phase centers is 3λ. 3λ was a simulated distance that spaced the radars grating lobes far enough apart to avoid ambiguities (REQF-011).

2.5 Overall Risk Assessment

2.5.1 Shipping Risks

Risk: Northeast Snow Blizzard Delays Shipping

Consequence: The Coaxial Waveguide Adapter from ARRA has been ordered. However, the shipping time has been delayed due to the ongoing snow blizzard in the Northeast corner of the

United States. The Coaxial Waveguide Adapters connect to the antennas and without the coaxial waveguide adapter the system will not propagate the signal.

Mitigation Strategy: Keep open contact with vendors for updated delivery times once the snow blizzard passes. If unable to get desired vendor at optimal price, the team will have to order from another vendor at a higher price.

2.5.2 Budget Risks

Risk**:** Insufficient Funds

Consequence**:** If the $50,000 budget is spent before all parts, assemblies, and support material have been ordered then the project will not be completed. Current items that are placing restrictions on the budget include the frame assembly, radar absorbing foam, switches, and miscellaneous support material (lasers, extension cords, power supplies, etc.).

Mitigation Strategy**:** To find savings in the budget, the mechanical engineers are performing price comparisons amongst local vendors for a competitive quote for welding the frame assembly as well as lower material cost. Also, to reduce the amount of money spent on the radar absorbing foam, the team will calculate the exact amount of foam required to cover the scene to avoid over purchasing. The switches were the most expensive electronic components. The difference in vendor pricing was dependent upon the delivery lead time. To avoid overspending, the team chose the vendor with the most reasonable lead time in accordance to the semester's scheduled milestones.

2.5.3 Project Risks

2.5.3.1 Software Development Risk

Description:
During the design process, the software design may be inadequate or incomplete as far as the scope of the project is hoped to reach. This includes generating code that will allow the FPGA to generate pulses, control timing of the switches, and if needed the signal processing of the results recorded. This may delay the testing strategies of the project time line and/or completion of the whole project itself.

Probability: Moderate
The coding level required to generate the pulses and timing for the system is not inherently difficult. The only difficulty that may arise will be just figuring out how to match the correct timing with the physical implementation of the project which could include unknown factors. If the PC cannot be used to do image processing using a program like Labview, then the image processing on the FPGA would be another factor that might be difficult to complete. This is because the FPGA used for the system (Digilent Nexys 3) does not come with image processing software.

Consequence: High
If the pulses and timing cannot be generated properly, then it is very hard to show results from the work of this project. This is a vital portion of the project that must be at least partially working to get some results. These results include anywhere from detecting signal with an RF meter, to having imaging on the VGA display.

Strategy:
If the FPGA cannot be programmed in such a way to generate the signals and the timing required for the SAR system, a very simplified version of the system can be utilized by using test equipment. This new system would include a pulse generator to generate the pulse, and a scope to display the image and that would do the image processing. With this new system the FPGA would not be needed. Overall this is just an extreme backup in case nothing else works for this project. If the PC cannot be used to do the Image processing, then the image processing would have to be done on the FPGA.

2.5.3.2 Signal Processing Risk 1: I-data and Q-data Not Collected

Description:
There is a risk that the data from the I-channel and the Q-channel are not collected from the IQ demodulator and stored in the FPGA board.

Probability: Low
The probability that the data is not collected properly is low as the FPGA board will be programmed to receive the information.

Consequences: Minor
There is an alternate way to get the data without having to rely solely on the programming, so the consequences are not significant.

Strategy:
A voltmeter can be attached to the I-channel and the Q-channel of the demodulator to get the data manually. This measured data will then be entered into an Excel spreadsheet that is set up as a backup, which will then be used to calculate the 16 amplitudes for image formation.

2.5.3.3 Signal Processing Risk II: Hardware Errors

Description:
There is a risk that hardware errors interfere with the image formation as every transmit/receive combination might not be the same as there is variability in the hardware.

Probability: Moderate
The probability that the data is not collected properly is moderate as the image formation calibration isn't accounting for all the different path lengths.

Consequences: Moderate

The consequences of this risk is moderate as it is an additional error that can be obtained empirically when the hardware is measured.

Strategy:
In order to obtain the hardware errors, the hardware will be measured using a voltmeter. The measured data will then be entered into the Excel spreadsheet that is set up as a backup, which will then be used to as calibration for image formation.

2.5.3.4 Signal Processing Risk III: Image Not Formed

Description:
The image may not be formed properly on the VGA display.

Probability: Moderate
The probability that the image is not properly formed and displayed is moderate as there may be errors in the calibration.

Consequences: High
The consequences of this risk are high as the signal processing goal is to try to obtain a one-dimensional image.

Strategy:
In order to obtain the one-dimensional energy, the Excel spreadsheet containing the signal processing and image calibration information would need to be verified in order to make sure that the data entered is all correct and makes sense. The next thing to do would be to verify that the signal is actually being transmitted and received in order to be processed. Then the image processing program would need to be looked over and debugged so as to verify that it is performing its function.

3 Design of Major Components

3.1 Electrical Design

3.1.1 Transmit Signal Chain

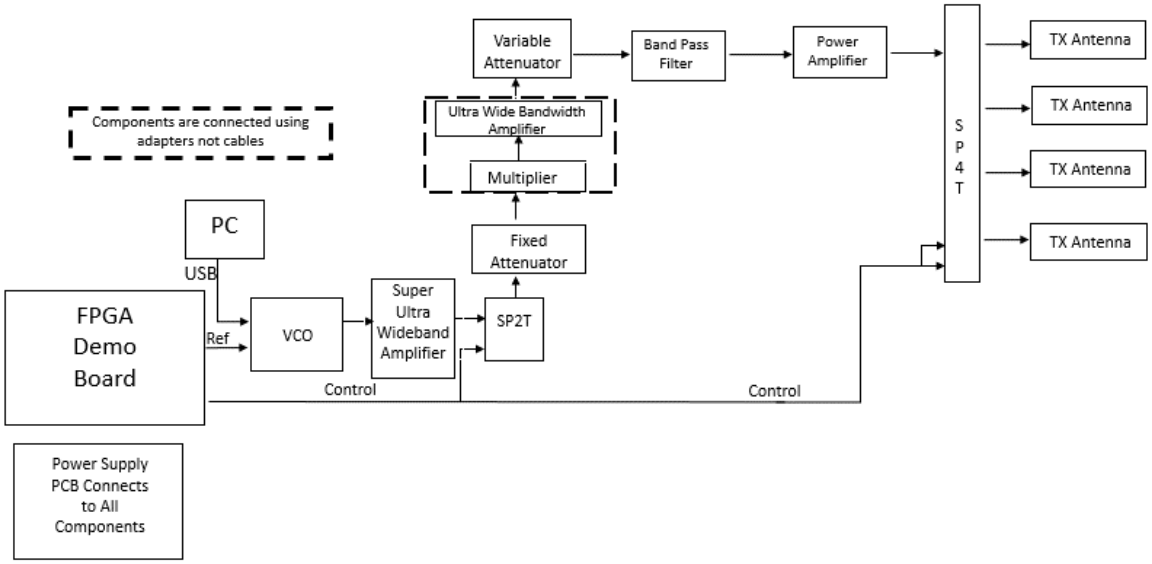


Figure 8: Transmit Signal Chain

The transmit signal chain is responsible for generating the RF signal that will be transmitted into the scene extent. The method by which the signal is generated is the VCO. The model chosen for this design generates a signal of -4 dBm at a frequency within the range of 4.38 GHz and 5.1 GHz. The next component in the transmit chain is the Super Ultra Wideband Amplifier. This amplifier was chosen because of its gain (26 dB) as well as its operating frequency range (700 MHz–18 GHz). The P1db compression point of this amplifier is 24 dBm however the output power of this design is 21.88 dBm. The cable that connects the VCO and the super ultra wideband amplifier is 3 inches long. It has a loss of 0.12 dB. This was based on the loss conversion factor of 0.47 dB/ft. This conversion factor applies to all cables in the electrical system that transmit the RF signal. Table 9 shows the places in the chain where there are cables. The next component is the SPDT; the purpose this component is to switch the system between transmit and receive mode. This model is capable of outputting a signal power of up to 27 dBm before the output begins to compress. This component was designed to output 19.76 dBm due to the loss of 2 dB inherent to this model. The next component in this design is a fixed value attenuator. This attenuator has a loss of 10 dB. The frequency multiplier is needed in this chain to increase the frequency of the system to 10 GHz. The loss associated with this component is 12.5 dB; the output of this component is designed to be -3.06 dBm. The next component is the ultra-wide bandwidth amplifier which has a gain of 12 dB. The designed output of this amplifier is 8.94 dBm, this takes into account the P1dB compression point of 10 dBm. The next component is the variable attenuator. The loss chosen for this component is 13 dB. This was attenuation level was chosen to limit the input power to the power amplifier that follows. The band pass filter is the next component after the variable attenuator. Its purpose is to center the frequency of the signal to 10.5 GHz. This

component has a loss of 3 dB and a P1db compression point of 30 dBm. With the loss in mind the output of this component is -7.3 dBm. The power amplifier follows the band pass filter. It has again of 30 dB and a P1db compression point of 37 dBm. The calculated output power of this component is 22.5 dBm. The SP4T switch follows, it has an input P1db compression point of 24 dBm. The calculated output of this component is 20.38 dBm, this takes into account the loss of 2 dB that is inherent to it. The cable that connects the SP4T to the transmit antennas is 36 inches long and has a loss of 1.41 dB.

Major risks for the transmit signal chain include:

- Component failure:
    - Consequences:
        - Signal may not be the correct frequency and/or strength
        - Component damage
    - Mitigation Strategy:
        - Ensure that all components will operate within their limits specified by the data sheets (input/output voltage, current, dBm)
- VCO Software Failure:
    - Consequences:
        - The VCO will not generate a signal with the correct frequency and/or strength
    - Mitigation Strategy:
        - Ensure that the appropriate registers have the correct programming data on the VCO

Table 9: Receive Chain Signal Characteristics

Components	Input Power (dBm)	Input Power (mW)	Gain (dB)	Output Power (dBm)	Output Power (mW)	P1db Compression (dBm)
VCO	0	1	0	-4	0.398	-
Cable	-4	0.398	-0.12	-4.12	0.387	-
Super Ultra Wideband Amplifier	-4.12	0.387	26	21.88	154.170	24
Cable	21.88	154.170	-0.12	21.76	149.968	-
SPDT	21.76	149.968	-2	19.76	94.624	27
Cable	19.76	94.624	-0.12	19.64	92.045	-
Fixed Attenuator	19.64	92.045	-10	9.64	9.204	-
Cable	9.64	9.204	-0.2	9.44	8.790	-
Frequency Multiplier	9.44	8.790	-12.5	-3.06	0.494	-
Ultra Wide Bandwidth Amplifier	-3.06	0.494	12	8.94	7.834	10

Cable	8.94	7.834	-0.12	8.82	7.621	-
Variable Attenuator	8.82	7.621	-13	-4.18	0.382	-
Cable	-4.18	0.382	-0.12	-4.3	0.372	-
Band Pass Filter	-4.3	0.372	-3	-7.3	0.186	30
Cable	-7.3	0.186	-0.2	-7.5	0.178	-
Power Amplifier	-7.5	0.178	30	22.5	177.828	37
Cable	22.5	177.828	-0.12	22.38	172.982	-
SP4T	22.38	172.982	-2	20.38	109.144	24 (Input)
Cable	20.38	109.144	-1.41	18.97	78.886	-

3.1.2 Receive Signal Chain

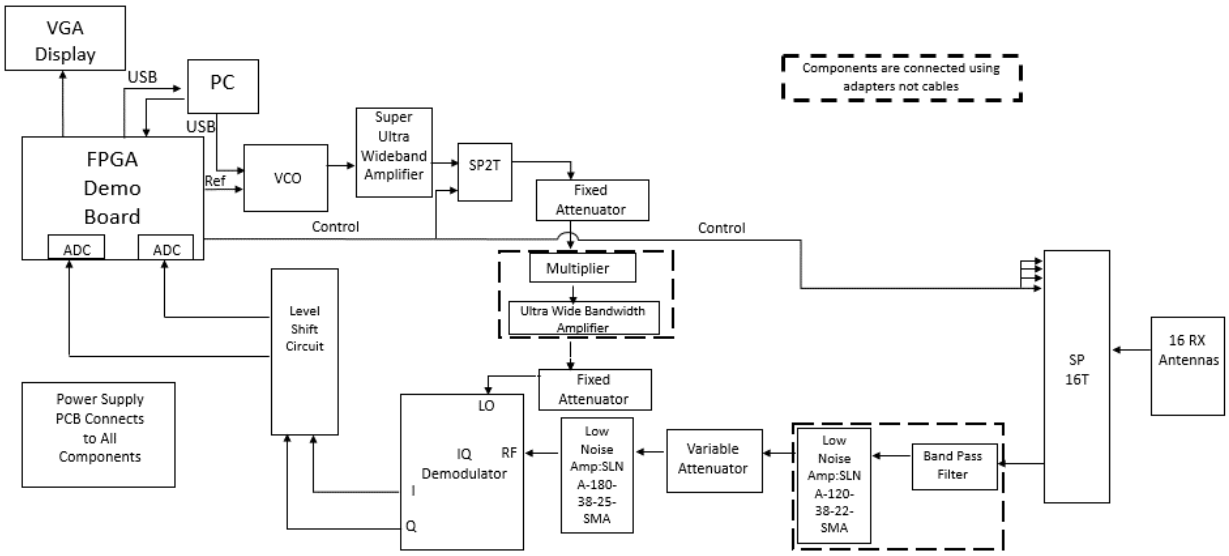


Figure 9: Receive Signal Chain

This chain was designed to receive the reflected signal scatterings from the target, interpret the phase and amplitude information of the signal, and create imagery using signal processing. The received power seen at the cable that connects the receive antennas to the SP16T is -51.825 dBm. The SP16T switch has a calculated input of -53.235 dBm, a loss of 4.7 dB and an output of -57.935 dBm. A band pass filter follows the switch; it has a loss of 3 dB and its output is -61.085 dBm. The next component is a low noise amplifier. This component has a gain of 38 dB and outputs -23.205 dBm. Next is a variable attenuator placed to limit the input to the low noise amplifier that follows it. The attenuation loss used in the calculations is 4 dB. This creates an output of -27.205 dBm from the attenuator. The low noise amplifier that follows the variable attenuator has a gain of 38 dB and a P1db compression point of 22 dBm. The calculated input power is -27.325 dBm and the output is 10.675 dBm. The signal received then propagates to the RF channel of the IQ

demodulator. The input P1db compression point is 12 dBm, the designed input to this channel is 10.555 dBm.

Major risks for the transmit signal chain include:

- Component failure:
    - Consequences:
        - Signal may not be the correct frequency and/or strength
        - Component damage
    - Mitigation Strategy:
        - Ensure that all components will operate within their limits specified by the data sheets (input/output voltage, current, dBm)

Table 10: Receive Chain Signal Characteristics

Component	Pin (dBm)	Gain (dB)	Pout (dBm)	Pout (mW)	Pout (W)
Cable (from RX antenna)	-51.825	-1.41	-53.235	4.748E-06	4.748E-09
SP16T	-53.235	-4.7	-57.935	1.609E-06	1.609E-09
Cable	-57.935	-0.15	-58.085	1.554E-06	1.554E-09
Band Pass Filter	-58.085	-3	-61.085	7.790E-07	7.790E-10
LNA:SLNA-120-38-22-SMA	-61.085	38	-23.085	4.915E-03	4.915E-06
Cable	-23.085	-0.12	-23.205	4.781E-03	4.781E-06
Variable Attenuator	-23.205	-4	-27.205	1.903E-03	1.903E-06
Cable	-27.205	-0.12	-27.325	1.851E-03	1.851E-06
LNA:SLNA-180-38-25-SMA	-27.325	38	10.675	1.168E+01	1.168E-02
Cable	10.675	-0.12	10.555	1.136E+01	1.136E-02
RF (IQ Demodulator)	10.555	-7	3.555	2.267E+00	2.267E-03

3.1.3 IQ Demodulator Chain

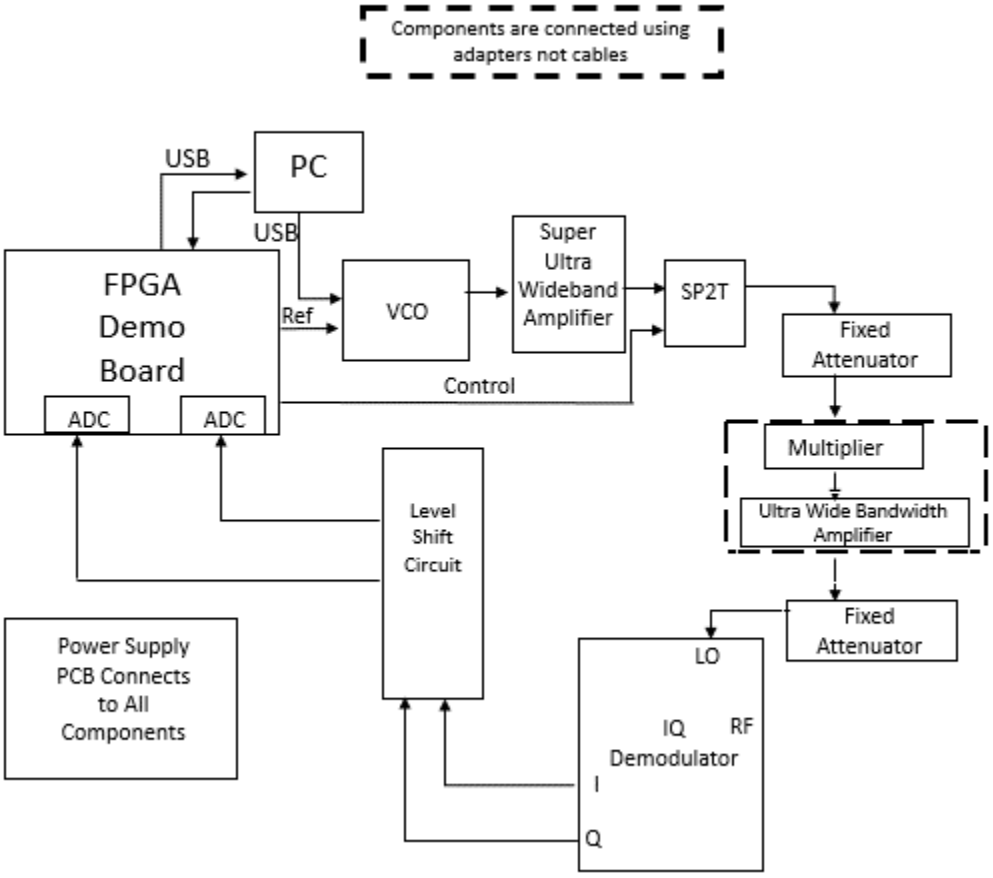


Figure 10: IQ Demodulator Chain

The IQ demodulator is important because it interprets the phase and amplitude of the received signals and outputs them as voltages. The IQ demodulator (LO) chain is the controller of the receive chain. The IQ demodulator only outputs the phase and amplitude voltages when the signal that enters the LO channel has the same frequency of the signal that enters the RF channel. The VCO, super ultra wideband amplifier, and the SPDT are considered to be in this chain because they drive the signal that enters the LO channel. The input and output power for all of the components are shown in Table11. A key factor that went into designing this chain was that the typical strength of the signal inputted into the LO channel should be within the range of 3 to 7 dBm, preferably 5 dBm.

Major risks for the IQ Demodulator include:

- Component failure:
    - Consequences:
        - Phases and amplitudes of the RF signal do not get interpreted correctly
    - Mitigation Strategy:

- Ensure that the component will operate within its limits specified by the data sheet (input/output voltage, current, dBm)

Table 11: IQ Demodulator Chain Signal Characteristics

Components	Input Power (dBm)	Input Power (mW)	Gain (dB)	Output Power (dBm)	Output Power (mW)	P1db Compression (dBm)
VCO	0	1.000	0	-4	0.398	-
Cable	-4	0.398	-0.12	-4.12	0.387	-
Super Ultra Wideband Amplifier	-4.12	0.387	26	21.88	154.170	24
Cable	21.88	154.170	-0.12	21.76	149.968	-
SPDT	21.76	149.968	-2	19.76	94.624	27
Cable	19.76	94.624	-0.12	19.64	92.045	-
Fixed Attenuator	19.64	92.045	-10	9.64	9.204	-
Cable	9.64	9.204	-0.2	9.44	8.790	-
Frequency Multiplier	9.44	8.790	-12.5	-3.06	0.494	-
Ultra Wide Bandwidth Amplifier	-3.06	0.494	12	8.94	7.834	10
Cable	8.94	7.834	-0.12	8.82	7.621	-
Fixed Attenuator	8.82	7.621	-3	5.82	3.819	-
Cable	5.82	3.819	-0.27	5.55	3.589	-
LO IQ Demodulator	5.55	3.589	0	-	-	-

3.1.4 Dual Level Shift Circuit

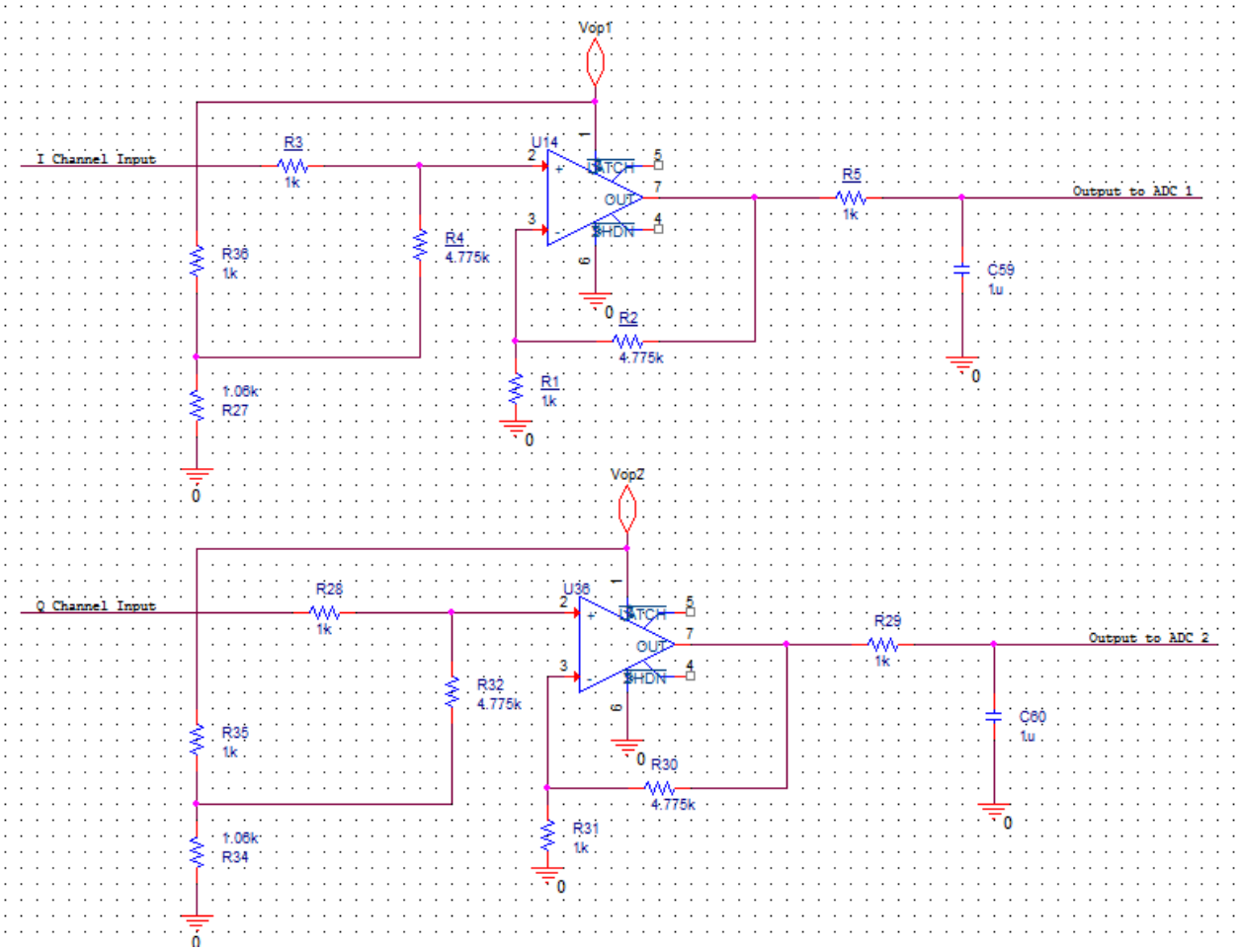


Figure 11:Dual Level Shift Circuit

This circuit was designed to shift the output voltages from the I and Q channels of the IQ demodulator (±340mVdc) to 0 to 3.3Vdc which is compatible for the input of the two analog to digital converters. This circuit was designed to have a gain of 4.85 (13.594 dB), which is the desired range of output 3.3V divided by the input range 680mV. Equation 15 shows the how the gain in magnitude was calculated. In order to shift the voltage to the range of 0 to 3.3Vdc the offset voltage needed to be 1.65 Vdc therefore the offset gain therefore with the node voltage at R27 being 1.65V.

$$A = \frac{R4}{R1} * \frac{(R1 + R2)}{(R3 + R4)}$$

Equation 15: Gain for level shift op amp circuit

$$A_{Offset} = \frac{(R2 + R1)}{R1} * \frac{R3}{(R3 + R4)}$$

Equation 16: Gain of the offset voltage

Major risks for the level shift circuit include:

- Component failure:
  - Consequences:
    - The conversion of the input to output voltages will not be accurate
  - Mitigation Strategy:
    - Ensure that the components will operate within its limits specified by the data sheet (input/output voltage, current)

3.2 Antenna Design

Having the T-shaped design with two linear antenna arrays; the transmit antennas spaced 3λ from the outer receive antennas; and the receive antennas spaced 6λ from their neighboring receive antennas was conceptually and theoretically determined based on various antenna theory guidelines. One linear antenna array aperture covers one dimension of a scene. The horizontal array aperture covers the azimuth dimension of the scene, and the vertical array aperture covers the elevation dimension of the scene. Thus, the two array aperture crossing will allow two dimensional scanning of a scene. Due to the low gain level of the antennas and large beamwidths, angling the horn antennas toward the scene extent is unnecessary.

3.2.1 Antenna Spacing

For each array aperture, eight receive antennas will be linearly aligned, spaced six inches apart from each antenna's center point. A transmit antenna will be placed on both ends of the array aperture, spaced three inches from the neighboring receive antenna. Figure 12 illustrates the design of one linear array aperture. The spacing and the antenna configuration will create 16 phase centers for one array aperture. Each phase center will be 3λ apart from each other.

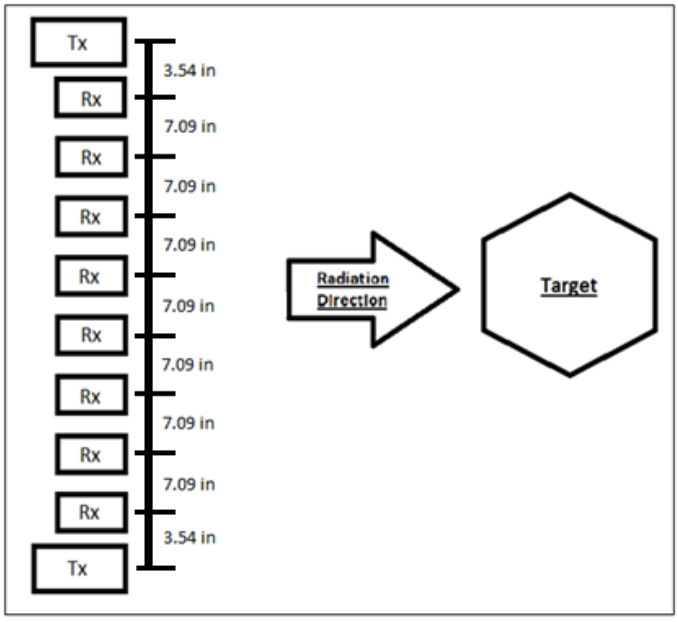


Figure 12: One Antenna Aperture Design

3.2.2 Phase Centers

The construction of one antenna aperture creates sixteen phase centers – a phase center is a maximum absorbance point of a reflected signal and is located between one transmit and one receive horn antenna. Each transmit horn antenna is responsible for eight phase centers. Two transmit antennas on both sides of an antenna aperture creates 16 phase centers per array aperture. The phase centers are spaced 3λ away from each other. The spacing between phase centers is calculated to prevent the main lobe from an antenna aperture to scan the size of the scene extent without having excessive grating lobes entering the scene – a grating lobe is radiation directed at a different angle than the main lobe and is similar in strength as the main lobe. If grating lobes enter the scene, receive antennas will gather multiple return signals and cause confusion and errors when processing the data. Figure 13 illustrates the phase center locations on one of the antenna array apertures. The red and blue arrows represent the phase centers in correlation to their same colored transmit antenna. Each antenna aperture has the same amount phase centers and at the same locations, theoretically. Thus, Figure 13 represents both the azimuth and elevation antenna arrays.

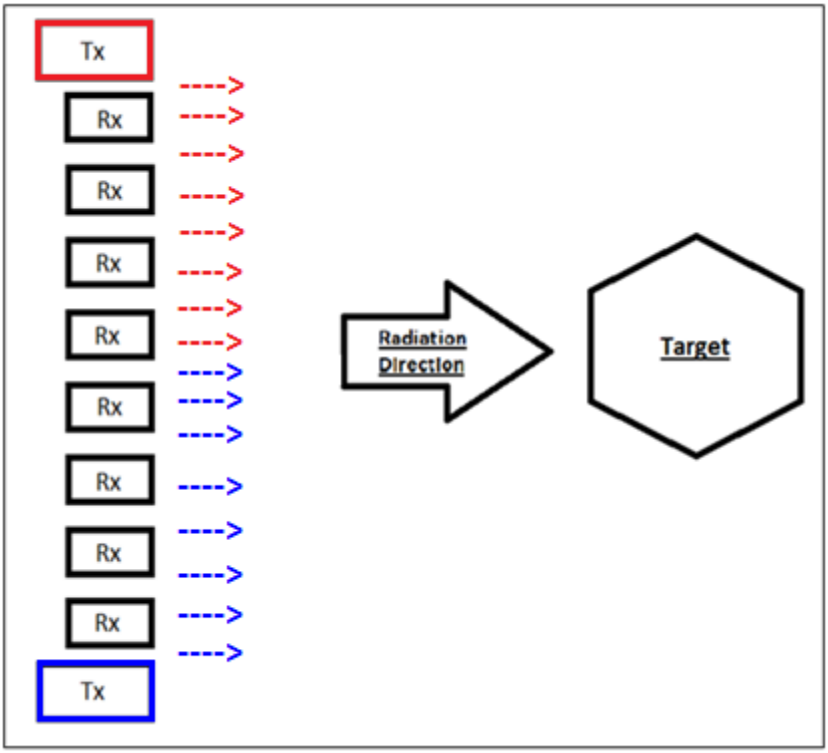


Figure 13: Phase Center Illustration

3.2.3 Linear Antenna Array Radiation Patterns

The arrangement of the horn antennas in a linear array and the 3λ spacing between phase centers creates a main lobe with grating lobes 20 degrees spaced from the main lobe. Justifying the 3λ spacing required generating the total radiation pattern equation based on multiplying the element factor and array factor equations. Once the total radiation pattern equation is complete, the next step is to plot the equation to simulate the beams originating from the antenna array. Once the main lobe and grating lobes are angled far enough apart based on the simulation plots, the distance is justified. For this design the 3λ is a workable distance and isolates the main lobe.

3.2.3.1 Total Radiation Pattern

The total radiation pattern equation is both the element factor and array factor multiplied together. The plots in Figure 14 demonstrate the distances between the main lobe and grating lobes, but also illustrates how to the grating lobes weaken as the zenith angle decreases or increase. The simulation plots of the total radiation pattern validate that the spacing of phase centers at 3λ will allow the main lobe of the linear antenna array to scan the scene without excessive grating lobes also propagating onto the scene. Equation 17 represents the total array radiation, and Table 12 specifies the variable values, which are the same from the element factor and array factor.

$$TAP = EF \cdot AF = (AF)_N = \left| \frac{1}{N} \frac{\sin\left(\frac{Nkd}{2}\sin(\theta)\right)}{\sin\left(\frac{kd}{2}\sin(\theta)\right)} \right| \cdot \sqrt{\cos(\theta)}$$

Equation 17: Total Array Radiation (TAP) Equation

Table 12: Total Radiation Pattern Variables

Total Radiation Pattern Variables		
Description	***Variable***	***Value***
Antenna Spacing	d	3λ
No. of Elements/Phase Centers	N	16
Wavelength	λ	0.03 m
k-constant = $\frac{2\pi}{\lambda}$	k	209.44
Zenith Angle Range	θ	0-90°

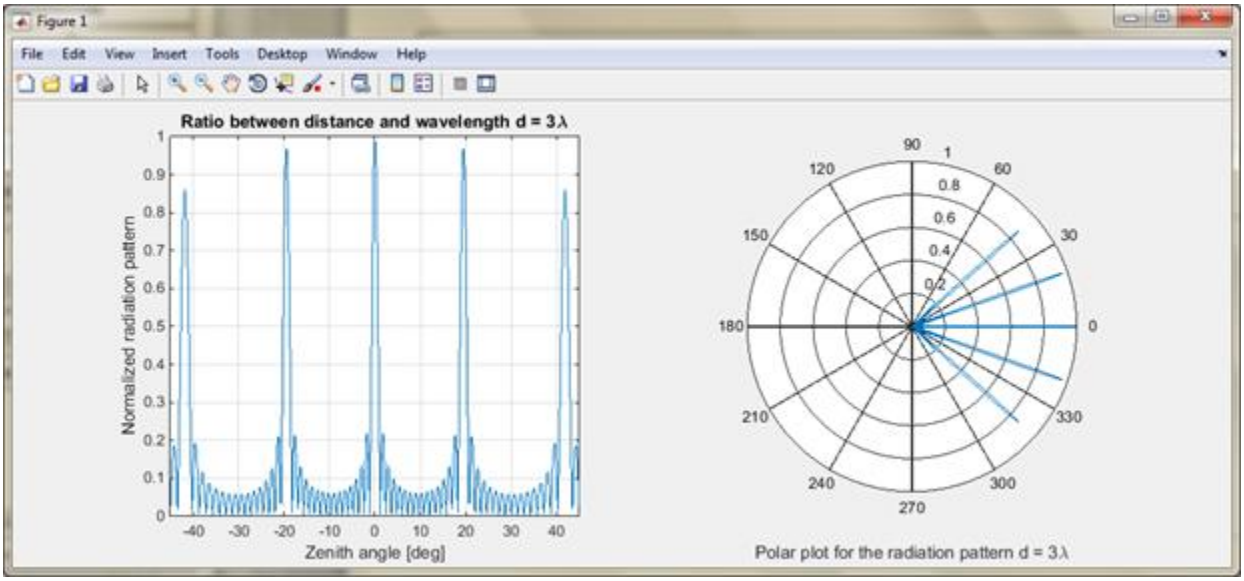


Figure 14: Total Radiation Simulation Plots

3.3 Antenna Structure Design

From the Mechanical aspect, the design of the antenna structure has been modified. Also, there have been additions to the structure. The additions consist of two trihedral and horn covers for each +individual antenna horn. The modification of the structure included the structure stand and the component box. These additions and changes have been made to accommodate the fabrication company that is yet to be decided. Along with the modified components, Test analysis has been conducted on each component. These test correspond to stress analysis displaying the durability of each component. Electrical heat dissipation has also been calculated to assure the component box will not over heat and cause a disturbance to the electrical components.

3.3.1 Refined Structure

In the following section, explanations of the modified components will be presented. Each modification is a resultant of lower cost material and easier manufactural parts. The new modifications have been calculated and adjusted accordingly to fit our parameters.

3.3.1.1 Horn Holders

The original idea for the horns was to have them be able to rotate toward the object area creating a dish effect. The structure was made in a way to hold the horns by welding a threaded rod onto the side of the horn for rotational motion. The threaded rod could not be welded directly to the horn which gave an idea of using Velcro. The newest idea in which the mechanical team will use is a clamping of the horns with a threaded rod welded to the clamp. Below in Figure 15 shows a 3D model of the old Velcro attachment idea and the new clamping attachment idea.

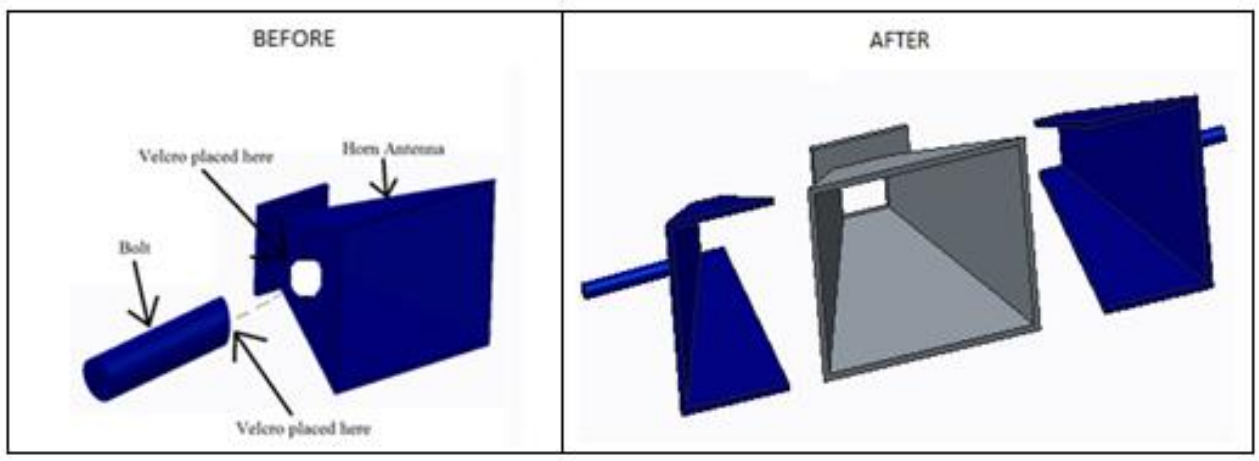


Figure 15: Before and After of Holding Horns

3.3.1.2 Component Box

The component box to hold the electrical components had to be readjusted because of addition parts added/removed from the block diagram. Below in Figure 16 shows the old box compared to the new box

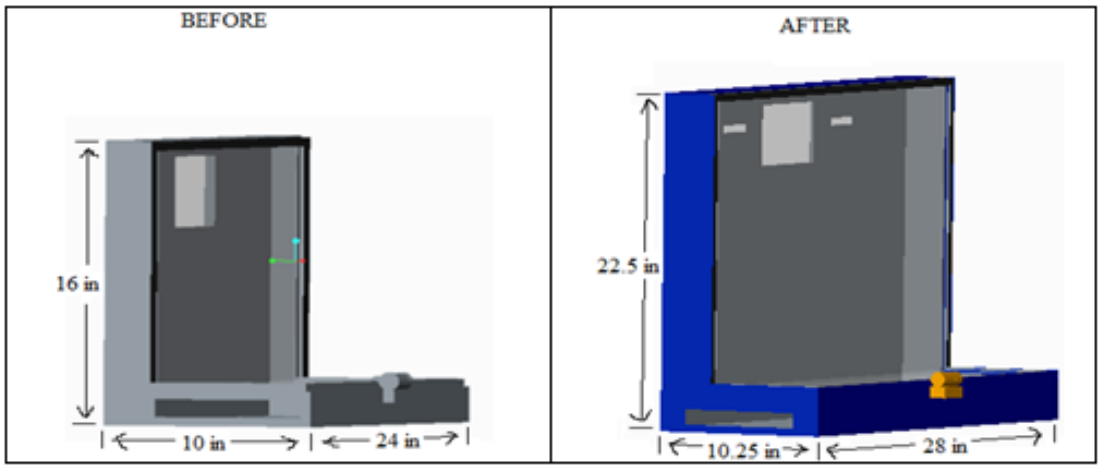


Figure 16: Electrical Component Box Before and After Changes

Figure 17 below shows the modification of the structure stand from a before and after depiction. The legs have been extended around the perimeter of the stand and reduced the thickness from 2 inch to 3/16th of an inch. The legs around the perimeter will help to support the weight of the structure allowing us to reduce the thickness of the metal.

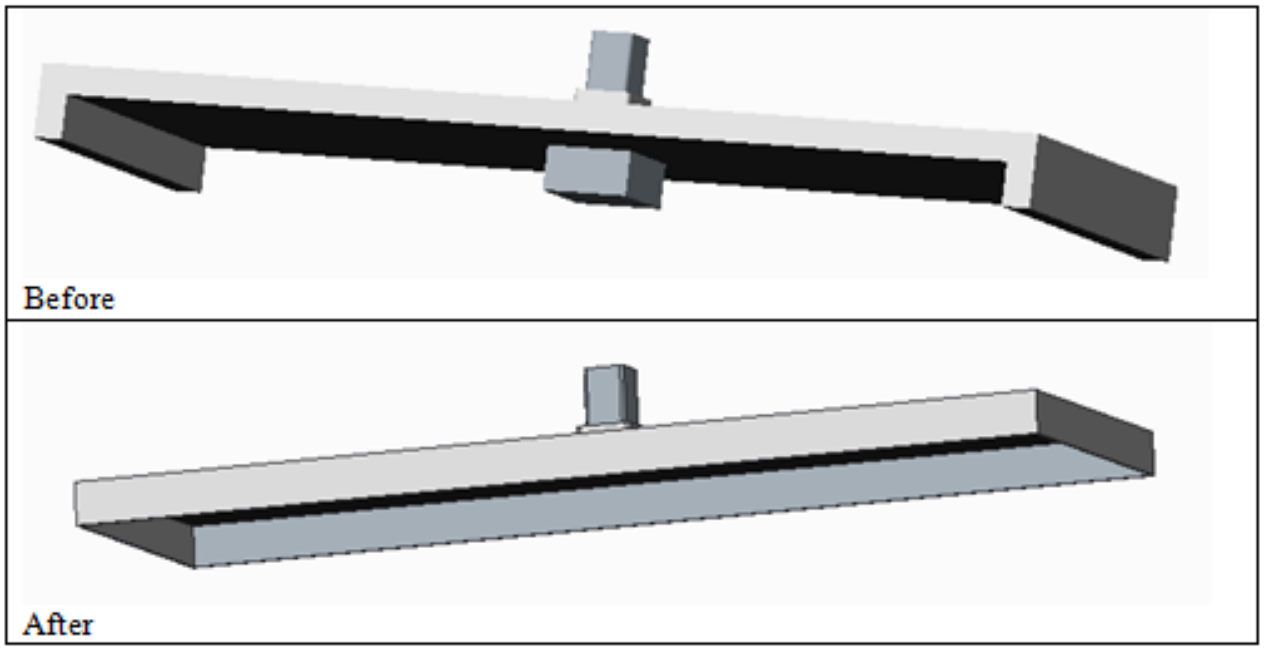


Figure 17: Modification of Structure Stand Used to Hold the Structure Upright

3.3.1.3 Trihedral

The Trihedral, commonly known as a corner reflector, has been fabricated with three equilateral triangle planes. The initial material will be aluminum. If needed, aluminum will be placed on the interior of the triangle for stronger reflection. These planes are joined together to form a triangular pocket to receive and reflect waves, this is reflected in Figure 18. Two trihedral will be used to calibrate the waves sent from the Synthetic Aperture Radar. By placing the trihedral

in the x and y axial locations, hot spots can be found to determine the maximum strength location of the SAR imager. The process is to place the trihedral on the target control point and orient it toward the SAR imager. The trihedral will be stood upright using a tripod for latitude adjustment. This will allow for a nice contrast response in the image of the control point.

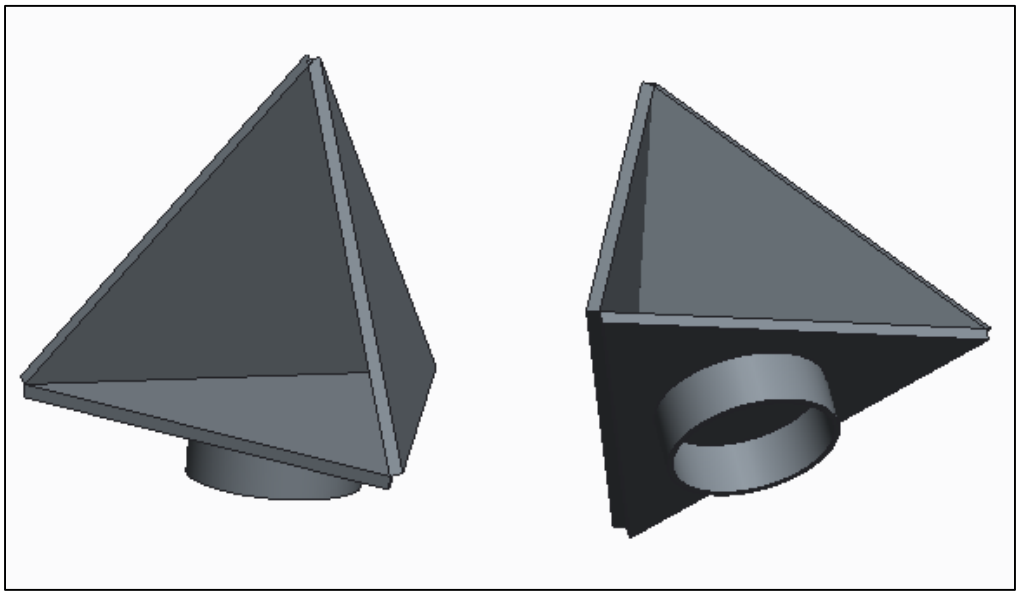


Figure 18: Trihedral assembly used to calibrate radio waves

3.3.2 Stress Analysis

Before each component of the structure is analyzed, it is essential that a visual of the whole structure is displayed for reference. Figure 19 is a reference visual for each component listed in the stress analysis section. Following the reference is Table 13 showing the actual weight of each component.

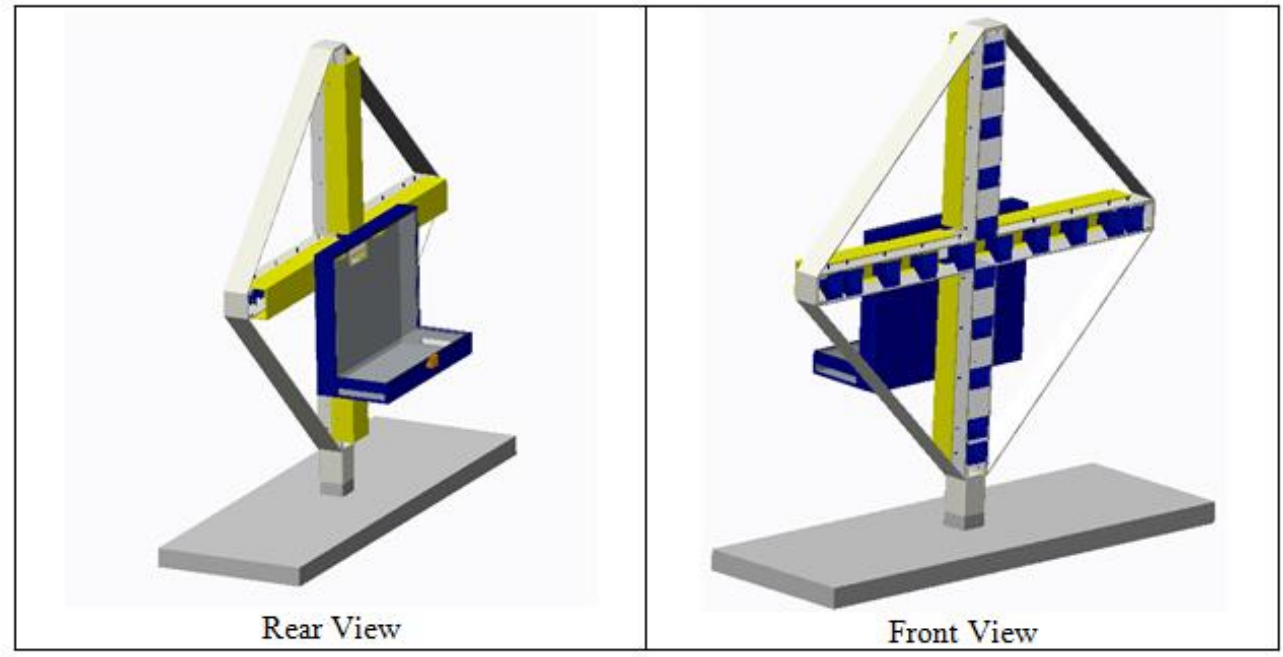


Figure 19: Synthetic Aperture Radar Structure

Table 13: Weight Distribution for Each Component of the SAR Imager Structure

Component	Weight	units
Component Box	33.3	lb
Quadrant Panel	9.9	lb
Quadrant Connector	1.3	lb
Quadrant Connector to Stand	4.7	lb
Vertical Horn Cover (Top and bottom)	7.9	lb
Horizontal Horn Cover(Left)	8.0	lb
Horizontal Horn Cover (Right)	8.0	lb
Structure Stand	48.2	lb
Total	129.3	lb

3.3.2.1 Components

3.3.2.1.1 Horn Cover (Left & Right)

Figure 20 displays the stress analysis through displacement. There will be two horn covers supplying support for the component box. This will be done with two slot inserts cutting the weight of the component box in half. Both slot inserts will be holding approximately a maximum of 20 lbs. The visual in the figure is an over exaggerated depiction of the displacement at the maximum weight. The maximum displacement of deformation at maximum load is 8.8 x 10^{-6} in. This displacement has no effect on the material, proving the Aluminum 6061 is a valid choice for our structure.

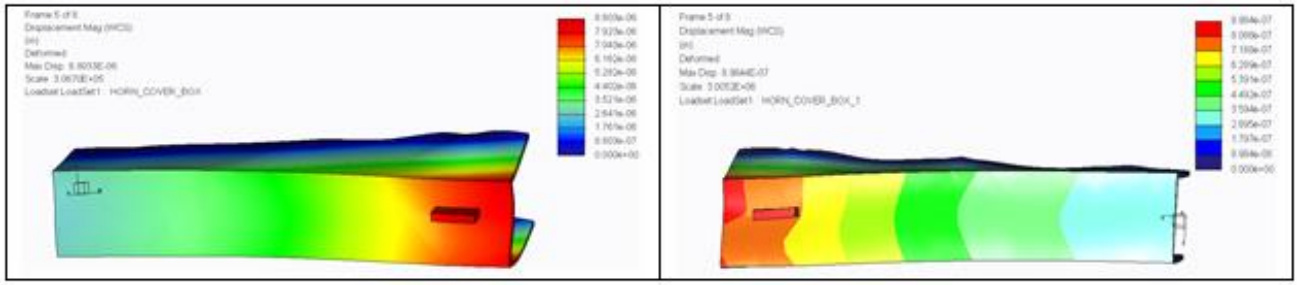


Figure 20. Horn cover for both left and right horizontal horn alignment.

3.3.2.1.2 Quadrant Panel (Quadrant 1 & 2)

The stress analysis associated with Figure 21 is the quadrant panel for quadrant one and two. These are the two quadrants located above the centerline of the structure. The displacement in the figure is for quadrant 1, but because the weight distribution is symmetrical to one another, the displacement will be the same for both quadrants. The maximum deformation displacement on these quadrant panels will be 1.0 x 10^{-6} in at maximum load. The largest load quadrant panel

one and two will be holding is approximately 27.5 lbs. As said before, both quadrants will evenly distribute the weight of approximately 56 lbs.

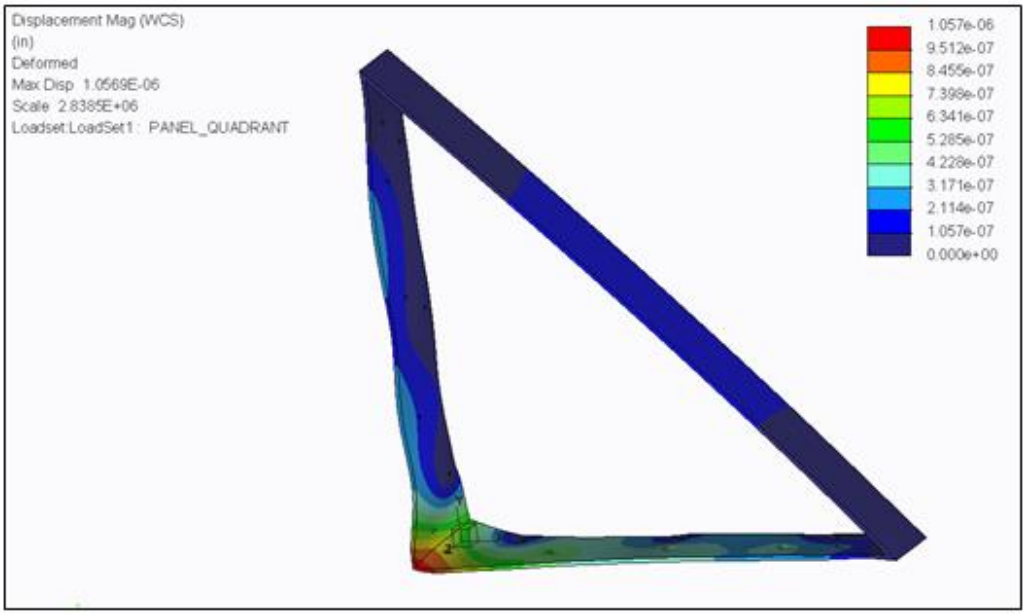


Figure 21. Stress Analysis of Quadrant 1 and 2 Quadrant Panels.

3.3.2.1.3 Quadrant Panel (Quadrant 3 & 4)

Quadrant Panel three and four are located below the centerline of the structure. These panels will support the weight of the component box and the two quadrant panels above them. The load is now pulling down on the quadrant panel, rather than pushing down. The horn cover is bolted to the bottom of the quadrant panel creating a pulling force on the panel. In this case, the maximum displacement is 3.0 x 10^{-7} in. This displacement is recorded at the maximum load. Figure 22 has specific detail to display the displacement of the material. The Panel will not be deformed from the applied load expected.

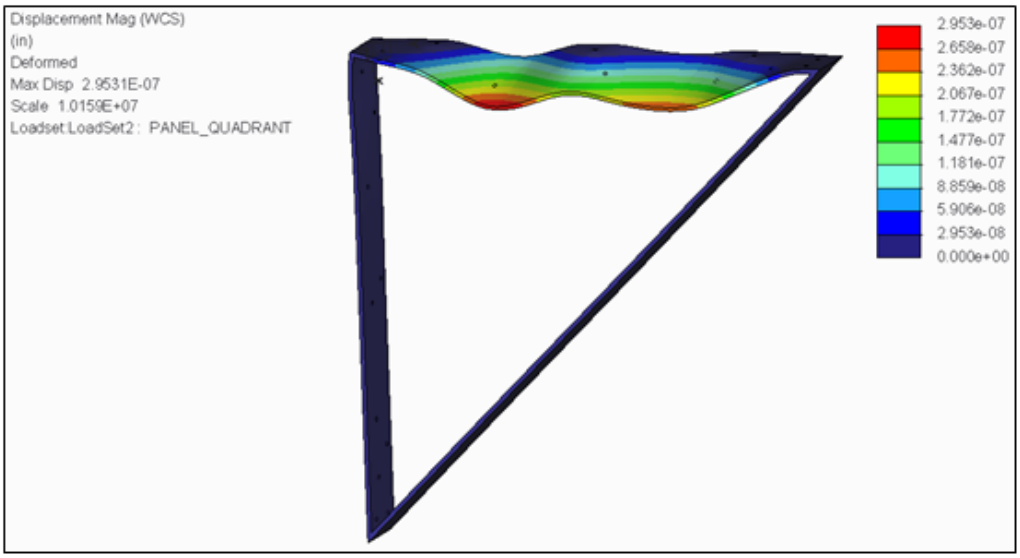


Figure 22. Stress Analysis of Both Quadrant 3 and 4 Quadrant Panels.

3.3.2.1.4 Connector Channel (Structure to Stand)

The connector channel, Figure 23, is the female component to the structure stand. This component will hold the weight of the whole structure including the four quadrant panels and component box. The connector component will be made of thick metal that will support the weight of the entire structure. After stress analysis, the maximum displacement is 8.1 x 10^{-7} in. The maximum load of the structure is roughly 75 lbs. This custom component was designed specifically to withstand the weight of the structure.

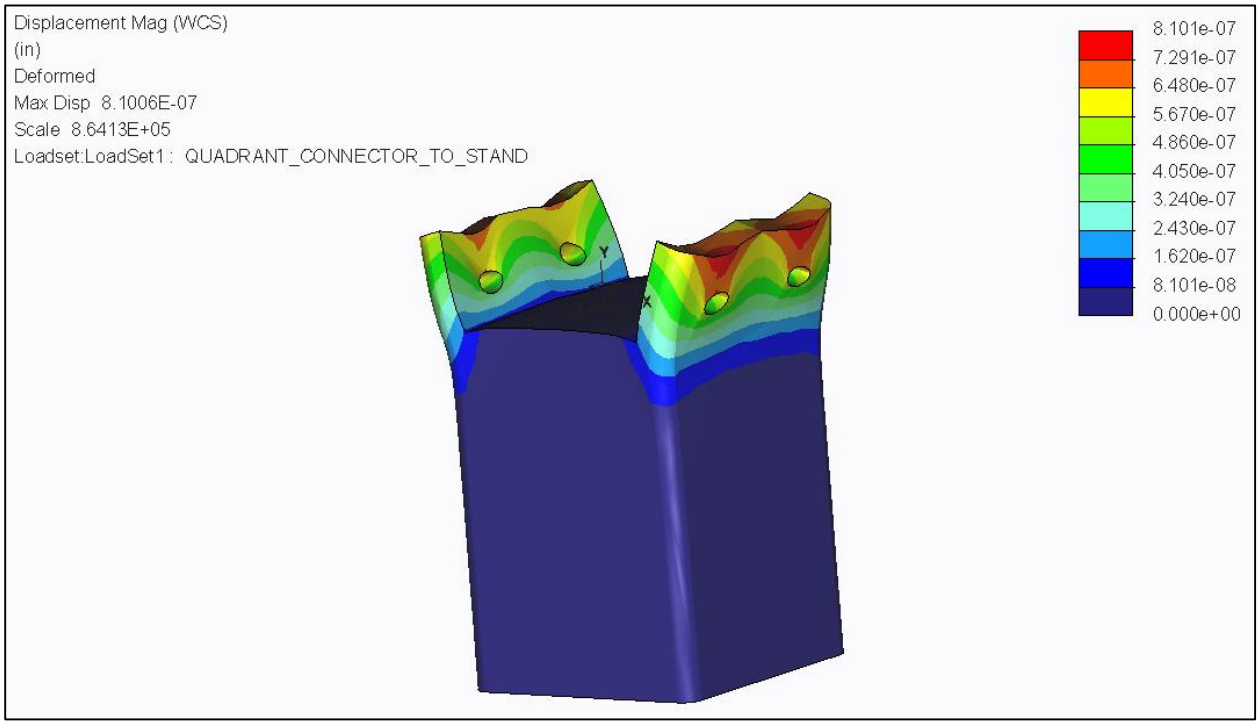


Figure 23. Stress Analysis of C-channel Connecting Structure to Structure Stand.

3.3.2.1.5 Structure Stand

The structure stand below is again shown at an exaggerated state. Due to the moment the structure causes on the stand, the male component to the connector channel will receive a bending force. From analysis, shown in Figure 24, the maximum displacement is 5.5 x 10^{-5} in. This will cause negligible deflection in the component. The Structure stand itself will withstand the weight of the structure as well. The maximum displacement at the male components is zero inches. The modification of the stand deems suitable to hold the structure.

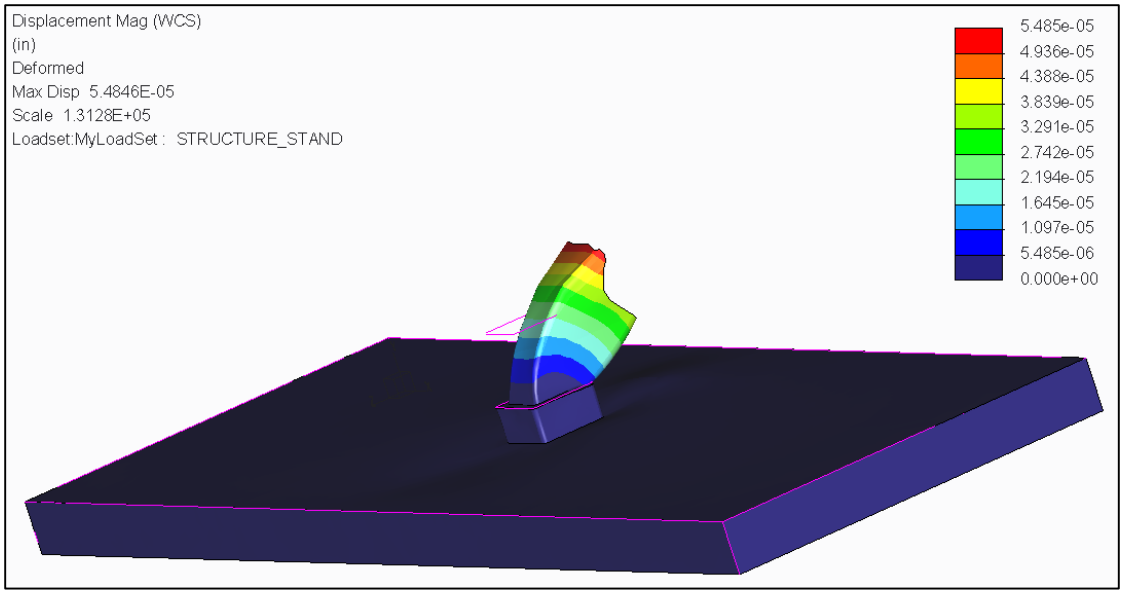


Figure 24. Stress Analysis on Structure Stand Holding the Entire Structure.

3.3.3 Heat Dissipation Analysis

3.3.3.1 Electrical Component Placement

The Electrical components will be placed inside the components box which will be attached to the antenna structure. The components will be placed onto an L-shaped sheet of aluminum metal. The FPGA, Power Supply, and Level Shift Circuit will be placed on the horizontal while the remaining components will be placed on the vertical of the L-shape sheet. A simple 3D model of the components on the sheet can be seen in Figure 25 below along with the cables excluding the USB, VGA, Power, and switch to horn cables/wires. The figure also includes dimensions of the L-shape sheet.

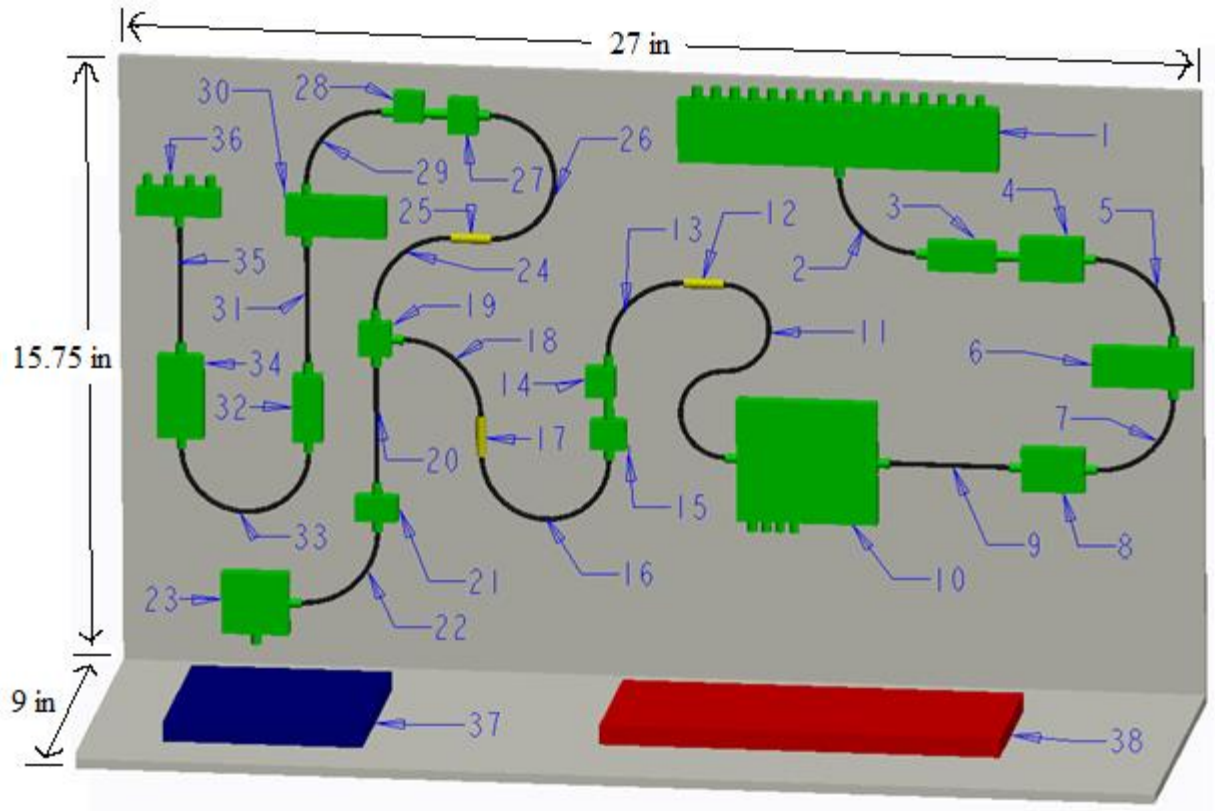


Figure 25. Electrical Components on L-shaped Sheet.

The following list corresponds with the numbers in Figure 25 above.

1 - SP16T Switch
2 - 3 Inch 90 Degree Bend Cable
3 - Band Pass Filter
4 - Low Noise Amplifier
5 - 3 Inch 90 Degree Bend Cable
6 - Variable Attenuator
7 - 3 Inch 90 Degree Bend Cable
8 - Low Noise Amplifier
9 - 3 Inch Cable
10 - IQ Demodulator
11 - 7 Inch S Bend Cable
12 - Fixed Attenuator
13 - 3 Inch 90 Degree Bend Cable
14 - Ultra Wide Band Amplifier
15 - Multiplier
16 - 5 Inch 180 Degree Bend Cable
17 - Fixed Attenuator
18 - 3 Inch 90 Degree Bend Cable
19 - SP2T Switch
20 - 3 Inch Cable
21 – Super Ultra Wide Band Amplifier
22 - 3 Inch 90 Degree Bend Cable
23 - VCO
24 - 3 Inch 90 Degree Bend Cable
25 - Fixed Attenuator
26 - 5 Inch 180 Degree Bend Cable
27 - Multiplier
28 - Ultra Wide Band Amplifier
29 - 3 Inch 90 Degree Bend Cable
30 - Variable Attenuator
31 - 3 Inch Cable
32 - Band Pass Filter
33 - 5 Inch 180 Degree Bend Cable
34 - Power Amplifier
35 - 3 Inch Cable
36 - SP4T Switch
37 - FPGA
38 – Power Supply/Level Shift Circuit

3.3.3.2 Heat Transfer from Electrical Components

For calculating the heat transfer of the components the box will be treated as a completely closed electrical component box. The first step in finding the temperature rise inside the box was to determine the inside surface area of the box which was calculated to be 12.76 ft^2. The power going into the box was found by totaling the power supplied to each component which was calculated to be 34.8 W. Dividing the total power by the total surface area gives the heat flux inside the box which was calculated to be 2.7 W/ft^2. By using the graph in Figure 26 below the temperature rise inside the box was determined to be approximately 13.5 ± 2.8 ^oC. The error was found by taking 25% of the calculated temperature rise which was suggested from a PENTAIR data sheet [2].

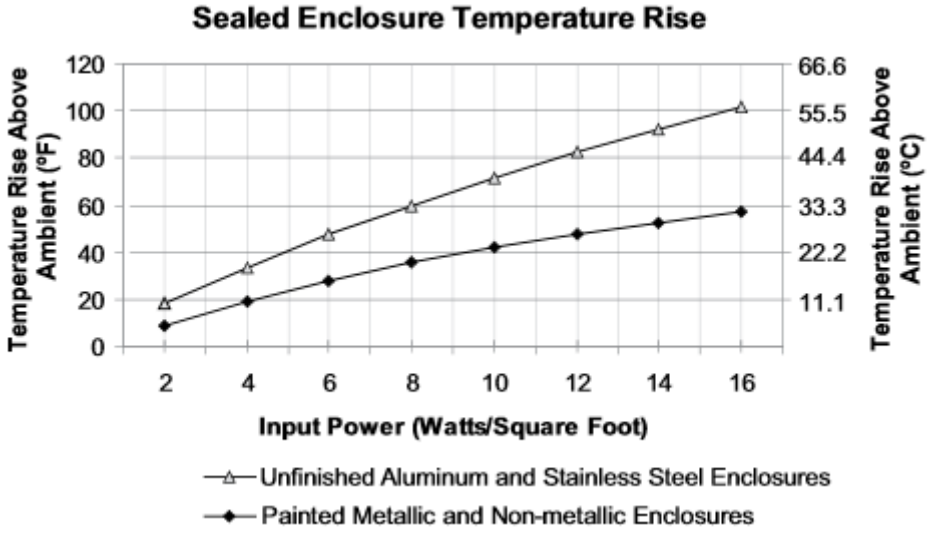


Figure 26. Sealed Enclosure Temperature Rise.

The above calculation was for an average temperature inside the box. The super ultra wide band, ultra wide band, low noise, and power amplifier dissipate the most heat inside the box creating hotter spots. Below in Table 14 shows the heat transfer of each electrical component.

Table 14: Heat Transfer of Each Electrical Component.

Component	Area (ft^2)	Voltage (V)	Current (A)	Dissipated Power (W)	Heat Transfer (W/ft^2)
VCO	0.174	3.300	0.045	0.149	0.855
FPGA	0.278	3.300	0.200	0.660	2.376
SPDT	0.005	5.000	0.001	0.007	1.400
SP4T	0.010	5.000	0.160	0.800	78.367
SP16T	0.089	5.000	0.550	2.750	30.938
IQ DEMOD	0.075	5.000	0.110	0.550	7.300
SUPER ULTRA WBA	0.005	12.000	0.400	4.800	897.662
ULTRA WBA	0.005	12.000	0.400	4.800	1031.642

LOW NOISE AMP	0.012	12.000	0.320	3.840	321.488
POWER AMP	0.017	15.000	1.100	16.500	981.818
Total	X	X	X	**34.856**	**3353.846**

From Table 14 above the amplifiers dissipate the most heat. A heat sink was ordered with the super ultra wide band amplifier to ensure proper cooling. The ultra wide band, low noise, and power amplifiers can be cooled by a heat exchanger which is TBD. A fan (also TBD) will be placed on each side of the vertical portion of the component box to draw heat out the box and wiring will be integrated into the power supply. Note that the power supply itself was not calculated into the above analysis which will be at a later date.

3.4 Power System Design

The power supply board will contain the circuitry to provide power to all of the components that need power. The board itself will be powered by nine DC power supply inputs. Each of these supply inputs will provide power to the linear voltage regulators used in the design. See appendices for the data sheet as well as the schematics for all circuits and components.

Major risks for the power supply board include:

- Insufficient Power:
  - Consequences:
    - The needed output voltages and currents will not be supplied or may not be large enough to meet the needs of the components
  - Mitigation Strategy:
    - Ensure that the components will operate within its limits specified by the data sheet (input/output voltage, current)

Table 15: Voltage Regulators

QTY	Part Name	Voltage Regulator Used
1	VCO	LP38690_3P0
1	FPGA Board	LP38690_3P0
1	SPDT Switch	LM2940-N_5P0
1	SP4T Switch	LM2940-N_5P0
1	SP4T Switch	TPS7A3301
1	SP16T Switch(V+)	LM2940-N_5P0
1	SP16T Switch(V-)	TPS7A3301
1	IQ Demodulator(V+)	LM2940-N_5P0
1	IQ Demodulator(V-)	TPS7A3301
1	Super Ultra Wideband Amplifier	LM2940-N_12P0

2	Ultra Wide Bandwidth Amplifier	LM2940-N_12P0
1	Low Noise Amplifier SLNA-120-38-22-SMA	LM2940-N_12P0
1	Low Noise Amplifier SLNA-180-38-25-SMA	LM2940-N_12P0
1	Power Amplifier	TPS7A4501
2	Level Shift Supply	TPS7A4501

3.4.1 +3.3Vdc Supply

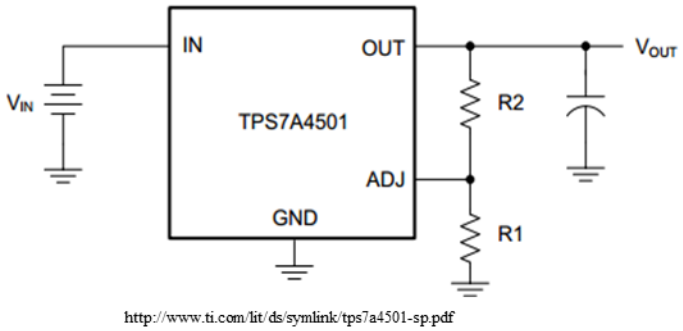
There are two components that require an input voltage of +3.3Vdc, the VCO and the FPGA board. The VCO is required to have a supply current of 45 mA and the FPGA board is required to have 200 mAdc. Supplying these required inputs will be supplied using a 3.3Vdc fixed output linear voltage regulator (LP38690_3P3). This voltage regulator will be supplied by a 10Vdc supply line.

3.4.2 +3.5Vdc Supply

There are two components that require an input voltage of +3.5Vdc, the comparators in the level shift circuits. The part number for the comparators is MAX941. The required supply voltage will be provided using an adjustable output linear voltage regulator (TPS7A4501). These regulators allow for the output voltage to be set using a resistor divider network. To obtain the desired output R1 = 2kΩ and R2 = 1.06kΩ. These regulators will be powered by a 10Vdc supply line.

$$Vout\ (Vdc) = 1.21Vdc\left(1 + \frac{R2}{R1}\right) + Iadj * R2 \text{ (Iadj = 3uAdc @ 25ºC)}$$

Equation 18: TPS7A4501 Output Voltage



http://www.ti.com/lit/ds/symlink/tps7a4501-sp.pdf

Figure 27: TPS7A4501 Circuit

3.4.3 +5Vdc Supply

There are four components that require an input of +5Vdc the SPDT, SP4T, SP16T switches and the IQ demodulator. The fixed output liner voltage regulator that provides the input voltage for these components is (LM2940-N_5P0). It an input from a 10Vdc supply line.

3.4.4 +12Vdc Supply

There are four components that require an input of +12Vdc the super ultra wideband amplifier, the ultra wide bandwidth amplifier, and both of the low noise amplifiers. The fixed value linear regulators that will provide the necessary voltages for these components are LM2940-N_12P0. The all operate from a 15Vdc supply line.

3.4.5 +15Vdc Supply

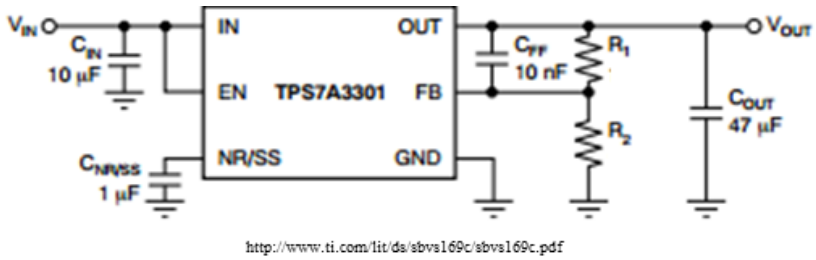
The +15Vdc supply is needed for the power amplifier. The linear voltage regulator used to supply this power is the TPS7A3301. It is the same as the voltage regulator used to supply the +3.5Vdc to the comparators in the level shift circuit. To obtain the desired output R1 = 5.7kΩ and R2 = 500Ω. This regulator will be powered by a 20Vdc supply line.

3.4.6 -5Vdc Supply

The -5Vdc supplies are needed for the SP4T switch and the IQ demodulator. The linear voltage regulator used to supply this power is the TPS7A4501. To obtain the desired output R1 = 5.7kΩ and R2 = 500Ω. This regulator will be powered by a -25Vdc supply line.

$$Vout\ (Vdc) = 1.21Vdc\left(1 + \frac{R2}{R1}\right) + Iadj * R2 \text{ (Iadj = 3uAdc @ 25ºC)}$$

Equation 19: TPS7A4501 Output Voltage



http://www.ti.com/lit/ds/sbvs169c/sbvs169c.pdf

Figure 28: TPS7A3301 Circuit

3.4.7 -12Vdc Supply

The -12Vdc supply is needed for the SP16T switch. The linear voltage regulator used to supply this power is the TPS7A4501. To obtain the desired output R1 = 9.2kΩ and R2 = 1kΩ. This regulator will be powered by a -25Vdc supply line.

3.5 Software Design

This section will describe the code that will be used to control the timing of the switches, the changing from binary to binary coded decimal for the A/D converter, and the 7 segment display of the voltages from the A/D converters for the SAR Imager. The code will be explained thoroughly, although this is just a rough draft of what will actually be implemented in the final design. The final design will have extra elements added to it (such as switches, pins used when testing), and will be in much greater detail. Note that the FPGA has a 100 MHz clock, which is a 10 ns period (5 ns on, 5 ns off). The description of the code will be separated by explaining the different inputs of the FPGA, outputs of the FPGA, and the buffers used as well for the FPGA. Reference code can be seen in Appendix 10.11.

3.5.1 Inputs, Buffers, and Outputs

3.5.1.1 Inputs

The inputs of the FPGA are clk, rst, B, and C. Clk is just the inherent 100 MHz clk of the FPGA and is labeled as pin V10 from the reference sheet. Rst is just the signal used for when rst='1', then all of the signals of the FPGA are just logic 0. B is the output from the first A/D converter (the A/D converter with the real voltage from the IQ demodulator) and C is the output from the second A/D converter (the A/D converter with the imaginary voltage from the IQ demodulator).

3.5.1.2 Buffers

The buffers for the clock division of the clock on the FPGA are clk_div_by2, clk_div_by4, clk_div_by8, clk_div_by16, clk_div_by32, clk_div_by64, and clk_div_by128. These are simply the results of the clock dividers used to make signals with longer periods. This will be explained below and as well as the reasoning behind this. The other buffers on the FPGA are P, dec_place, and Q. These buffers are used for displaying the digital voltage on the 7 segment display, and are explained thoroughly later.

3.5.1.3 Outputs

The outputs of the FPGA are pulse, spdt, sp4t, sp16t, seg_7_display_whole, seg_7_display_dec_place, and seg_display_decimal. As of right now, these will be the signals that are the outputs of the FPGA. They are thoroughly described below:

3.5.1.3.1 SPDT

The output spdt is of type std_logic (although it could have also just been a bit value as well) and needs only a logic 1 or a logic 0 as the output. This is because the SPDT switch is considered on when it has a logic 1 (transmit mode) and off when it has a logic 0 (receive mode).

3.5.1.3.2 SP4T

The output sp4t is of type std_logic(0 TO 3). This is because this signal has to control four different transmit antennas, with each bit controlling only one transmit antenna. When a bit is logic 1, that means that the signal will be transmitting from the antenna that has that bit controlled by it. Note that for this project, only one transmit antenna will be on at one time, so at most only one bit can be logic 1 at one time.

3.5.1.3.3 SP16T

The output sp16t is of type std_logic(0 TO 15). This is because this signal has to control sixteen different receive antennas, with each bit controlling only one receive antenna. When a bit is logic 1, that means that the signal will be receiving from the antenna that has that bit controlled by it. Note that for this project, only one receive antenna will be on at one time, so at most only one bit can be logic 1 at one time.

3.5.1.3.4 PULSE

The output pulse is of type std_logic (although it could have also just been a bit value as well) and needs only a logic 1 or a logic 0 as the output. This is because the signal transmitting from the selected transmit antenna just needs to be logic 1 when it is transmitting from the antenna and logic 0 when the system is in receive mode. Note that the pulse output just controls the actual output of the signal from the transmit antenna, while the sp4t output controls which antenna is actually emitting the signal.

3.5.1.3.5 7 SEGMENT DISPLAY

The outputs seg_7_display_whole, seg_7_display_dec_place, and seg_display_decimal are of type std_logic(0 to 6). This is because even though the the A/D converter has a 12 bit output, the output on the seven segment display is a combination of 7 bits, and will be read in the form of a binary coded decimal. More detail is given in the section explaining the Hexadecimal display code.

3.5.2 Code for Timing Explanation:

The signals used in the FPGA for the timing are as follows: clk_div, clk_div2, clk_div4, 8, clk_div16, clk_div32, clk_div64, and blink. clk_div, clk_div2, clk_div4, 8, clk_div16, clk_div32, and clk_div64 are the signals used for the processes that divide the clocks. Blink is the signal that is used to assign the timing to the pulse (20 ns on, 140 ns off). Recall that the timing for the pulse is the same for the timing for the spdt output and sp4t output. This is because again the timing for all the signals in transmit mode is the same. The steps of the code for the timing of the switches and the reasoning behind it are shown below:

3.5.2.1 Clock Division

Since a 20 ns pulse of logic 1 is needed for the timing, the way this was done was by making a clock divider of the 10 ns clock inherent to the FPGA (which was called clk in the code below). Note that clk which has a period of 10 ns has its period being 5 ns on, 5 ns off. A Clock divider was then used for clk, which was the divide_by_2 process. This had rst and clk being in the sensitivity for the process which means that any changes in the process rely on these two signals. The signal used for assigning information in the divide_by_2: process was clk_div. The description of the clock divider is as follows:

3.5.2.2 Algorithm for code of Clock Division

If the rst is logic 1, the signal clk_div is going to be logic 0 since the point of rst is to have all signals logic 0 when rst is logic 1. Now for all other cases with rst (which would mean when rst is logic 0), then when the input clk of period 10 ns has a rising edge (clk has transitioned from logic 0 to logic 1), the output of clk_div will be the opposite of its current value. Since clk_div is only updated on the rising edge of the clk input signal, the output from clk_div will be half the frequency of the clk input. This will create a divide by 2 effect. The divide by two effect of the divide_by_2 process will have the signal clk_div having the divide by 2 effect. This yields the clk_div to have a period of 20 ns (10 ns on. 10 ns off). By having clk_div being assigned to the buffer clk_div_by_2, the period of clk_div_by_2 has a period of 10 ns just like clk_div.

3.5.2.2.1 Divide by 4 process

The same algorithm was used for the divide_by_4 process, with the exception of the sensitivity list consisting of rst and clk_div. This means that the new period of clk_div was divided, with the signal clk_div2 being used as the assignment of information in the divide_by_4 process. This yields the clk_div2 to have a period of 40 ns (20 ns on, 20 ns off). By having clk_div being assigned to the buffer clk_div_by4, the period of clk_div_by4 has a period of 20 ns just like clk_div2.

3.5.2.2.2 Divide by 8 process

The same algorithm was used for the divide_by_8 process, with the exception of the sensitivity list consisting of rst and clk_div2. This means that the new period of clk_div2 was divided, with the signal clk_div4 being used as the assignment of information in the divide_by_8 process. This yields the clk_div4 to have a period of 80 ns (40 ns on, 40 ns off). By having clk_div2 being assigned to the buffer clk_div_by8, the period of clk_div_by48has a period of 80 ns just like clk_div4.

3.5.2.2.3 Divide by 16 process

The same algorithm was used for the divide_by_16 process, with the exception of the sensitivity list consisting of rst and clk_div4. This means that the new period of clk_div4 was divided, with the signal clk_div8 being used as the assignment of information in the divide_by_8 process. This yields the clk_div8 to have a period of 160 ns (80 ns on, 80 ns off). By having clk_div8 being assigned to the buffer clk_div_by16, the period of clk_div_by16 has a period of 80 ns just like clk_div2.

3.5.2.2.4 Divide by 32 process

The same algorithm was used for the divide_by_32 process, with the exception of the sensitivity list consisting of rst and clk_div8. This means that the new period of clk_div8 was divided, with the signal clk_div16 being used as the assignment of information in the divide_by_32process. This yields the clk_div 16 to have a period of 320 ns (160 ns on, 160 ns off). By having clk_div16 being assigned to the buffer clk_div_by32, the period of clk_div_by32 has a period of 320 ns just like clk_div16.

3.5.2.2.5 Divide by 64 process

The same algorithm was used for the divide_by_64 process, with the exception of the sensitivity list consisting of rst and clk_div16. This means that the new period of clk_div16 was divided, with the signal clk_div32 being used as the assignment of information in the divide_by_64process. This yields the clk_div 32 to have a period of 640 ns (320 ns on, 320 ns off). By having clk_div32 being assigned to the buffer clk_div_by64, the period of clk_div_by64 has a period of 640 ns just like clk_div32.

3.5.2.2.6 Divide by 128 process

The same algorithm was used for the divide_by_128 process, with the exception of the sensitivity list consisting of rst and clk_div32. This means that the new period of clk_div32 was divided, with the signal clk_div64 being used as the assignment of information in the divide_by_128process. This yields the clk_div64 to have a period of 1280 ns (640 ns on, 640 ns off). By having clk_div64 being assigned to the buffer clk_div_by128, the period of clk_div_by128 has a period of 1280 ns just like clk_div64.

3.5.2.3 Assignment of Signals to Get Timing

The main reason why all of the outputs of the clock dividers have the data type buffer was because VHDL does not allow you to use outputs as inputs for the FPGA. The results of the clock dividers were used as either inputs for clock dividers, or for combinational logic that was used to get the actual timing of the switches.

3.5.2.3.1 Transmit Path Timing

For the transmit path process, the buff_pulse buffer is used as the sensitivity of the process, since all the assignments for the sp4t signal rely on buff_pulse. The outputs for sp4t(0), sp4t(1), sp4t(2), and sp4t(3) are just logical combinations of the buffers assigned periods.

3.5.2.3.2 Receive Path Timing

For the receive path process, the clk_div_by8 buffer is used as the sensitivity of the process, since all the assignments for the sp4t signal rely on clk_div_by8. The outputs for sp16t(0), sp16t(1), sp16t(2), sp16t(3), sp15t(4), sp15(5), sp16t(6), sp16t(7), sp16t(8), sp16t(9), sp16t(10), sp16t(11), sp16t(12), sp16t(13), sp16t(14), and sp16t(15) are just logical combinations of the buffers assigned periods.

3.5.3 A/D Code

The next portion of code that is to be completed and tested is the A/D code. This code will get an analog voltage value and put it in terms of a binary value onto the FPGA. This will be done in the form of a binary to BCD (binary coded decimal) conversion. There are several things to note for this next task. The first is that the Digilent distributor has sample code for actually changing the analog signal and changing it into a binary value for the PMOD A/D converter. More will be looked into this for future design, since this was not in VHDL. The second thing to note is that the logic of the code for the conversion of the output of the A/D converter (which is a 12 bit value) to a form that can be stored and worked on (binary coded decimal) is provided in the appendix. For the next milestone, the A/D will hopefully be able to return two values, a real and

imaginary voltage from the two A/D converters. Doing this will allow for accurate troubleshooting of the received values in the 7 segment display of the FPGA board.

A subtask of this is having the FPGA display the analog voltage value from the shift level circuit (and before that the IQ demodulator). This will be done using a 7 segment display. The code below shows the type of logic that the assignments of the display would use, with the two different cases being for the real and imaginary voltages from the two A/D converters. Recall that the voltage from the A/D converter can only be output from 0 to 3.3 V. The A/D converter has a 12 bit output value, which is why there are 12 bits in the bits that will affect the 7 segment display and output numbers from 0 to 9. The dec_place signal used as the sensitivity for the Dec_place_v is what will be acting as the decimal place in the display of the voltages. This will just be an underscore, and note that in all cases this underscore will remain on. In actual practicality of the system, a switch will be used to control whether the output to the 7 segment display is the real voltage or the imaginary voltage from the A/D converters. The real and imaginary voltages will be displayed one at time, since there are only four 7 segment displays on the FPGA.

3.5.3.1 Binary to BCD conversion

The explanation of the binary to binary coded decimal conversion is explained below:

For this portion of the code, the shift and Add-3 algorithm was used for an n-bit signal. It goes as follows:

1. Shift the binary number left one bit.
2. If n shifts have taken place, the binary coded decimal number not in the binary column anymore and the algorithm is finished. If this has not happened, go to step 3.
3. If the binary values in any of the binary coded decimal columns is 5 or greater, the value in that column must be added by 3.
4. Go back to Step 1 and repeat.

Below in Table 16 the steps for the algorithm taken to get this binary coded decimal number from the FPGA is illustrated.

Table 16: Logic of Conversion

Binary coded Decimal columns					
Operation	Thousands	Hundreds	Tens	Units	Binary
B					1111 1111 1111
HEX					1111 1111 1111
Start					1111 1111 1111

Shift 1				1	1111 1111 111
Shift 2				11	1111 1111 11
Shift 3				111	1111 1111 1
Add 3				1010	1111 1111 1
Shift 4			1	0101	1111 1111
Add 3			1	1000	1111 1111
Shift 5			11	0001	1111 111
Shift 6			110	0011	1111 11
Add 3			1001	0011	1111 11
Shift 7		1	0010	0111	1111 1
Add 3		1	0010	1010	1111 1
Shift 8		10	0101	0101	1111
Add 3		10	1000	1000	1111
Shift 9		101	0001	0001	111
Add 3		1000	0001	0001	111
Shift 10	1	0000	0010	0011	11
Shift 11	10	0000	0100	0111	1
Add 3	10	0000	0100	1010	1
Shift 12	100	0000	1001	0101	
BCD	4	0	9	5	
P	15 12	11 8	7 4	3 0	
z	27 24	23 20	19 16	15 12	11 0
Vectors	Thousands = P[14:12]=z[26:24]	Hundreds= P[11:12]=z[26:24]	Tens= P[7:4]=z[19:16]	Units= P[3:0]=z[15:12]	

3.5.3.2 Explanation of Binary to BCD Code

Recall in the above figure (the figure which shows the declarations of all of the inputs, outputs, and buffers), that there was an input B which had an input type of std_logic_vector (11 DOWNTO 0). This input B is just the 12 bit output from the A/D converter which goes into the FPGA. The logic for the code is explained as follows and can be checked by analyzing the chart showing the shifts of the binary values. Note that this is just an explanation of the code line by

line, and for the full image of the code it can be seen in the code in the appendix section. Another thing to note is that both conversions for the real and imaginary voltage follow the same logic.

1. The variable z is just the binary number which has been shifted from the above chart. Note that after the shifts there is 26 bits (the 14 that are shifted into the binary coded decimal column and the 12 bits that the original binary bits were from). The command below does this:

```
variable z: std_logic_vector (26 downto 0);
```

2. In the architecture begins with setting z to zero. This is to set the default value of the binary number. This is done for all bits of z, hence why it runs from 0 to 26. The commands below do this:

```
for i in 0 to 26 loop
   z(i) :='0';
end loop;
```

3. Note that the first 3 actions of the chart are to shift the binary values three times. In terms of z, the numbered bits after the first three bits are now 14 down to 0. Originally the first 12 bits are simply 11 down to 0, but by shifting the bits left 3 times when z is a variable ranging from 0 to 26, the new values of z after the shift are bits 14 down to 0. The command below does this:

```
z(14 downto 3) :=B;
```

4. For the next loop, this is ranged from 0 to 8 because since there are 12 shifts required for this 12 bit input binary value from the A/D converter, the first three shifts were already done from step 3. Since three shifts were already done, and for a 12 bit binary value that leaves 9 shifts left, hence the loop from 0 to 8 which gives 9 loops. Looking at the chart above, the total value of z has the units being bits 15 to 12. Using the fact that if a number is 5 or greater, then 3 is added to that column (in this case the bits 15 to 12 is the column in question). For the tens column, the bits are from 19 to 16, with the same logic that if a number is 5 or greater, then 3 is added to that column. For the hundreds column, the bits are from 23 to 20, with the same logic that if a number is 5 or greater, then 3 is added to that column. The loop will finish after step 5, and the commands for this process is shown below:

```
for i in 0 to 8 loop
   if z(15 downto 12) > 4 then
      z(15 downto 12) := z(15 downto 12) + 3;
   end if;

   if z(19 downto 16) > 4 then
      z(19 downto 16) := z(19 downto 16) + 3;
   end if;

   if z(23 downto 20) < 4 then
      z(23 downto 20) := z(23 downto 20) + 3;
   end if;
```

5. The value for z is then shifted left one bit to encompass the entire binary number after the previous two loops. This was done by letting z(12 DOWNTO 1) being the same as z(11 DOWNTO0). . The command for that is shown below, with the loop finishing as well (this was stated above in step 4):

```
z(26 downto 1) := z(25 downto 0);

end loop;
```

6. The answer will then be the final 13 binary values from z. This is highest enough to contain the highest value in binary for 12 bits, which is written in the chart as well (i.e.: 4095). With this step the conversion is finished, and the command for this step is shown below:

```
P <= z(26 downto 14);
```

3.5.3.3 7 Segment Display Code

The explanation of the 7 segment display code is below. This code is just the logic to show the assignments to what would be displayed on the 7 segment display. Note that for the actual implementation of the project, a switch on the FPGA board will be used to control whether the real voltage or imaginary voltage is displayed. This is because there are only four 7 segment displays.

3.5.3.3.1 Display of Real Voltage Explanation

The Real_num_v process is the process that controls the output of the 7 segment display. The sensitivity of the process is solely dependent on the binary coded decimal value from the A/D converter. Recall that the binary coded decimal value will be P, which is the sensitivity for the Real_num_v. When this binary value is zero, the output to the 7 segment display is zero. When the value of the binary coded decimal is 1, then the only values that will light up on the 7 segment display will be slot b and c. This same algorithm which is shown in the image below will be used for values 0-9. If any other value gets input into the process, then P the default display would be

that all of the 7 segments on the 7 segment display will light up. This would mean an error, although this was only done to have a default value for the seven segment display and this should not happen.

3.5.3.3.2 Display of Imaginary Voltage Explanation

The Imag_num_v process is the process that controls the output of the 7 segment display. The sensitivity of the process is solely dependent on the binary coded decimal value from the A/D converter. Recall that the binary coded decimal value will be Q, which is the sensitivity for the Imag_num_v. When this binary value is zero, the output to the 7 segment display is zero. When the value of the binary coded decimal is 1, then the only values that will light up on the 7 segment display will be slot b and c. This same algorithm which is shown in the image below will be used for values 0-9. If any other value gets input into the process, then P the default display would be that all of the 7 segments on the 7 segment display will light up. This would mean an error, although this was only done to have a default value for the seven segment display and this should not happen.

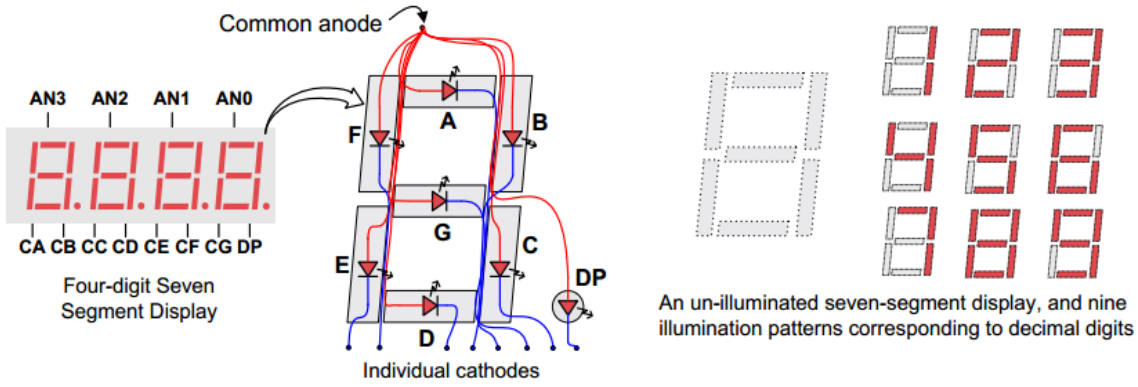


Figure 29 Schematic of the different segments on the 7 segment display and the combinations that will be used

3.6 Signal Processing Design

If the target was really close to the array of antennas, there would be a huge difference in the path length between the center of the array and the phase center that's off to the side. However, when going 20 feet away from the array, then the difference is manageable, so a target would be set up at boresite 20 feet away at the center of the array, which would be called a calibration target. And then each phase center and the I and Q voltages would be measured, which would then become the calibration factor. This calibration factor represents the error out in free space from the horn to the target. So the calibration at boresite was done in order to determine what the calibration factor would be when the target is at the center of the array of horns. The calculation of error at the maximum angle was done in order to determine how the calibration holds up when the scatter energy is brought in at different angles.

The range from the antennas to the target is 20 feet; however, for the calibration, the measurements will be done in inches, hence the range is 240 inches. The antenna separation, in lambda, is 6λ. One lambda at a frequency of 10 GHz is equal to 1.18 inches.

3.6.1 Boresite Calibration

As explained in the signal processing section, there are two transmit horns and eight receive horns, and sixteen phase centers from each transmit and receive antenna pair to the scene are created. In the following Figure 30, A is the first transmit horn and A_1 through A_8 are the receive horns, which in this case each one of them is pairing with transmit horn A. B at the bottom is the second transmit horn, and B_1 through B_8 going from bottom to top are pairing with transmit horn B.

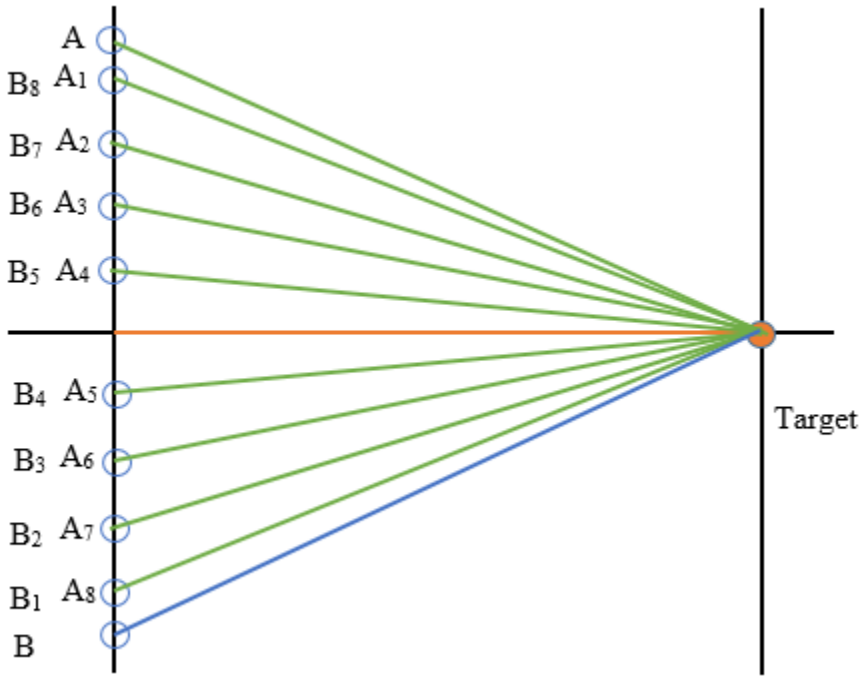


Figure 30. Transmit and Receive Horns with Target at Boresite

In Table 17, the distance relative to the center of the array is calculated in lambda. The distance for A_4, as well as for A_5, is calculated by dividing the antenna separation of 6λ by 2, as the center is halfway between antennas A_4 and A_5, which results in 3λ. Then the distance for A_3, as well as for A_6, is calculated by adding the result of A_4 to the antenna separation of 6λ, and the result is 9λ. These calculations continue in this trend for horns A_1, A_2, A_7, and A_8. For the transmit horn A, the distance relative to the center of the array is found by adding the result of A_1, which is 21λ to half of the antenna separation for a result of 24λ. The same process is applied to the transmit horn B along with the receive horns B_1 through B_8.

In order to calculate the distance relative to the center of the array in inches, the distances in lambda were simply multiplied by 1.18 inches, which is what one lambda is equal to. To find the distance to range when the target is not moved off at any angle, in which case θ = 0°, the Pythagorean Theorem is used as shown in Figure 31. If a is equal to the distance relative to the center of the array and r is the distance from the center to the target, then the relation for each horn would be $distance = \sqrt{a^2 + r^2}$. Then for horns A_1 through A_8, the sum of the transmit/receive path of each antenna was calculated by adding the calculated distance of horn A to each of these

receive horns. The same was done for transmit horn B and receive horns B_1 through B_8. This is essentially the boresite calibration.

Table 17. Boresite Calibration

BORESITE CALIBRATION				
	f = Distance Relative to Center of Array (λ)	**a = Distance Relative to Center of Array (inches)**	**Distance to Range from Each Antenna (θ=0°) (inches)**	**Sum of Tx and Rx Path of Each Antenna (inches)**
A	24	28.34645669	241.67	
A1	21	24.80314961	241.28	482.95
A2	15	17.71653543	240.65	482.32
A3	9	10.62992126	240.24	481.90
A4	3	3.543307087	240.03	481.69
A5	3	3.543307087	240.03	481.69
A6	9	10.62992126	240.24	481.90
A7	15	17.71653543	240.65	482.32
A8	21	24.80314961	241.28	482.95
B8	21	24.80314961	241.28	482.95
B7	15	17.71653543	240.65	482.32
B6	9	10.62992126	240.24	481.90
B5	3	3.543307087	240.03	481.69
B4	3	3.543307087	240.03	481.69
B3	9	10.62992126	240.24	481.90
B2	15	17.71653543	240.65	482.32
B1	21	24.80314961	241.28	482.95
B	24	28.34645669	241.67	

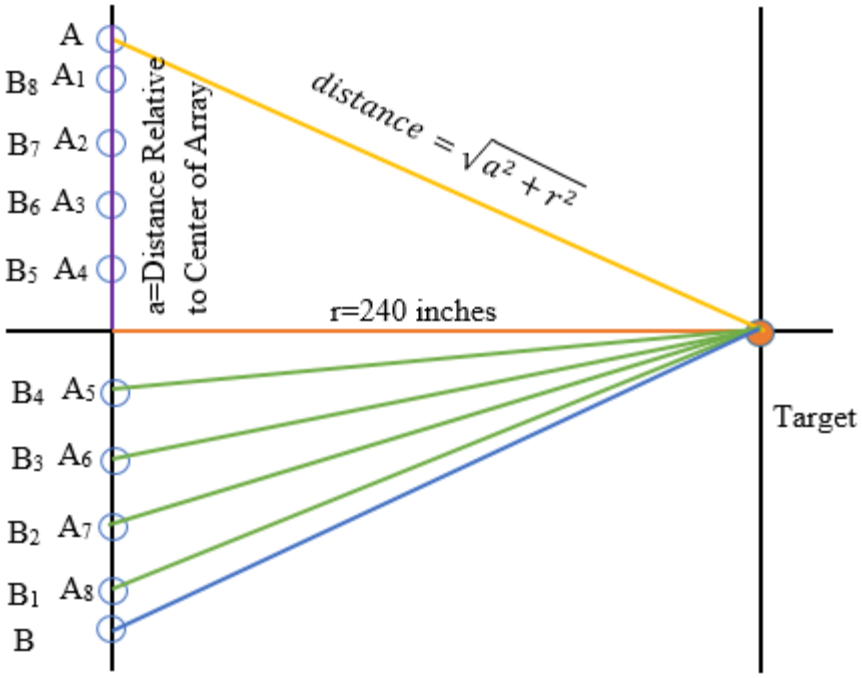


Figure 31. Calculation of Path from Antenna to Target

In Figure 32, the sums of the transmit and receive paths to each antenna were plotted out as sixteen points. As observed in the previous table, the results of each of the antennas A_1 through A_8 are the same as of each of the corresponding antennas B_1 through B_8, which is reflected in the plot below.

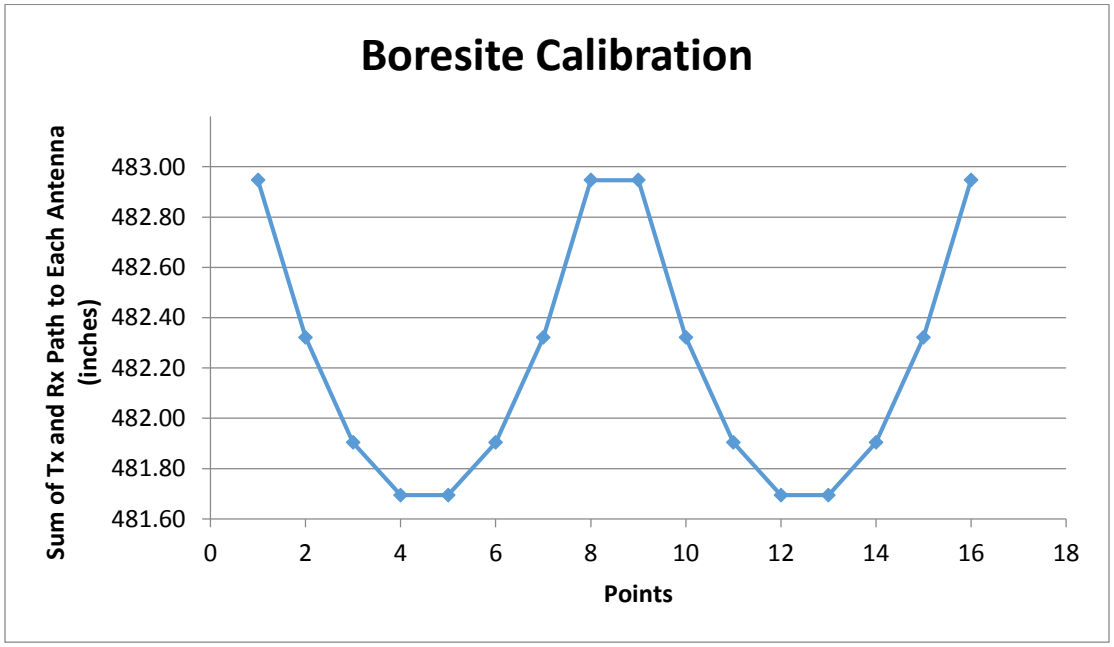


Figure 32. Sum of Tx and Rx Path to Each Antenna for Boresite Calibration

3.6.2 Calculation of Error at Maximum Angle

After calculating the boresite calibration, it is necessary to calculate the error with the target at maximum angle, which is five degrees in this case. When the target is rotated five degrees, the vertical line that the horns are on are also rotated the same angle as shown in Figure 33. The same relationship with the rotated line is present as there was previously with the boresite calibration. The distance between each phase center is the hypotenuse of a right triangle.

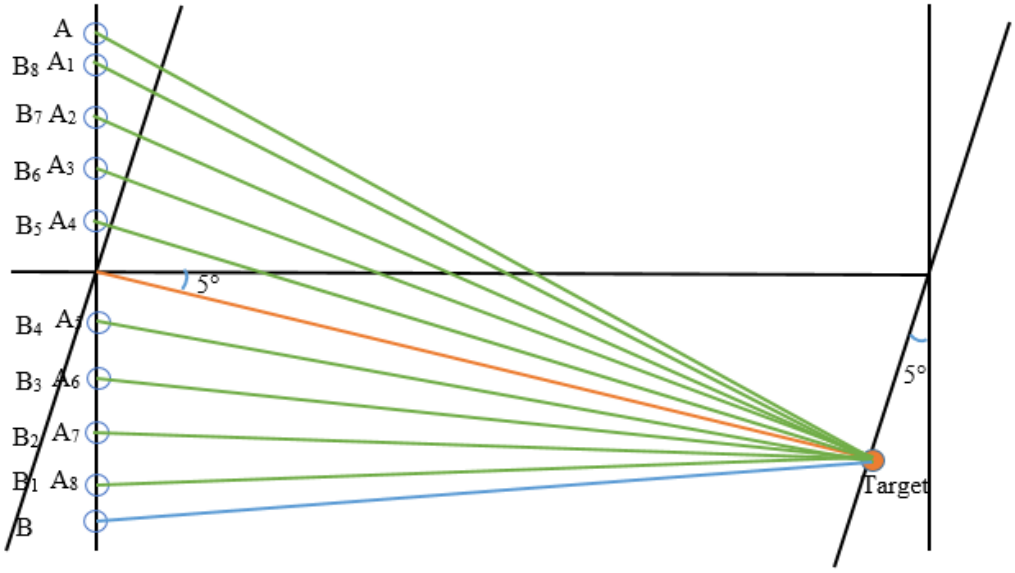


Figure 33. Transmit and Receive Horns with Target Off-Center 5°

The phase centers are being formed from the middle of the transmit horn to the middle of a receive horn, and a line is drawn about halfway in between. This is the reference point for the processing. When it goes to the far field having a transmit and receive field, it is equivalent to having one antenna that does transmit and receive at a point halfway in between. So these sixteen points in phase are taken and then when going off at an angle, there would be a target that's not at boresite and even at far field. If it is shifted and rotated at an angle θ, then the distance to each of the phase centers increases by d*sin(θ).

With the target at boresite, there's no phase difference as d*sin(θ) would be zero since θ is zero so there wouldn't be any difference in the distance. But as the target is rotated, a progressively increasing distance is picked up as it goes from each phase center. That's what the processing is looking for, the phase line coming in with different slope. That is what the scatter energy is being decomposed into, how it comes in at different angles and causes different phase slopes from phase center to phase center.

In the following Table 18, the far field phase centers are calculated by taking the average of the transmit antenna and the receive antenna being calculated. For example for A_1, the far field phase center is calculated in the following manner: $\frac{f_A+f_{A1}}{2} = \frac{24\lambda+21\lambda}{2} = 22.5$. To calculate the far field phase centers in inches as shown in the third column, the values of each far field phase centers is multiplied by 1.18 inches, which is equal to one lambda.

In the fourth column, which is labeled as 2*d*sin(θ) (inches), d*sin(θ) was multiplied by two since it's two-way as with the transmit and receive, it goes out and back, which means it picks up twice the distance. Now the transmit and receive are the same lengths at far field. When that fourth column is plotted, it is a slope line as shown in Figure 34. If θ is equal to zero, it would go to zero, and the path length to all the phase centers would be the same. If θ is increased to 1, it would get bigger. That's the ideal response, so if there is a target at far field, that's how it would respond as.

Table 18. Phase Centers for Each Transmit Antenna

	e=Far Field Phase Centers (lambda)	**d=Far Field Phase Centers (inches)**	**2*d*sin(θ) (inches)**
A1	22.5	26.57480315	-4.17
A2	19.5	23.03149606	-3.61
A3	16.5	19.48818898	-3.06
A4	13.5	15.94488189	-2.50
A5	10.5	12.4015748	-1.95
A6	7.5	8.858267717	-1.39
A7	4.5	5.31496063	-0.83
A8	1.5	1.771653543	-0.28
B8	1.5	1.771653543	0.28
B7	4.5	5.31496063	0.83
B6	7.5	8.858267717	1.39
B5	10.5	12.4015748	1.95
B4	13.5	15.94488189	2.50
B3	16.5	19.48818898	3.06
B2	19.5	23.03149606	3.61
B1	22.5	26.57480315	4.17

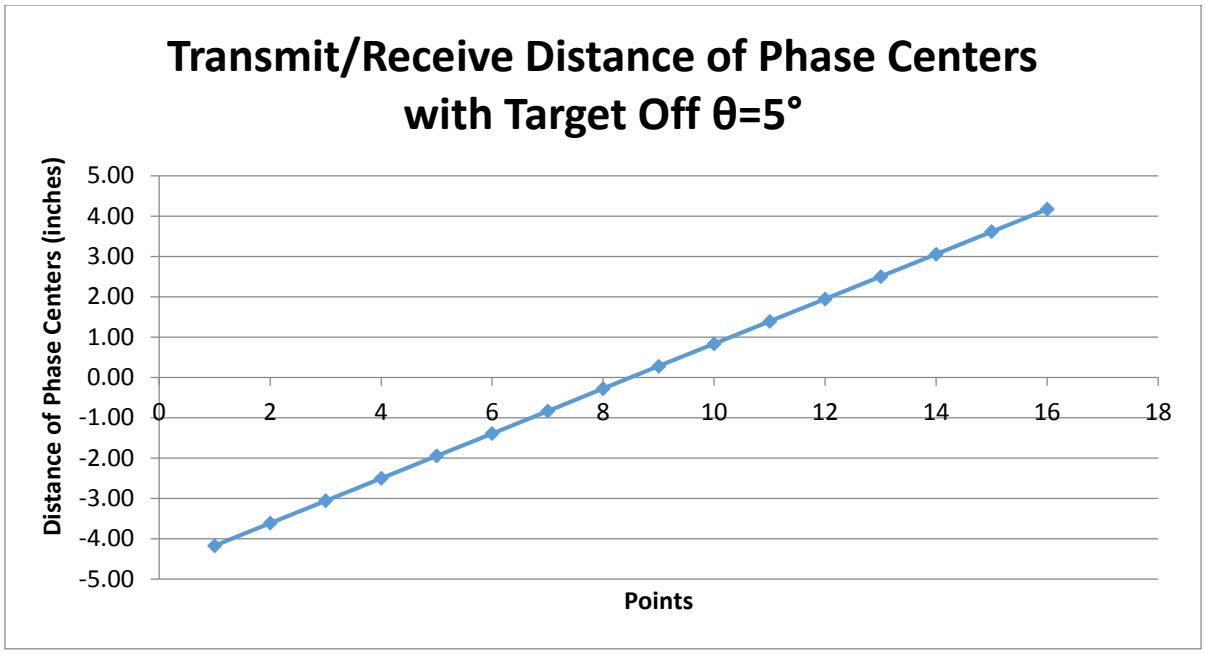


Figure 34. Transmit and Receive Distances of Phase Centers with Target Rotated to θ=5°

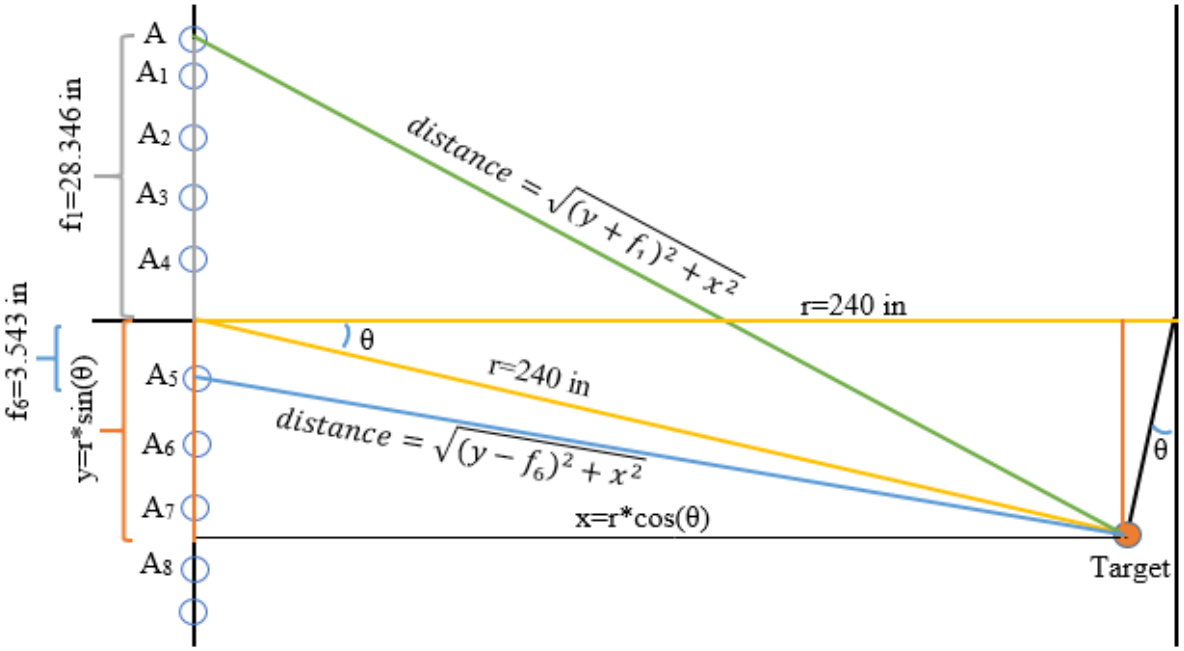


Figure 35. Geometry of Antennas with Target Rotated Off at 5°

Figure 35 above shows the transmit horn as well as the receive horns on the vertical line with the target off-center at five degrees. In this case, the distance relative to the center of the array is denoted as f, in which it is shown that it is 24λ for transmit horn A. Since the target is rotated to θ = 5°, it needs to be accounted for here. The distance to the target is still equal to 240 inches, which is denoted by r, and a right triangle can be formed. The relation is such that from the center of the array down to where the target is located, it is equal to 240 inches times the sine of the angle

θ, and this is denoted as y and is equal to 18.83 inches. The base is denoted as x and it is equal to the distance of the range of 240 inches times the cosine of the angle θ, and the result is 239.26 inches. In order to find the total distance from the horn to the target, the Pythagorean Theorem can be used again for the transmit horn A and the receive horns A_1 through A_4 as follows: $distance\ to\ target = \sqrt{(y+f)^2 + x^2}$.

However, that same relation cannot be used for the receive horns A_5 through A_8 as shown also in Figure 43. For these horns, since they are below the center of the array, the distances relative to the center of the array have to be subtracted from y, which is the following: $distance\ to\ target = \sqrt{(y-f)^2 + x^2}$.

The calculations for the distance to point on the radius of the range, which are the path lengths, are shown below in Table 19. The same process of calculating the sums of the transmit and receive paths to each antenna from the boresite calibration is applied in this case as well. The path length for transmit antenna A is added to the respective path lengths for receive antennas A_1 through A_8, and it is likewise done for transmit antenna B and the receive antennas B_1 through B_8.

For the Resultant column in the table, the sums of the path lengths with the target off five degrees were subtracted from the sums of the path lengths at boresite. For example, for receive antenna A_1, the sum of the path length for boresite calibration is equal to 482.95 inches and the sum of the path length with the target off five degrees is equal to 487.07 inches. The subtraction result is equal to -4.13 inches.

The resultant values are converted from inches to degrees by first converting them to lambda values and multiplying it by 360°. All the distances get converted to phase because a radar can essentially be considered a phase machine, which is why the distance differences were realized. In the error column in inches, the results of the resultant in inches are subtracted from the results of the 2*d*sin(θ) calculated previously in Table 18 above.

Table 19. Calculating Error at Max Angle 4.5°

CALCULATE ERROR AT MAX ANGLE						
	Distance to Point on Radius of Range (inches)	**Sum of Tx and Rx Path to Each Antenna (inches)**	**Resultant (inches)**	**Resultant (deg)**	**Error (inches)**	**Error (deg)**
A	243.87					
A1	243.21	487.07	-4.13	-1257.819076	-0.04	-13.218
A2	242.04	485.90	-3.58	-1091.478135	-0.03	-10.088
A3	241.07	484.93	-3.03	-923.6783062	-0.03	-8.4158
A4	240.30	484.17	-2.48	-754.8362734	-0.03	-7.7861
A5	239.75	483.61	-1.92	-585.3829798	-0.03	-7.7678
A6	239.40	483.27	-1.36	-415.7582631	-0.03	-7.9209
A7	239.26	483.13	-0.81	-246.4052117	-0.03	-7.8023

A8	239.33	483.20	-0.26	-77.76440994	-0.02	-6.9714
B8	243.21	482.66	0.29	88.65160372	-0.01	-3.9158
B7	242.04	481.48	0.84	254.9925449	0.00	-0.7851
B6	241.07	480.52	1.39	422.7923735	0.00	0.88674
B5	240.30	479.75	1.94	591.6344063	0.00	1.51636
B4	239.75	479.20	2.50	761.0876999	0.01	1.53471
B3	239.40	478.85	3.05	930.7124166	0.00	1.38164
B2	239.26	478.71	3.61	1100.065468	0.00	1.50024
B1	239.33	478.78	4.16	1268.70627	0.01	2.33108
B	239.45					

In Figure 36 shown below, the values of the sums of the transmit and receive paths to each antenna are plotted out, and it's taking on the shape of a slope with a hump in the middle, which is desirable. When the processing is being done and the target is across at an angle, it would reflect back a phase slope to each one of the horns that's more severe as it's off at an angle. The slope of that response to each horn when the distance is converted to phase will used to determine the location in the angle space. The ideal result is to have a linear slope. When the target is placed off five degrees, then a response of a linear slope is desired and it would be known if there's a scatter there.

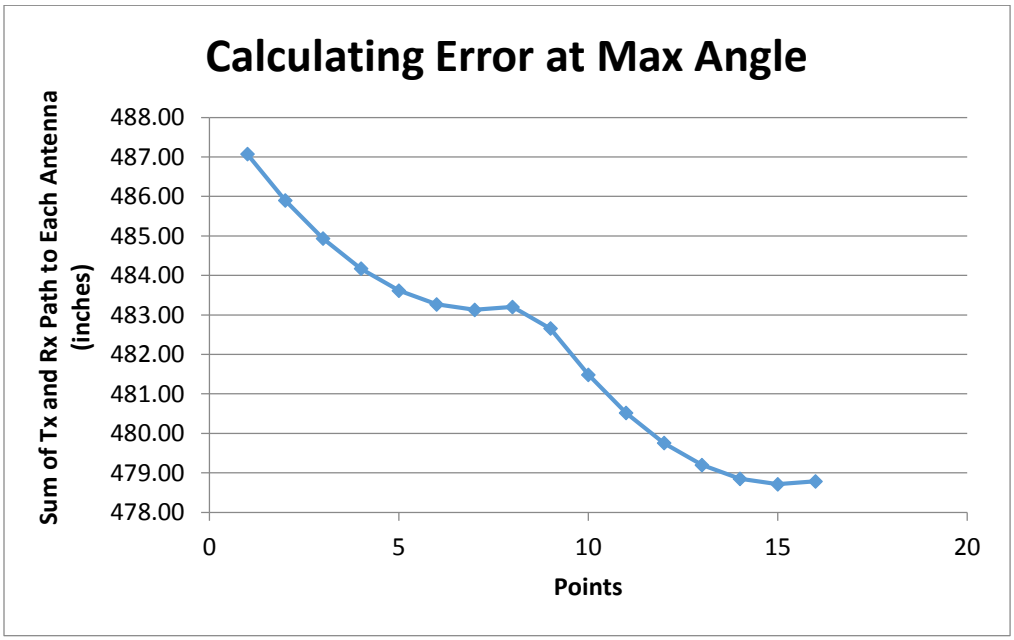


Figure 36. Sum of Tx and Rx Path to Each Antenna for Error Calculation

Figure 37 below shows the resultant, in inches, plotted out and it ends up being a line that is increasing from left to right, which means that calibration is holding. So when the target is off an angle and the different path length differences are calculated and then the original calibration for the errors at boresite is subtracted, a linear response is obtained, which is the desired response. The next thing to do is to compare that to the d*sin(θ) reference.

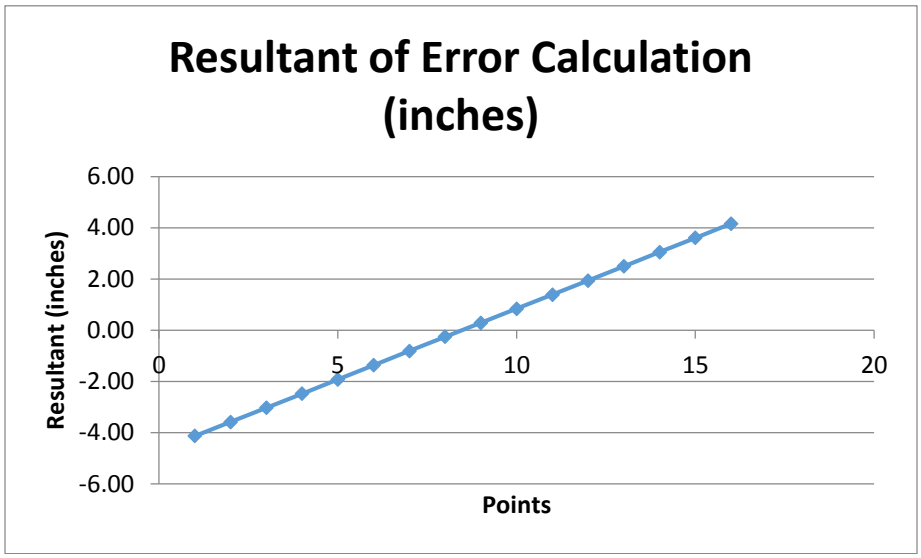


Figure 37. Error Calculation Resultant

In Figure 38 below, the results for the error calculations in degrees are plotted out. This ends up being the phase error that occurs. If everything were ideal, for example if the range was set to far field at 24,000 inches instead of 240 inches, the shape would stay the same but the error would go down to a very small value and that final difference is negligible. At 240 inches, there are ripples, which are the errors. If a perfect scatter at 5° is obtained, then a linear slope would not be obtained as though it was in far field, and instead there be errors obtained.

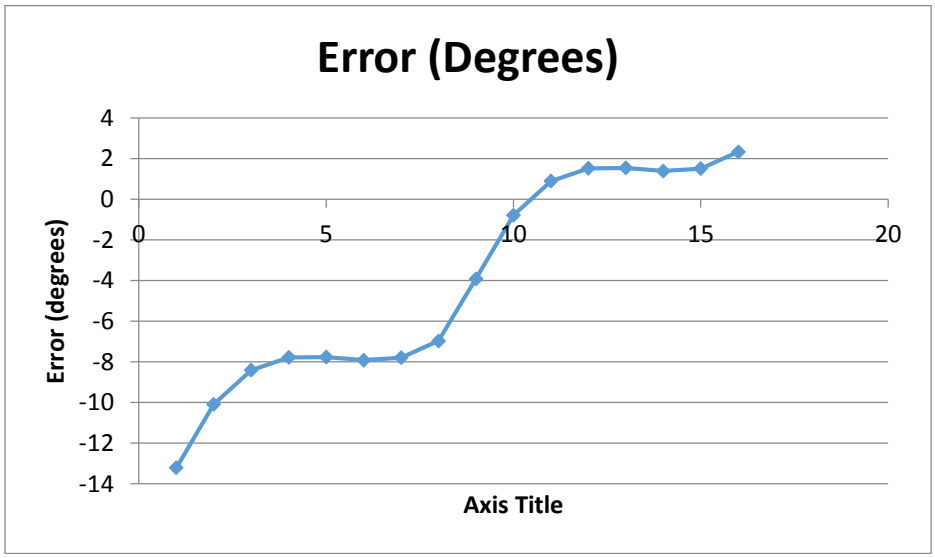


Figure 38. Error for Max Angle

3.7 Mechanical Frame & Auxiliary Systems

Section 3.4 describes the fabricated structures the support the electrical components' ability to transmit, receive, and process signals. Figure 39 depicts the entire Mechanical Frame System as it will stand once fabricated. The entire system is composed of 4 major subsystems: Antenna Structure, Stand Structure, and the Component Box.

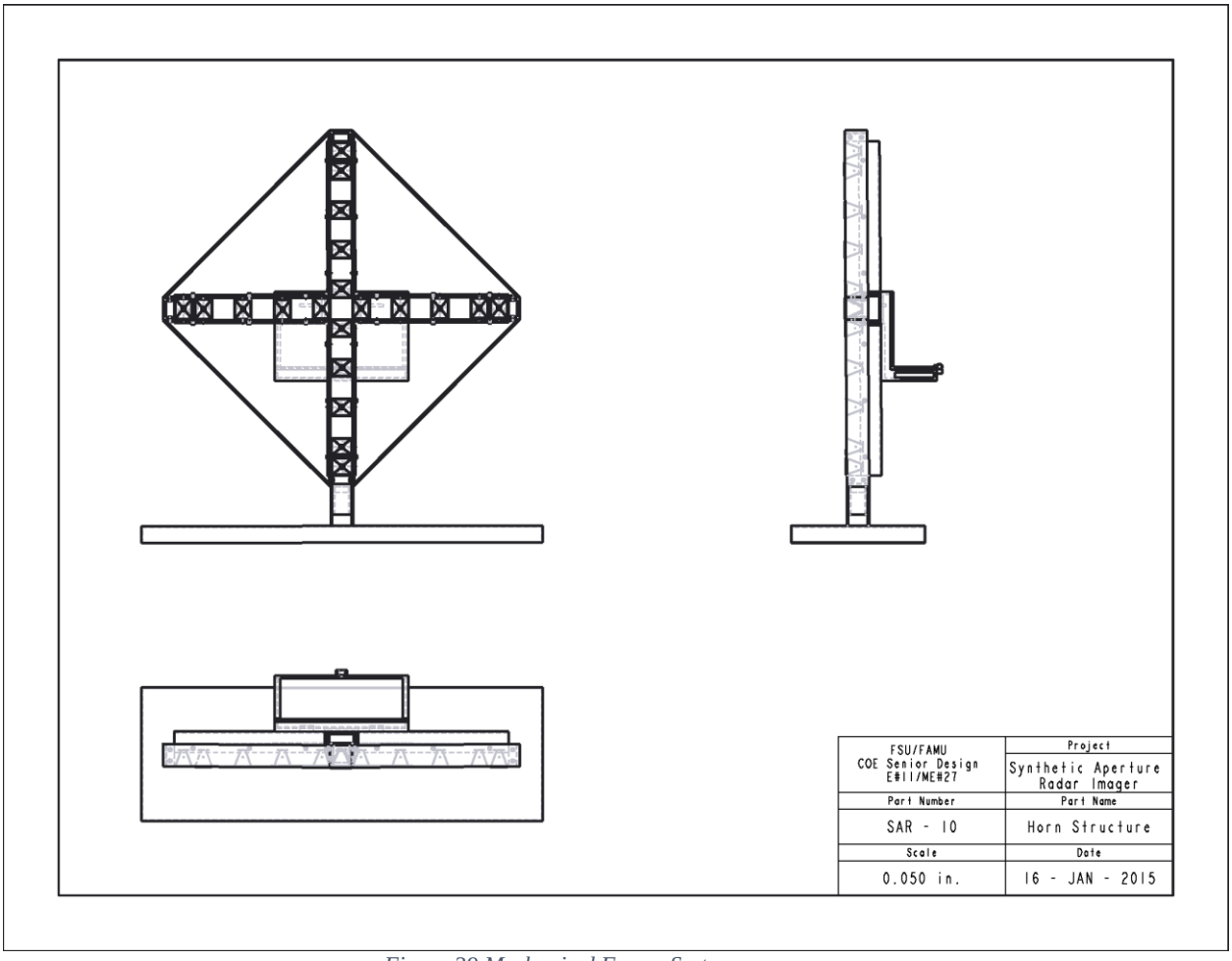


Figure 39 Mechanical Frame System

3.7.1 Mechanical Frame System Exploded View

Figure 40 below depicts the exploded view for the Mechanical Frame System. SAR – 1 refers to the Plexiglas covering to the component box, detailed schematics and dimensions may be referenced in Appendix 10.2. SAR – 2 references the actual design for the component box that attaches to the antenna horn structure, this design was chosen for its capability to optimize the layout and cabling layout for the components; detailed schematics may be referenced in Appendix 10.3. SAR – 3 depicts the Quadrant Connector that marries the Antenna Structure and the Stand Structure; detailed schematics may be referenced in Appendix 10.4. SAR – 4 represents the stand utilized to support the Antenna Structure and the Component Box; detailed schematics may be referenced in Appendix 10.5. SAR – 5 establishes the mode in which the 4 triangular pieces are married together, these connectors allow for the structure to be disassembled in to lighter-weight

parts for easier transportation and storage. Appendix 10.6 describes a detailed schematic of SAR – 5. SAR – 6, SAR – 7, and SAR -8 depict the two types of Quadrant Connectors which singularize the entire frame into a unified system; both of these structures can be examined further in Appendix 10.7, 10.8, and 10.9, respectively. SAR – 9 describes the Quadrants that form the horn apertures, detailed descriptions can be found in Appendix 10.10.

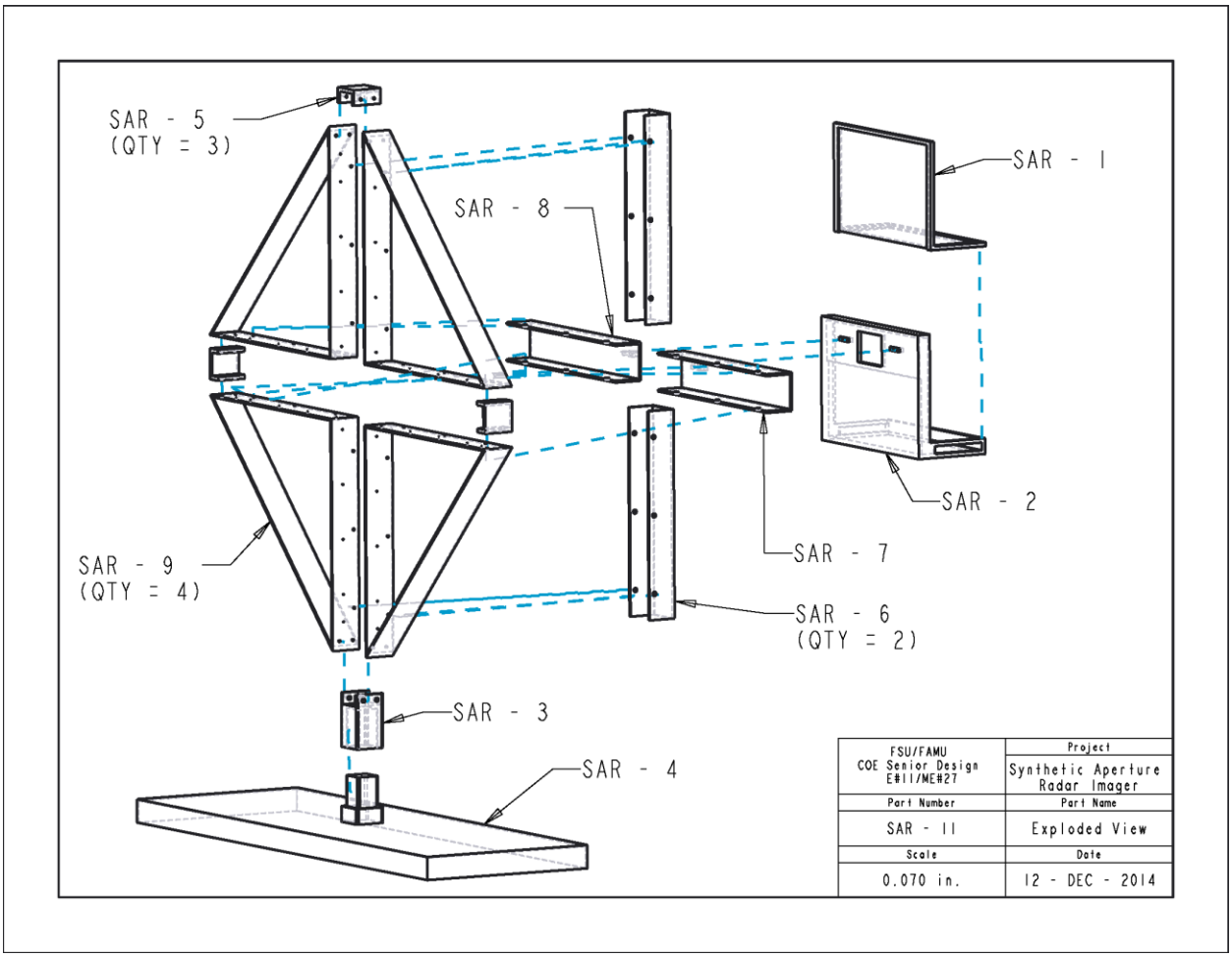


Figure 40 Mechanical Frame System: Exploded View

4 Test Plan

4.1 Test Plan for Major Components

4.1.1 Electrical System

Each electrical component has a theoretical output power level based on its input power. After the first component within the transmit and receive paths, the output power because the input power for the following component with a slight decrease due to the SMA cables connecting components. It is critical the actual output levels for each paths need to be equivalent to the theoretical values with a ±10% leniency in order for transmit and receive antennas to function properly. A power meter will measure the decibel power level of each component. Table 20 represents the input and output power levels required for each component within the *transmit* path. Table 20 represents the input and output power levels required for each component within the *receive* path.

4.1.1.1 Transmit Chain

Input and output power levels for each transmit chain components:

Table 20: Transmit Chain Component Power Levels

Component	Input Power		Output Power	
	[dBm]	***[mW]***	***[dBm]***	***[mW]***
Voltage Controlled Oscillator (VCO)	0	1	-4	0.398
Super Ultra Wideband Amplifier	-4.12	0.387	21.88	154.2
Single Pole Double Throw (SPDT) Switch	21.76	150.0	19.76	94.62
Fixed Attenuator	19.64	92.05	9.64	9.204
Frequency Multiplier	9.44	8.79	-3.06	0.494
Ultra Wide Bandwidth Amplifier	-3.06	0.494	8.94	7.834
Variable Attenuator	8.82	7.621	-4.08	0.382
Band Pass Filter	-4.3	0.372	-7.3	0.186
Power Amplifier	-7.5	0.178	22.5	177.83
Single Pole Four Throw (SP4T) Switch	22.38	172.98	20.38	109.14

4.1.1.2 Receive Chain Components

Input and output power levels for each receive chain components:

Table 21: Receive Chain Component Power Levels

Component	Input Power		Output Power	
	[dBm]	***[mW]***	***[dBm]***	***[mW]***
Single Pole Sixteen Throw (SP16T) Switch	-53.24	4.742E-06	-57.94	1.609E-06
Band Pass Filter	-58.09	1.552E-06	-61.09	7.790E-07
Low Noise Amplifier (LNA-SLNA-120-38-22-SMA)	-61.09	7.780E-07	-23.09	4.915E-03
Variable Attenuator (SA4077)	-23.21	4.775E-03	-27.21	1.903E-03
Low Noise Amplifier (LNA-SLNA-180-38-25-SMA)	-27.33	1.849E-03	10.68	1.168E+01
Radio Frequency (RF) IQ Demodulator	10.56	11.38	3.555	2.267E+00

4.1.1.3 IQ Demodulator Chain Components

Input and output power levels for each receive chain components:

Table 22: IQ Demodulator Chain Component Power Levels

Component	Input Power		Output Power	
	[dBm]	***[mW]***	***[dBm]***	***[mW]***
Voltage Controlled Oscillator (VCO)	0	1	-4	0.398
Super Ultra Wideband Amplifier	-4.12	0.387	21.88	154.2
Single Pole Double Throw (SPDT) Switch	21.76	150.0	19.76	94.62
Fixed Attenuator	19.64	92.05	9.64	9.204
Frequency Multiplier	9.44	8.79	-3.06	0.494
Ultra Wide Bandwidth Amplifier	-3.06	0.494	8.94	7.834
Fixed Attenuator	8.82	7.621	5.82	3.819
LO (IQ Demodulator)	5.55	3.589	-	-

4.1.1.4 Dual Level Shift Circuit

Input and output values for the level shift circuit. These values must be validated by inputting a voltage into the level shift circuit and measuring the output voltages.

Table 23: Level Shift Input and Output Voltages

Vin(Vdc)	Vout(Vdc)	Percent Error		Vin(Vdc)	Vout(Vdc)	Percent Error
-0.34	0.000	0		0.005	1.674	0.27
-0.335	0.024	8.21		0.010	1.699	0.26
-0.330	0.049	8.59		0.015	1.723	0.26
-0.325	0.073	6.99		0.020	1.747	0.25
-0.320	0.097	5.61		0.025	1.771	0.40
-0.315	0.121	4.59		0.030	1.796	0.40
-0.310	0.146	3.85		0.035	1.820	0.39
-0.305	0.170	3.30		0.040	1.844	0.39
-0.300	0.194	2.89		0.045	1.868	0.39
-0.295	0.218	2.56		0.050	1.893	0.38
-0.290	0.243	2.30		0.055	1.917	0.38
-0.285	0.267	2.08		0.060	1.941	0.37
-0.280	0.291	1.90		0.065	1.965	0.37
-0.275	0.315	1.75		0.070	1.990	0.37
-0.270	0.340	1.62		0.075	2.014	0.36
-0.265	0.364	1.51		0.080	2.038	0.36
-0.260	0.388	1.41		0.085	2.063	0.36
-0.255	0.412	1.32		0.090	2.087	0.35
-0.250	0.437	1.24		0.095	2.111	0.35
-0.245	0.461	1.17		0.100	2.135	0.35
-0.240	0.485	1.11		0.105	2.160	0.34
-0.235	0.510	1.05		0.110	2.184	0.34
-0.230	0.534	1.00		0.115	2.208	0.34
-0.225	0.558	0.96		0.120	2.232	0.34
-0.220	0.582	0.91		0.125	2.257	0.33
-0.215	0.607	0.87		0.130	2.281	0.33
-0.210	0.631	0.84		0.135	2.305	0.33
-0.205	0.655	0.80		0.140	2.329	0.32
-0.200	0.679	0.77		0.145	2.354	0.32
-0.195	0.704	0.74		0.150	2.378	0.32
-0.190	0.728	0.71		0.155	2.402	0.32
-0.185	0.752	0.69		0.160	2.426	0.31
-0.180	0.776	0.67		0.165	2.451	0.31
-0.175	0.801	0.64		0.170	2.475	0.31
-0.170	0.825	0.62		0.175	2.499	0.31
-0.165	0.849	0.60		0.180	2.524	0.31
-0.160	0.874	0.58		0.185	2.548	0.30
-0.155	0.898	0.57		0.190	2.572	0.30

-0.150	0.922	0.55		0.195	2.596	0.30
-0.145	0.946	0.53		0.200	2.621	0.30
-0.140	0.971	0.52		0.205	2.645	0.29
-0.135	0.995	0.50		0.210	2.669	0.29
-0.130	1.019	0.49		0.215	2.693	0.29
-0.125	1.043	0.48		0.220	2.718	0.29
-0.120	1.068	0.46		0.225	2.742	0.29
-0.115	1.092	0.45		0.230	2.766	0.29
-0.110	1.116	0.44		0.235	2.790	0.28
-0.105	1.140	0.43		0.240	2.815	0.28
-0.100	1.165	0.42		0.245	2.839	0.28
-0.095	1.189	0.41		0.250	2.863	0.28
-0.090	1.213	0.40		0.255	2.888	0.28
-0.085	1.237	0.39		0.260	2.912	0.27
-0.080	1.262	0.38		0.265	2.936	0.27
-0.075	1.286	0.37		0.270	2.960	0.27
-0.070	1.310	0.36		0.275	2.985	0.27
-0.065	1.335	0.36		0.280	3.009	0.27
-0.060	1.359	0.35		0.285	3.033	0.27
-0.055	1.383	0.34		0.290	3.057	0.27
-0.050	1.407	0.33		0.295	3.082	0.26
-0.045	1.432	0.33		0.300	3.106	0.26
-0.040	1.456	0.32		0.305	3.130	0.26
-0.035	1.480	0.31		0.310	3.154	0.26
-0.030	1.504	0.31		0.315	3.179	0.26
-0.025	1.529	0.30		0.320	3.203	0.26
-0.020	1.553	0.29		0.325	3.227	0.26
-0.015	1.577	0.29		0.330	3.251	0.25
-0.010	1.601	0.28		0.335	3.276	0.25
-0.005	1.626	0.28		0.340	3.300	0.22
0.000	1.650	0.27				

4.1.2 Software Testing

The following Tests will describe the different dub processes that need to be tested in order to check the functionality of the programming aspect of this project. They are as follows:

4.1.2.1 Simulations of the timing

The timing for the switches will be checked via simulation on the Xilinx and Adept software.

4.1.2.2 Testing the timing with a probe and an oscilloscope

The timing for the switches will be checked by outputting the signals to control the switches via testing by a probe. A probe will be placed wherever the pin is, and this probe will have the output shown to the oscilloscope and this will show the discrete outputs from the FPGA.

4.1.2.3 Outputting the voltages received from the A/D converter

The voltage from the A/D output will be checked by being displayed on a 7 segment display on the FPGA. This will verify the functionality of the A/D converter.

4.1.2.4 VGA code test

The VGA code could be checked by using slider switches to generate a digital word that is proportional to what pixels get activated on display. This could be done by letting the VGA display get split into 8 columns, with each column being controlled by a slider switch. When a slider switch gets activated, the portion of the VGA display controlled by that slider switch would light up. This would show proper communication between the VGA display and the FPGA

4.1.3 Static SAR Phased Array Propagation Testing

The following tests will describe the different sub-processes that need to take place before testing the overall SAR theme phase array radar system. In addition, test plans for the final 2-d testing will also be illustrated.

4.1.3.1 Transmitting Antenna/Waveguide Adapter Power Test

The necessary transmit power for the each transmitting horn antennas to propagate an X-band beam, traveling a minimum of 20 [ft], is 18.97 [dBm] (78.88 [mW]). To confirm that each transmit horn antenna is receiving its required power flow, a power meter will be utilized. Separately, a power meter will replace one of the transmit horns and its connected waveguide adapter in the transmit path of the radar system. When the radar system starts, the power meter will sample the power flow at the location of the transmit horn antenna in the system and provide the actual transmit power. If the actual transmit power for all of the transmit antennas match the theoretical value with ±5% error, then each horn will be able to form a beam that can travel 20 [ft]. Figure 41 illustrates the power testing design for the transmit antennas.

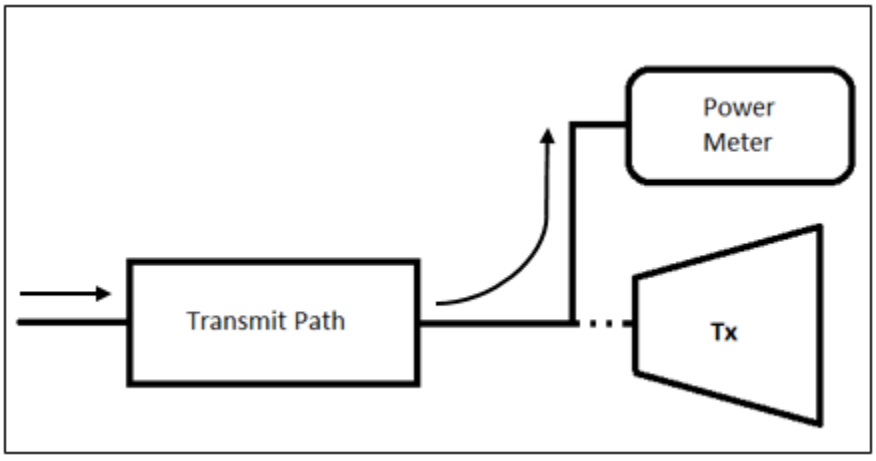


Figure 41: Transmit Power Test Design with Power Meter

4.1.3.2 Receiving Antenna/Waveguide Adapter Power Test

The test plan to determine if the actual receive power is equivalent to the calculated, theoretical receive power compares similar to the transmitting power test. A power meter will

replace a receive horn antenna and waveguide adapter and record the power level being inputted into the receive antenna. Each receive antenna will be test individually and have the same results. The theoretical receive power is -51.25 [dBm] ($4.75x10^{-6}$ [mW]). If the actual receive power for all of the receive antennas match the theoretical value, then the each receiver will be able to detect and reflected, response signal. Figure 42 illustrates the power testing design for the receive antennas.

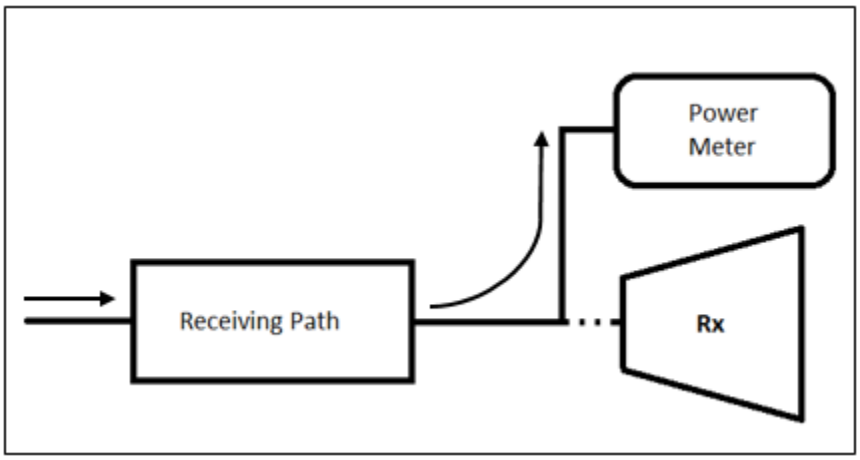


Figure 42: Receive Power Test Design with Power Meter

4.1.3.3 Radiating at Correct Frequency Test

The following test will determine if the transmit horn antennas are actually radiating and at the correct frequency of 10 [GHz]. Employing an extra spare horn antenna and waveguide adapter, a movable radiation tester can be constructed. A spectrum analyzer is connected to the spare waveguide adapter and horn antenna. The horn then acts a receive antenna and is angled towards the transmit antenna being tested. If the transmit antenna is radiating, the spectrum analyzer will plot the signal level and frequency absorbed by the receive antenna. This test will confirm that each transmit horn antenna is radiated at 10 [GHz]. Note, each transmit horn needs to be tested individually. Figure 43 illustrates the testing design.

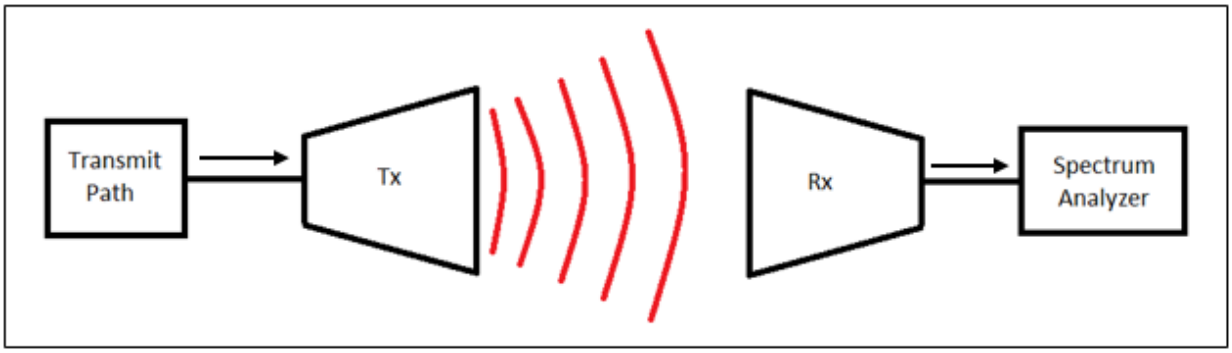


Figure 43: Radiating & Frequency Test Design

4.1.3.4 Final Static SAR System Test

4.1.3.4.1 1-D Antenna Array Test

Before running the final radar system test which will generate a 2-d image, each antenna array needs to be tested. Both arrays will conduct the same test. To only test one array, disconnect the horn antennas from one array while the other antenna array is being tested. Each antenna array will transmit and receive through a self-made anechoic chamber, constructed of radio frequency absorbance foam. At the end of the chamber, a trihedral, located at the center point of the far end of the anechoic chamber, will reflect the radiation back towards the antenna array. The reflected signal will be picked up by the receive antennas and processed through the demodulator and determined through signal processing software where the one-dimensional column or row, depending on which array is being tested, needs to be highlighted based on the return signal. Since the trihedral is located at the mid-point, the middle column or row should be lit up after the data is processed through signal process programing. The constant position of the trihedral creates a known variable for the calibration process. Figure 44 illustrates the setup for testing with the anechoic chamber.

4.1.3.4.2 2-D Full SAR Final Test (Projected Goal)

If both antenna arrays function properly during the *1-D Antenna Array Test*, then testing the final design should not have any complications. The final SAR antenna design, both elevation and azimuth arrays, is directed into the anechoic chamber and towards the trihedral on the far side of the chamber. The anechoic chamber will extinguish any existing ambiguous radiation waves, preventing any misleading results. The design of the anechoic chamber will slim the 9'x9' beamwidth of each horn by the narrowness of the chamber size. The anechoic chamber will have four 6'x22' chamber walls and one 6'x'6 end wall at the end of the chamber. Figure 46 illustrates the final test setup with the anechoic chamber. The trihedral will reflect back any radiation directly back towards the antenna structure for the receive horn antennas to collect any radiation. After the return signal has been deciphered through the demodulator and process with the same signal processing program used for the one-dimensional antenna array tests, only a small box should be highlighted on the computer screen. The highlighted box represents the location of the trihedral, which should be center of the screen which represents the mid-point of the far end of the anechoic chamber. Again, the trihedral will provide calibration references when mending the overall SAR antenna design.

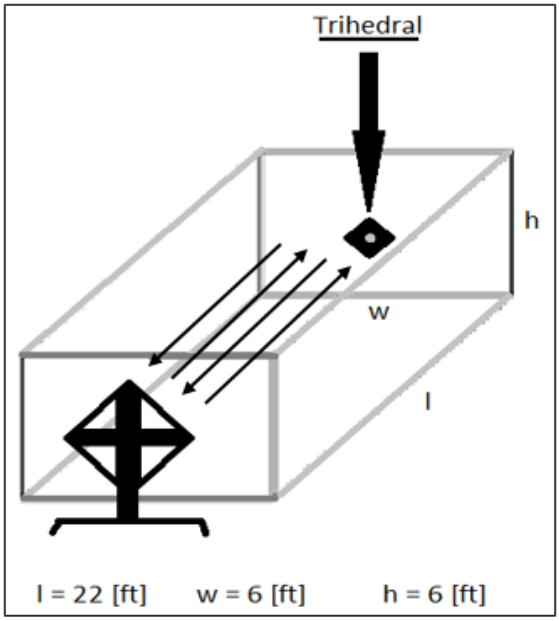


Figure 44: Final Antenna Structure with Anechoic Chamber Setup

4.1.3.4.3 Contingency Plan for Full Static SAR Final Test

If the component designs for the transmit and receive paths do not create the necessary power levels or fail to produce a 10 [GHz] signal, then the original project goal needs to be simplified to a simpler task by employing laboratory testing equipment: a signal generator and spectrum analyzer. The new goal for the project will be to at least transmit a 10 [GHz] signal through one horn antenna and be able to switch on another horn to act as a receiver, while also switching off the transmitting horn. Both horns, receive and transmit, will be angled towards the trihedral located at the end of the anechoic chamber. A new antenna structure does not constructed for the contingency design. Horn antennas from the antenna arrays can be utilized. The signal generator will be wired to the transmit antenna's path and create a continuous 10 [GHz] waveform. While the spectrum analyzer will determined the return signal's strength after being obtained by the receive antenna. Figure 45 illustrates the connection setup with the spectrum analyzer and signal generator with horn antennas. The contingency plan is extremely simple compared to the original project goal, but it does still demonstrate radar concepts. Figure 47 illustrates the setup for the contingency test plan, which is the same as original goal's setup since horn antennas on the structure can still be exercised.

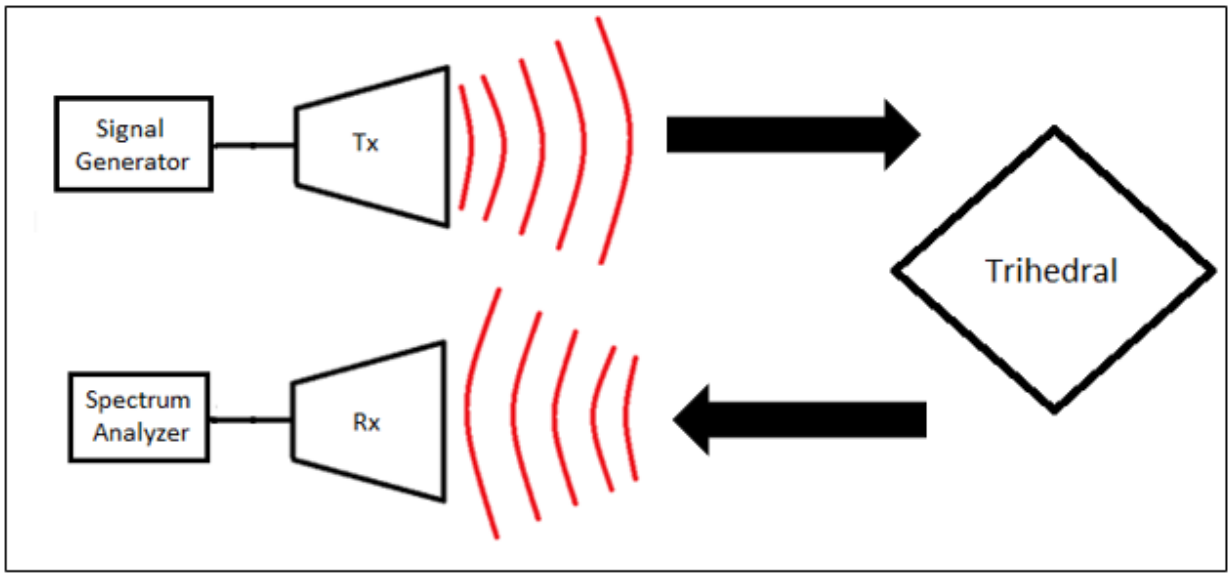


Figure 45: Contingency Plan Configuration

4.1.4 Power Supply

The voltages and currents output from each regulator must be verified by providing the necessary input voltages to the board using the DC power supplies. Once the input sources are measured and verified the output voltages and currents from each of the regulators can be measured with a voltmeter, ammeter or a multimeter. See Table 24 below for the output voltages and currents.

Table 24: Input DC Power Supplies

QTY	Voltage (Vdc)
1	-25
5	10
2	15
1	20

Table 25: Component Power Supply Requirements

QTY	Part Name	V+(Vdc)	I+ (mAdc)	V- (Vdc)	I- (mAdc)
1	VCO	3.3	45	-	-
1	FPGA Board	3.3	200	-	-
1	SPDT Switch	5	1.4	-	-
1	SP4T Switch	5	160	-5	50
1	SP16T Switch	5	550(max)	-12	200(max)
1	IQ Demodulator	5	110	-5	-
1	Super Ultra Wideband Amplifier	12	400(max)	-	-

2	Ultra Wide Bandwidth Amplifier	12	62	-	-
1	Low Noise Amplifier SLNA-120-38-22-SMA	12	250	-	-
1	Low Noise Amplifier SLNA-180-38-25-SMA	12	280	-	-
1	Power Amplifier	15	900	-	-
2	Level Shift Op Amp (V+)	3.5		-	-
2	Level Shift Op Amp (VRef)	1.65	-	-	-

5 Schedule

Below in Table 26 is a task list for the spring 2015 semester. A full view of the Gantt chart can be seen in the Appendix 10.12. Critical activities for the project have been identified in red on the Gantt chart and a responsible person has been assigned to each task.

There is a delay in the schedule with component ordering due to changing parts and some vendors being out of stock on merchandise that had previously been labeled in stock on the company's website. Also, the team has identified some "problem items" for materials needed to perform certain tasks. The anechoic radar absorbing foam has yet to be ordered. Since the foam is expensive per 2'x2' square, the team would like to know an exact measurement of how many square feet to purchase. The testing facility was recently secured so now the team can take measurements of the room and get the proper dimensions. Matthew Cammuse has been assigned as the responsible person to develop the layout of the foam and coordinate with Benjamin Mock for ordering. Another problem item on the schedule is acquiring the DC power supplies and testing equipment. The team is currently working on the power system design and identifying the necessary testing equipment needed. Once these items are finalized, procurement can take place.

Some upcoming tasks for the project on the critical path include the FPGA code simulation and testing, as well as the subassembly testing of the Transmit Signal and Modulator LO Chain. These tasks are priority because this is what the team plans to show in the mid-term hardware/software review during the week of February 23-27, 2015. The review will show partial elements of each chain and provide some coding for the timing diagrams, discrete controls of switches, and the analog-to-digital converter code.

Other critical items on the schedule are the assembly of the frame and attachment of the component box. The mechanical engineers have obtained a preliminary quote from a local welding company to assemble the antenna frame. Once any last changes to the frame design have been made by February 11, 2015, the final design will be submitted to the vendor and

funds will be allocated to start assembly on February 12, 2015. The critical date for the frame to be assembled and ready for use is February 27, 2015.

The electrical engineers will need approximately 3-5 weeks to perform the hardware and software integration in preparation for the final project demonstration during the week of April 6-10, 2015. In order to integrate all the parts and software on time, the frame must be ready by that February deadline. However, earlier would be better so that the electrical and mechanical engineers could begin setting up the assembly.

Lastly, syncing the hardware with software is critical to project completion and has been identified as a critical item in the schedule. In order to perform the final testing of the entire integrated system the software must be compatible with the hardware by April 3, 2015. Troubleshooting the system is also a critical path item because there are only three days left in the schedule to fix any problems before the final review.

Table 26: Tentative Spring 2015 Schedule

Task Name	Duration	Start	Finish	Resource Names
Begin Spring Semester	0 days	Wed 1/7/15	Wed 1/7/15	**All**
Internal Team Meeting: 5pm	0 days	Mon 1/12/15	Mon 1/12/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/14/15	Wed 1/14/15	**Pete Stenger, All**
FPGA Programming	9 days	Thu 1/8/15	Tue 1/20/15	**Patrick De La llana**
Timing Diagrams	8 days	Thu 1/8/15	Mon 1/19/15	Patrick De La llana
Waveguide Adapter Selection	10 days	Mon 1/12/15	Fri 1/23/15	Matthew Cammuse
Obtain Testing & Storage Facility	15 days	Mon 1/12/15	Fri 1/30/15	**Benjamin Mock, Jasmine Vanderhorst**
Meet with CAPS Safety Coordinator: Michael Coleman	4 days	Mon 1/12/15	Thu 1/15/15	Benjamin Mock, Jasmine Vanderhorst
Complete Online Safety Training	7 days	Thu 1/15/15	Fri 1/23/15	All
Attend EHS Safety Class	1 day	Fri 1/30/15	Fri 1/30/15	All
Identify Problem Items	18 days	Mon 1/12/15	Wed 2/4/15	**Benjamin Mock**
Radar Absorbing Foam	11 days	Mon 1/12/15	Mon 1/26/15	Matthew Cammuse
DC Power Supplies	8 days	Mon 1/26/15	Wed 2/4/15	Joshua Cushion
Internal Team Meeting: 5pm	0 days	Mon 1/19/15	Mon 1/19/15	**Jasmine Vanderhorst**
Frame Design	13 days	Mon 1/19/15	Wed 2/4/15	**Malcolm Harmon, Mark Poindexter**
Stress Analysis	10 days	Mon 1/19/15	Fri 1/30/15	Malcolm Harmon
Material Justifications	10 days	Mon 1/19/15	Fri 1/30/15	Malcolm Harmon
Component Layout Schematic	5 days	Wed 1/28/15	Tue 2/3/15	Mark Poindexter

Obtain Preliminary Frame Welding Price Quote	3 days	Mon 2/2/15	Wed 2/4/15	Mark Poindexter
Component Ordering	13 days	Mon 1/19/15	Wed 2/4/15	**Benjamin Mock**
Update Budget	6 days	Mon 1/19/15	Mon 1/26/15	Benjamin Mock
Identify Component Risks	7 days	Mon 1/26/15	Tue 2/3/15	Benjamin Mock
Level Shift Circuit Design	12 days	Tue 1/20/15	Wed 2/4/15	**Joshua Cushion**
Programming Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La llana**
Discrete Code Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	Patrick De La llana
7-Segment Display Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	Patrick De La llana
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/21/15	Wed 1/21/15	**Pete Stenger, All**
Ongoing Progress: Signal Processing	6 days	Wed 1/21/15	Wed 1/28/15	**Julia Kim**
Power Supply Design	4 days	Mon 1/26/15	Thu 1/29/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 1/26/15	Mon 1/26/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/28/15	Wed 1/28/15	**Pete Stenger, All**
Ongoing Progress: Signal Processing	6 days	Wed 1/28/15	Wed 2/4/15	**Julia Kim**
Develop Testing Plans	7 days	Wed 1/28/15	Thu 2/5/15	**Matthew Cammuse**
Individual Component Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
Subassembly Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
System Integration Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
Gather Appropriate Safety Signage	6 days	Fri 1/30/15	Fri 2/6/15	**Benjamin Mock**
Anechoic Foam Layout	11 days	Fri 1/30/15	Fri 2/13/15	**Matthew Cammuse**
Shipping Arrangements	11 days	Fri 1/30/15	Fri 2/13/15	**Benjamin Mock**
RF Lambda Vendor Parts	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock
Marki: Band-pass Filter	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock
Fairview Vendor Parts	7 days	Fri 1/30/15	Mon 2/9/15	Benjamin Mock
Digikey Vendor Parts	9 days	Fri 1/30/15	Wed 2/11/15	Benjamin Mock
Minicircuits Vendor Parts	11 days	Fri 1/30/15	Fri 2/13/15	Benjamin Mock
Team Meeting & Preparation for VP of Northrop Grumman	1 day	Mon 2/9/15	Mon 2/9/15	All
Internal Team Meeting: 5pm	0 days	Mon 2/2/15	Mon 2/2/15	**Jasmine Vanderhorst**
Calibration Plan: Hardware & Software Compatibility	3 days	Mon 2/2/15	Wed 2/4/15	**Joshua Cushion**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/4/15	Wed 2/4/15	**Pete Stenger, All**

Team Members Submit Report Sections	0 days	Wed 2/4/15	Wed 2/4/15	**All**
Milestone 4 Report Due	0 days	Thu 2/5/15	Thu 2/5/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 2/4/15	Wed 2/11/15	**Julia Kim**
Data Storing Software for FPGA to PCU	12 days	Thu 2/5/15	Fri 2/20/15	**Matthew Cammuse, Patrick De La llana**
Finalize Frame Design	3 days	Tue 2/10/15	Thu 2/12/15	**Malcolm Harmon, Mark Poindexter**
GO/NO-GO Design Stopping Point	2 days	Tue 2/10/15	Wed 2/11/15	**Mark Poindexter, Malcolm Harmon, Pete Stenger**
Submit Final Design Welding Vendors	2 days	Wed 2/11/15	Thu 2/12/15	**Malcolm Harmon, Mark Poindexter, Pete Stenger**
Prepare Presentation	4 days	Mon 2/9/15	Thu 2/12/15	**Jasmine Vanderhorst**
Milestone 4: Detailed Design Review & Test Plan Presentation	5 days	Mon 2/9/15	Fri 2/13/15	**All**
Northrop Grumman VP Visit and Project Update	2 days	Tue 2/10/15	Wed 2/11/15	**Pete Stenger, All**
Programming & Testing	20 days	Mon 2/9/15	Fri 3/6/15	**Patrick De La llana**
Analog To Digital Conversion Code	11 days	Mon 2/9/15	Mon 2/23/15	Patrick De La llana
FPGA Code Simulation and Testing	15 days	Mon 2/16/15	Fri 3/6/15	Patrick De La llana
Build Component Box and Attach to Frame	15 days	Mon 2/9/15	Fri 2/27/15	**Mark Poindexter**
Receive Completed Antenna Frame	0 days	Fri 2/27/15	Fri 2/27/15	**Malcolm Harmon**
Transmit and Modulator LO Chain Component Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Matthew Cammuse, Joshua Cushion**
Programming Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Patrick De La llana**
Subassembly Testing	10 days	Mon 2/9/15	Fri 2/20/15	**Joshua Cushion, Matthew Cammuse**
Transmit Signal and Modulator LO Chain	5 days	Mon 2/9/15	Fri 2/13/15	Joshua Cushion, Matthew Cammuse
Power Supply Board	3 days	Wed 2/18/15	Fri 2/20/15	Joshua Cushion, Matthew Cammuse
Data Gathering, Analysis, and Reporting	10 days	Mon 2/9/15	Fri 2/20/15	Julia Kim
Miscellaneous Task	10 days	Mon 2/9/15	Fri 2/20/15	Julia Kim
Receive Signal Chain	6 days	Fri 2/13/15	Fri 2/20/15	Joshua Cushion, Matthew Cammuse

Ongoing Progress: Signal Processing	6 days	Wed 2/11/15	Wed 2/18/15	**Julia Kim**
Build Power Supply Board	3 days	Mon 2/16/15	Wed 2/18/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 2/16/15	Mon 2/16/15	**Jasmine Vanderhorst**
Ongoing Progress: Signal Processing	6 days	Wed 2/18/15	Wed 2/25/15	**Julia Kim**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/18/15	Wed 2/18/15	**All**
Software Demonstration	5 days	Mon 2/23/15	Fri 2/27/15	**Patrick De La llana**
Discrete Code Switch Display	2 days	Mon 2/23/15	Tue 2/24/15	Patrick De La llana
A-to-D Conversion Display	2 days	Tue 2/24/15	Wed 2/25/15	Patrick De La llana
Tentative: VGA Imaging Display	2 days	Thu 2/26/15	Fri 2/27/15	Patrick De La llana
Internal Team Meeting: 5pm	0 days	Mon 2/23/15	Mon 2/23/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/25/15	Wed 2/25/15	**All**
Milestone 5: Midterm Hardware/Software Reviews	5 days	Mon 2/23/15	Fri 2/27/15	**All**
DC Wire Harness	**23 days**	**Mon 2/16/15**	**Wed 3/18/15**	**Mark Poindexter**
Wire Design Support for Pre-Fab	8 days	Mon 2/16/15	Wed 2/25/15	Julia Kim
Design DC Wire Harness	8 days	Mon 2/16/15	Wed 2/25/15	Mark Poindexter
Build DC Wire Harness	8 days	Wed 2/25/15	Fri 3/6/15	Malcolm Harmon
Troubleshooting	9 days	Fri 3/6/15	Wed 3/18/15	Malcolm Harmon, Julia Kim, Mark Poindexter
Ongoing Progress: Signal Processing	6 days	Wed 2/25/15	Wed 3/4/15	**Julia Kim**
VGA Coding	20 days	Mon 3/2/15	Fri 3/27/15	**Patrick De La llana**
Spring Break: No School	5 days	Mon 3/9/15	Fri 3/13/15	**All**
Ongoing Progress: Signal Processing	11 days	Wed 3/4/15	Wed 3/18/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/16/15	Mon 3/16/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/18/15	Wed 3/18/15	**All**
Hardware Integration	25 days	Mon 3/2/15	Fri 4/3/15	**Joshua Cushion, Julia Kim, Mark Poindexter, Matthew Cammuse, Patrick De La llana**
Soldering Components	13 days	Mon 3/2/15	Wed 3/18/15	Matthew Cammuse, Patrick De La llana
Install and Fasten Components	13 days	Mon 3/2/15	Wed 3/18/15	Malcolm Harmon, Mark Poindexter
Cabling	5 days	Thu 3/19/15	Wed 3/25/15	Mark Poindexter

Power Connection	10 days	Mon 3/23/15	Fri 4/3/15	Joshua Cushion, Julia Kim
Software Integration	25 days	Mon 3/2/15	Fri 4/3/15	**Patrick De La llana**
Integrate all codes with FPGA Board	22 days	Mon 3/2/15	Tue 3/31/15	Patrick De La llana
Sync Hardware with Code	15 days	Mon 3/16/15	Fri 4/3/15	Patrick De La llana, Joshua Cushion
Troubleshooting	10 days	Mon 3/23/15	Fri 4/3/15	Joshua Cushion, Julia Kim, Matthew Cammuse, Patrick De La llana
Ongoing Progress: Signal Processing	6 days	Wed 3/18/15	Wed 3/25/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/23/15	Mon 3/23/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/25/15	Wed 3/25/15	**All**
System Testing	11 days	Mon 3/23/15	Mon 4/6/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 3/25/15	Wed 4/1/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/30/15	Mon 3/30/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 4/1/15	Wed 4/1/15	**All**
Design Project Poster	5 days	Wed 4/1/15	Tue 4/7/15	**Jasmine Vanderhorst**
Finalize Signal Processing	6 days	Wed 4/1/15	Wed 4/8/15	**Julia Kim**
ECE Senior Design Fair	0 days	Thu 4/9/15	Thu 4/9/15	**All**
Milestone 6: Final System Demonstration	5 days	Mon 4/6/15	Fri 4/10/15	**All**
Reliability Engineering: Fault Tree Analysis	8 days	Mon 4/6/15	Wed 4/15/15	**Benjamin Mock, Jasmine Vanderhorst**
User Manual and Guide	8 days	Mon 4/6/15	Wed 4/15/15	**Benjamin Mock, Jasmine Vanderhorst, Matthew Cammuse**
Project Turnover & Lessons Learned	8 days	Mon 4/6/15	Wed 4/15/15	**All**
Milestone 7: Final Project Report	0 days	Thu 4/16/15	Thu 4/16/15	**All**
Prepare Presentation	4 days	Mon 4/13/15	Thu 4/16/15	**Jasmine Vanderhorst**
Milestone 7: Final Project Presentation	5 days	Mon 4/13/15	Fri 4/17/15	**All**

6 Budget Estimate

Below in Table 27 is an official update for the $50,000 budget. Listed in the table are the name of the component/test equipment and their associated prices with a total summation and remaining balance reported at the end of the table. Quote and estimate analyses were performed from a varied amount of vendors and distributors, where possible, to ensure that

the most cost-effective option was selected with relation to lead and delivery times.

Table 27: Budget Analysis

Component	Product Number	Quantity	Unit Price	Total Price
Power Amplifier	SPA-110-30-01-SMA	1	1930.72	1930.72
Low Noise Amplifier	SLNA-120-38-22-SMA	1	1361.40	1361.40
Variable Attenuator	SA4077	3	580.84	1742.53
Fixed Attenuator	SA18H-07	3	44.55	133.65
Fixed Attenuator	SA18H-08	3	44.55	133.65
Fixed Attenuator	SA18H-08	3	44.55	133.65
Fixed Attenuator	SA18H-09	3	44.55	133.65
Fixed Attenuator	SA18H-10	3	44.55	133.65
Fixed Attenuator	SA18H-03	3	44.55	133.65
Band Pass Filter	SA18H-06	3	240.00	480.00
FPGA Board	Nexys 3	2	189.00	378.00
ADC	410-064P-KIT	2	37.00	74.00
Pmod Test Point Header	410-135P	3	16.00	48.00
Antenna Horns	MA86551	25	22.50	562.50
VCO Kit	126489-HMC820LP6CE	1	327.98	327.98
SPDT	HMC-C058	1	2482.01	2482.01
SP4T	RFSPaTA0812G	1	1725.00	1725.00
SP16T	UMC SR-L010-16S	1	4009.00	4009.00
Wideband Amplifier	ZVA-183-S+	1	895.00	895.00
Waveguide Adapters	90-422	22	175	3740.00
50 Ohm Loads (Male)	ST1819	15	16.66	249.90
50 Ohm Loads (Female)	ST1825F	5	22.64	113.20
SMA Connector M-M	ACX1240-ND	5	6.13	30.65
SMA Connector F-M	ACX1246-ND	5	7.07	35.35
SMA Connector F-F	ACX1242-ND	5	5.23	26.15
SMA-BNC Adap. M-M	501-1341-ND	5	12.67	63.35
SMA-BNC Adap. M-F	501-1141-ND	5	10.51	52.55
SMA-BNC Adap. F-M	501-1140-ND	5	10.51	52.55
SMA-BNC Adap. F-F	501-1338-ND	5	9.99	49.95
48” RF Cables	SCA49141-48	3	6.13	44.10
36” RF Cables	SCA49141-36	25	7.07	339.00
12” RF Cables	SCA49141-12	3	5.23	37.80
7” RF Cables	SCA49141-07	5	12.67	63.00
5” RF Cables	SCA49141-05	10	10.51	126.00
3” RF Cables	SCA49141-03	10	10.51	126.00
Ultra Wideband Amplifier	ZX60-14012L+	3	179.95	539.85

Frequency Amplifier	ZX90-2-50-S+	2	41.95	83.90
Low Noise Amplifier	SLNA-180-38-25-SMA	1	1205.00	1205.00
Anechoic Absorber		X	50.00	50.00X
Mechanical Frame	N/A	1	12678.00	2557.00
Field Strength Meter		1	129.95	129.95
RF Detector	A409	1	500.00	500.00
Signal Generator	AT-N5183B	1	1302.02	1302.02
Signal Analyzer	AT-N9030A	1	1816.00	1816.00
			Total Cost	31789.29
			Savings	18210.71

7 Risk Assessment

7.1 Shipping Risks

Risk: Northeast Snow Blizzard Delays Shipping
Consequence: The Coaxial Waveguide Adapter from ARRA has been ordered. However, the shipping time has been delayed due to the ongoing snow blizzard in the Northeast corner of the United States. The Coaxial Waveguide Adapters connect to the antennas and without the coaxial waveguide adapter the system will not propagate the signal.
Mitigation Strategy: Keep open contact with vendors for updated delivery times once the snow blizzard passes. If unable to get desired vendor at optimal price, the team will have to order from another vendor at a higher price.

7.2 Budget Risks

Risk: Insufficient Funds
Consequence: If the $50,000 budget is spent before all parts, assemblies, and support material have been ordered then the project will not be completed. Current items that are placing restrictions on the budget include the frame assembly, radar absorbing foam, switches, and miscellaneous support material (lasers, extension cords, power supplies, etc.).
Mitigation Strategy: To find savings in the budget, the mechanical engineers are performing price comparisons amongst local vendors for a competitive quote for welding the frame assembly as well as lower material cost. Also, to reduce the amount of money spent on the radar absorbing foam, the team will calculate the exact amount of foam required to cover the scene to avoid over purchasing. The switches were the most expensive electronic components. The difference in vendor pricing was dependent upon the delivery lead time. To avoid overspending, the team chose the vendor with the most reasonable lead time in accordance to the semester's scheduled milestones.

7.3 Project Risks

7.3.1.1 Software Development Risk

Description:
During the design process, the software design may be inadequate or incomplete as far as the scope of the project is hoped to reach. This includes generating code that will allow the FPGA to generate pulses, control timing of the switches, and if needed the signal processing of the results recorded. This may delay the testing strategies of the project time line and/or completion of the whole project itself.

Probability: Moderate
The coding level required to generate the pulses and timing for the system is not inherently difficult. The only difficulty that may arise will be just figuring out how to match the correct timing with the physical implementation of the project which could include unknown factors. If the PC cannot be used to do image processing using a program like Labview, then the image processing on the FPGA would be another factor that might be difficult to complete. This is because the FPGA used for the system (Digilent Nexys 3) does not come with image processing software.

Consequence: High
If the pulses and timing cannot be generated properly, then it is very hard to show results from the work of this project. This is a vital portion of the project that must be at least partially working to get some results. These results include anywhere from detecting signal with an RF meter, to having imaging on the VGA display.

Strategy:
If the FPGA cannot be programmed in such a way to generate the signals and the timing required for the SAR system, a very simplified version of the system can be utilized by using test equipment. This new system would include a pulse generator to generate the pulse, and a scope to display the image and that would do the image processing. With this new system the FPGA would not be needed. Overall this is just an extreme backup in case nothing else works for this project. If the PC cannot be used to do the Image processing, then the image processing would have to be done on the FPGA.

8 Conclusion

The testing schedule for the Radar Imager is dependent upon the arrival of the ordered components and should begin Monday, February 22nd. The testing procedures have been laid out and the project is progressing along a steady and traceable critical path. Along the path, the necessary testing procedures have been explicitly defined. The subsystem and full system testing facility has been chosen and CAPS has been very helpful with aiding us in the setup of this location. The area in which we are testing will require the use of anechoic absorbing foam and the details from that test have been laid out. The other subsystem's testing will then be rendered once a successful arrangement of foam has been adequately established. The schedule will depend on the successful completion of the power supply system, additional component order, the DC wire harness, signal processing & image calibration techniques, and chamber support design fabrication.

9 References

[1] CenterPoint Energy, "Humidity & the Indoor Environment," 2006. [Online]. Available: http://www.centerpointenergy.com/staticfiles/CNP/Common/SiteAssets/doc/Humidity_indoor_environ%5B1%5D.pdf. [Accessed 13 October 2014].

[2] Hoffman, "Thermal Management - Heat Dissipation in Electrical Enclosures," PENTAIR - Equipment Protection Solutions, [Online]. Available: http://www.hoffmanonline.com/stream_document.aspx?rRID=233309&pRID=162533. [Accessed January 2015].

10 Appendices

10.1 Signal Processing Example

In the following example for signal processing, the start value for θ is -9° and the end value is 9°, and in order to make it symmetrical for sixteen points, an increment of 1.2 was found. The following Table 28 shows each value for angle θ, both in degrees and radians.

Table 28. Values for the Sixteen Angles

	Degrees	**Radians**
θ_1	-9	-0.1571
θ_2	-7.8	-0.1361
θ_3	-6.6	-0.1152
θ_4	-5.4	-0.0942
θ_5	-4.2	-0.0733
θ_6	-3	-0.0524
θ_7	-1.8	-0.0314
θ_8	-0.6	-0.0105
θ_9	0.6	0.01047
θ_{10}	1.8	0.03142
θ_{11}	3	0.05236
θ_{12}	4.2	0.0733
θ_{13}	5.4	0.09425
θ_{14}	6.6	0.11519
θ_{15}	7.8	0.13614
θ_{16}	9	0.15708

The spacing between phase centers in radians was found to be $d = 6\pi \approx 18.85$. By replacing these values into the equations, the following Table 29 for the basis functions can be found.

Table 29. Basis Functions for the Sixteen Angles

	1*d*sin(θn)	**2*d*sin(θn)**	**3*d*sin(θn)**	**4*d*sin(θn)**	**…**	**16*d*sin(θn)**
f(θ1)	-2.9487202	-5.89744039	-8.84616059	-11.7948808	…	-47.1795231
f(θ2)	-2.55817827	-5.11635654	-7.67453482	-10.2327131	…	-40.9308524
f(θ3)	-2.16651425	-4.33302849	-6.49954274	-8.66605698	…	-34.6642279
f(θ4)	-1.77389991	-3.54779983	-5.32169974	-7.09559966	…	-28.3823986
f(θ5)	-1.38050749	-2.76101498	-4.14152248	-5.52202997	…	-22.0881199
f(θ6)	-0.98650953	-1.97301907	-2.9595286	-3.94603814	…	-15.7841525
f(θ7)	-0.59207886	-1.18415772	-1.77623658	-2.36831544	…	-9.47326176
f(θ8)	-0.19738848	-0.39477696	-0.59216544	-0.78955392	…	-3.15821568
f(θ9)	0.19738848	0.39477696	0.59216544	0.78955392	…	3.15821568
f(θ10)	0.59207886	1.18415772	1.77623658	2.36831544	…	9.47326176

f(θ11)	0.98650953	1.97301907	2.9595286	3.94603814	…	15.7841525
f(θ12)	1.38050749	2.76101498	4.14152248	5.52202997	…	22.0881199
f(θ13)	1.77389991	3.54779983	5.32169974	7.09559966	…	28.3823986
f(θ14)	2.16651425	4.33302849	6.49954274	8.66605698	…	34.6642279
f(θ15)	2.55817827	5.11635654	7.67453482	10.2327131	…	40.9308524
f(θ16)	2.9487202	5.89744039	8.84616059	11.7948808	…	47.1795231

In Figure 46, it can be seen how each of these functions for each angle θ is linear with different slopes.

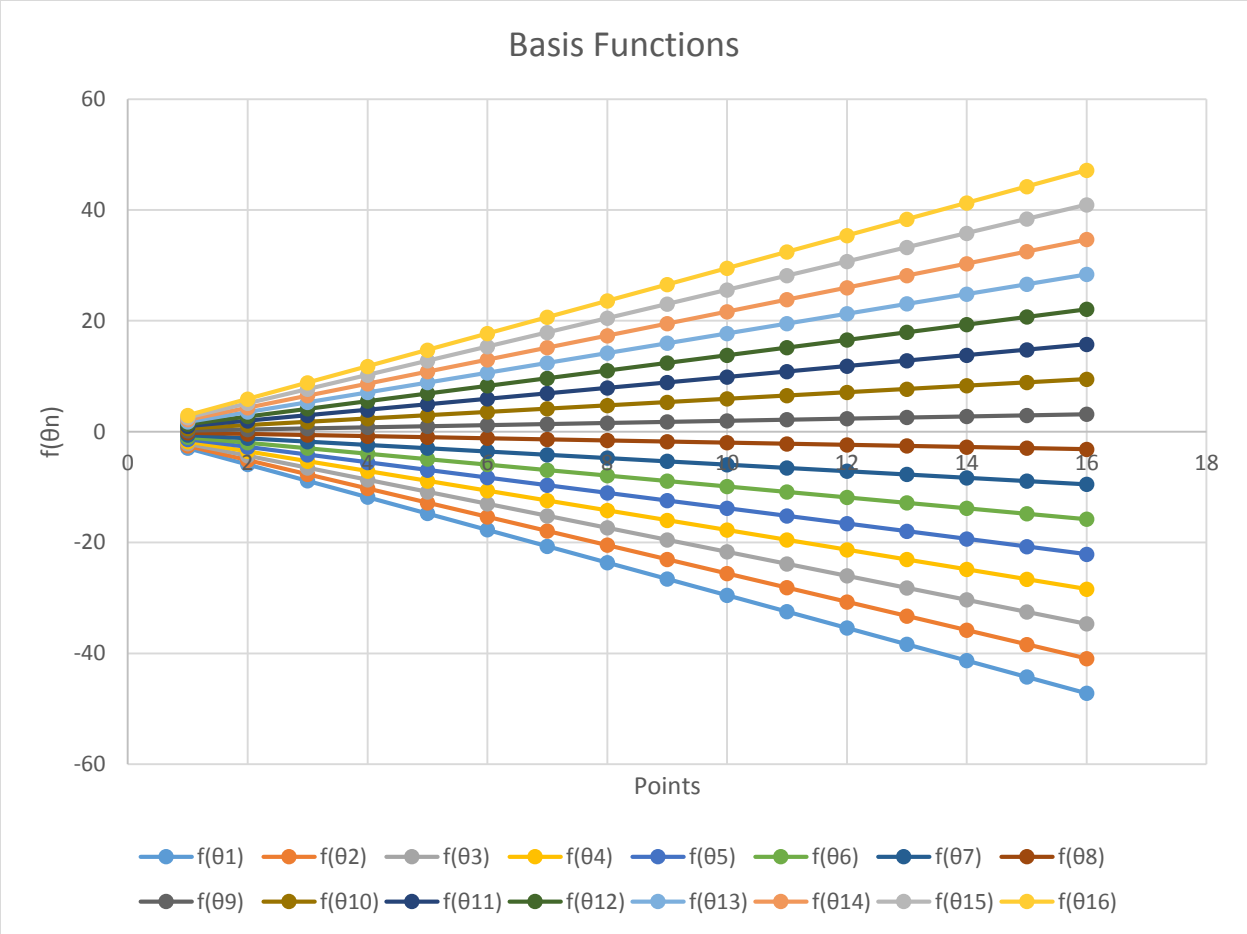


Figure 46. Linear Phase Slope for each function

Each of the functions are then broken into real and imaginary parts. The real part of the basis functions is shown in Table 30, while the imaginary part is shown in Table 31.

Table 30. Real Part of Basis Functions

	cos(1*d*sin(θn))	**cos(2*d*sin(θn))**	**cos(3*d*sin(θn))**	**cos(4*d*sin(θn))**	**…**	**cos(16*d*sin(θn))**
f(realθ_1)	-0.981457696	0.926518416	-0.837219564	0.716872752	…	-0.998452865
f(realθ_2)	-0.834586615	0.393069636	0.178485301	-0.690992523	…	-0.995939433
f(realθ_3)	-0.561103153	-0.370326502	0.97668589	-0.725716563	…	-0.994312023
f(realθ_4)	-0.201710092	-0.918626078	0.572302393	0.687747742	…	-0.994166685
f(realθ_5)	0.189142524	-0.928450211	-0.540361356	0.72403959	…	-0.995301966
f(realθ_6)	0.551604633	-0.391464659	-0.983472071	-0.693510842	…	-0.997099001
f(realθ_7)	0.829782288	0.37707729	-0.203998174	-0.715625434	…	-0.998824891
f(realθ_8)	0.980582064	0.923082369	0.829733965	0.704162119	…	-0.999861841
f(realθ_9)	0.980582064	0.923082369	0.829733965	0.704162119	…	-0.999861841
f(realθ_{10})	0.829782288	0.37707729	-0.203998174	-0.715625434	…	-0.998824891
f(realθ_{11})	0.551604633	-0.391464659	-0.983472071	-0.693510842	…	-0.997099001
f(realθ_{12})	0.189142524	-0.928450211	-0.540361356	0.72403959	…	-0.995301966
f(realθ_{13})	-0.201710092	-0.918626078	0.572302393	0.687747742	…	-0.994166685
f(realθ_{14})	-0.561103153	-0.370326502	0.97668589	-0.725716563	…	-0.994312023
f(realθ_{15})	-0.834586615	0.393069636	0.178485301	-0.690992523	…	-0.995939433
f(realθ_{16})	-0.981457696	0.926518416	-0.837219564	0.716872752	…	-0.998452865

Table 31. Imaginary Part of Basis Functions

	sin(1*d*sin(θn))	**sin(2*d*sin(θn))**	**sin(3*d*sin(θn))**	**sin(4*d*sin(θn))**	**…**	**sin(16*d*sin(θn))**
f(imagθ_1)	-0.191678877	0.376249417	-0.546866895	0.697204028	…	0.055604652
f(imagθ_2)	-0.550876739	0.919508707	-0.983942578	0.722861905	…	0.090025806
f(imagθ_3)	-0.827745886	0.928901653	-0.214673408	-0.687993801	…	0.106506346
f(imagθ_4)	-0.979445271	0.395127991	0.820042664	-0.725949753	…	0.107854544
f(imagθ_5)	-0.981949645	-0.371456868	0.841433066	0.689758416	…	0.096819397
f(imagθ_6)	-0.834105706	-0.920193143	-0.181059895	0.72044619	…	0.076115585
f(imagθ_7)	-0.558087229	-0.926181795	-0.978971269	-0.698484243	…	0.048464803
f(imagθ_8)	-0.196109193	-0.384602315	-0.55815907	-0.710039231	…	0.016622266
f(imag$\theta_{9)}$	0.196109193	0.384602315	0.55815907	0.710039231	…	-0.016622266
f(imagθ_{10})	0.558087229	0.926181795	0.978971269	0.698484243	…	-0.048464803
f(imagθ_{11})	0.834105706	0.920193143	0.181059895	-0.72044619	…	-0.076115585
f(imagθ_{12})	0.981949645	0.371456868	-0.841433066	-0.689758416	…	-0.096819397
f(imagθ_{13})	0.979445271	-0.395127991	-0.820042664	0.725949753	…	-0.107854544
f(imagθ_{14})	0.827745886	-0.928901653	0.214673408	0.687993801	…	-0.106506346
f(imagθ_{15})	0.550876739	-0.919508707	0.983942578	-0.722861905	…	-0.090025806

f(imagθ_{16})	0.191678877	-0.376249417	0.546866895	-0.697204028	…	-0.055604652

In Figure 47 shown below, each row for the sixteen points for each of the sixteen real parts of the basis functions have been plotted out and graphed, and in Figure 48, each row the sixteen points for each of the sixteen imaginary parts of the basis functions have been plotted out and graphed. As can be seen, they are both sinusoidal functions of different frequencies, and the imaginary part is 90° out of phase with the real part.

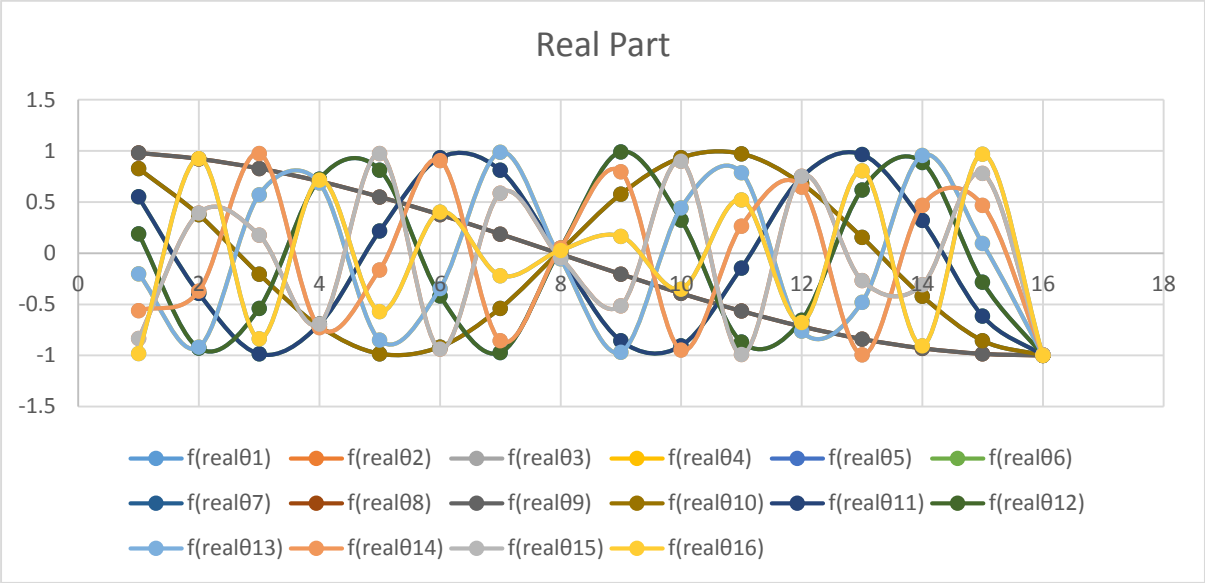


Figure 47. Real Part of the Basis Functions

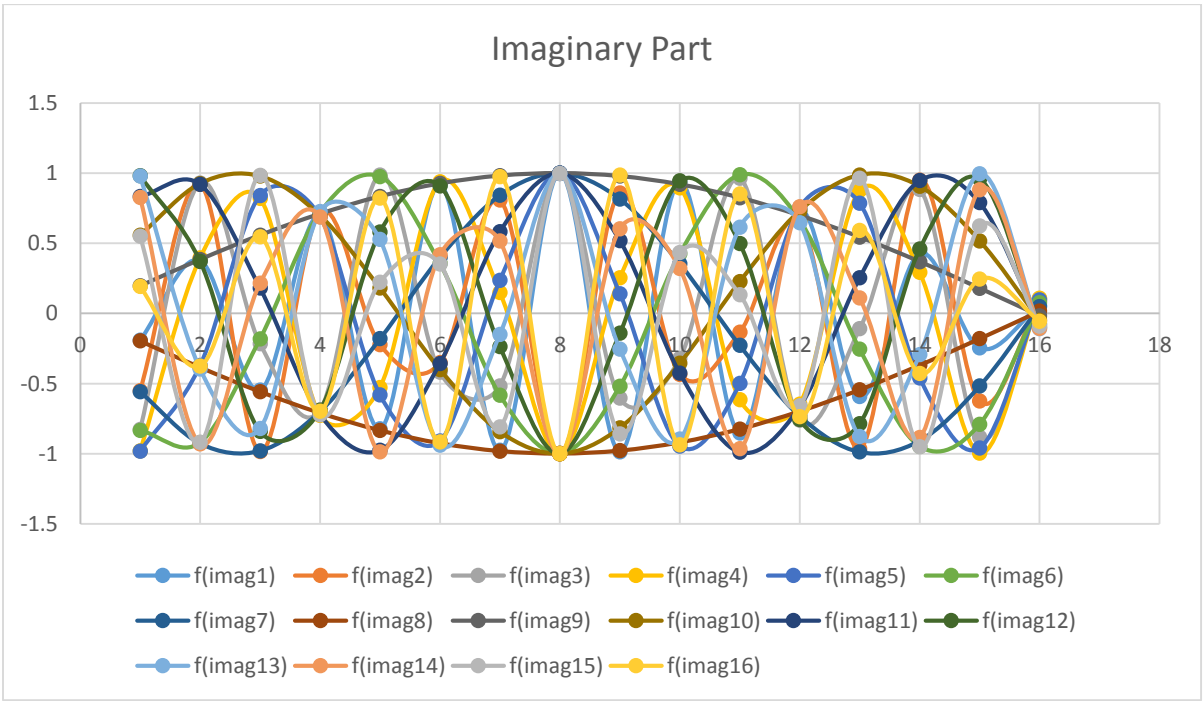


Figure 48. Imaginary Part of Basis Functions

In Table 32 shown below, the calibration data that was calculated from the image processing calibration is used. The error column is the calibration error that was calculated from the image processing calibration. The values for I_{error} are obtained by calculating the cosine of the error, while those of Q_{error} are obtained by calculating the sine of the error. These are calculated in order to get the phase error on the date by taking the error times the ideal phase return. To calculate the values of $I_{combined}$, the following was realized:

$$I_{combined,1} = \left(R_{1,\theta 1} \times I_{error,1}\right) - \left(I_{1,\theta 1} \times Q_{error,1}\right)$$
$$I_{combined,1} = \left[f\left(real\theta_{1,1}\right) \times I_{error,1}\right] - \left[f\left(imag\theta_{1,1}\right) \times Q_{error,1}\right]$$
$$I_{combined,1} = [(-0.981457696) \times (0.97351)] - [(-0.191678877) + (-0.2287)]$$
$$= -0.9993$$

To calculate the values of $Q_{combined}$, the following was realized:

$$Q_{combined,1} = \left(R_{1,\theta 1} \times Q_{error,1}\right) + \left(I_{1,\theta 1} \times I_{error,1}\right)$$
$$Q_{combined,1} = \left[f\left(real\theta_{1,1}\right) \times Q_{error,1}\right] + \left[f\left(imag\theta_{1,1}\right) \times I_{error,1}\right]$$
$$Q_{combined,1} = [(-0.981457696) \times (-0.2287)] + [(-0.191678877) + (0.97351)]$$
$$= 0.03782$$

Table 32. I and Q Error Data from Calibration

Error (degrees)	**I_{error} =cos(error)**	**Q_{error} =sin(error)**	**$I_{combined}$**	**$Q_{combined}$**
-13.2183	0.97351	-0.2287	-0.9993	0.03782
-10.0876	0.98454	-0.1752	0.9781	0.20815
-8.41575	0.98923	-0.1464	-0.9082	-0.4184
-7.78614	0.99078	-0.1355	0.80472	0.59366
-7.76778	0.99082	-0.1352	-0.6758	-0.7371
-7.92085	0.99046	-0.1378	0.52423	0.85158
-7.80226	0.99074	-0.1358	-0.3493	-0.937
-6.97141	0.99261	-0.1214	0.14893	0.98885
-3.91578	0.99767	-0.0683	0.09656	-0.9953
-0.78507	0.99991	-0.0137	-0.3375	0.94134
0.88674	0.99988	0.01548	0.53649	-0.8439
1.51636	0.99965	0.02646	-0.6962	0.71781
1.53471	0.99964	0.02678	0.8211	-0.5708
1.38164	0.99971	0.02411	-0.9142	0.40526
1.50024	0.99966	0.02618	0.97539	-0.2205
2.33108	0.99917	0.04067	-0.9999	0.01495

For this example, there is energy coming in from angles θ_4, θ_8, and θ_{13}, so the data from the demodulator would reflect this information. The I data would be the sum of the real part of the basis functions for those angles, which would be the sum of each of the sixteen points of f(realθ_4), f(realθ_8), f(realθ_{13}), and the value of $I_{combined,1}$, while the Q data would be the sum of the imaginary

part of the basis functions for those angles and the value of $Q_{combined,1}$. Each column of Table 33 shows the I data that sums each of the points for the real part at the specified angles for the corresponding column, while each column Table 34 shows the Q data that sums each of the points for the imaginary part at the specified angles for the corresponding column. For example, for column 1 in Table 33 below, it shows the following sum for f($I\theta_1$) through f($I\theta_{16}$):

$$f(I\theta_{n,1}) = (\cos(1 * d * \sin(\theta_4))) + (\cos(1 * d * \sin(\theta_8))) + (\cos(1 * d * \sin(\theta_{13}))) + I_{combined,1}$$

$$f(I\theta_{n,1}) = (-0.2017101) + (0.98058206) + (-0.2017101) + (-0.9993) = -0.422123$$

The same is done for column 1 in Table 33 below, which shows the following sum for f($Q\theta_1$) through f($Q\theta_{16}$), except with the imaginary part:

$$f(Q\theta_{n,1}) = (\sin(1 * d * \sin(\theta_4))) + (\sin(1 * d * \sin(\theta_8))) + (\sin(1 * d * \sin(\theta_{13}))) + Q_{combined,1}$$

$$f(Q\theta_{n,1}) = (-0.97944527) + (-0.19610919) + (0.97944527) + (0.03782) = -0.158288$$

Table 33. I data with Energy from θ_4, θ_8, and θ_{13}

	1	2	3	4	…	16
f($I\theta_1$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_2$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_3$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_4$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_5$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_6$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_7$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_8$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_9$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{10}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{11}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{12}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{13}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{14}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{15}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{16}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083

Table 34. Q data with Energy from θ_4, θ_8, and θ_{13}

	1	2	3	4	…	16
f(Qθ$_1$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_2$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_3$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_4$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_5$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_6$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_7$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_8$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_9$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{10}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{11}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{12}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{13}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{14}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{15}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{16}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157

Now that there is data for the I channel and the Q channel at the angles specified, they will be used to perform a complex multiplication for each of the points for the sixteen angles. Table 35 shows the results of the complex multiply realized for each point for the real part. For example, for point 1 of f(realcompθ_1), which is the complex multiply for the real part of θ_1, the following was performed:

$$f(realcomp\theta_{1,1}) = (R_{1,\theta 1} \times I_{1d}) + (I_{1,\theta 1} \times Q_{1d})$$
$$f(realcomp\theta_{1,1}) = [f(real\theta_{1,1}) \times f(I\theta_{1,1})] + [f(imag\theta_{1,1}) \times f(Q\theta_{1,1})]$$
$$f(realcomp\theta_{1,1}) = [(-0.981457696)(-0.422123)] + [(-0.19167888)(-0.158288)]$$
$$= 0.44463604$$

Table 35. Real Part after Complex Multiply

	1	2	3	4	…	16
f(realcompθ$_1$)	0.44463604	-0.007160336	-0.358484174	1.986588305	…	3.983668821
f(realcompθ$_2$)	0.439495233	-0.137121243	1.151207091	-2.077210003	…	3.974731723
f(realcompθ$_3$)	0.367876803	-0.187580296	1.250893807	-2.013169082	…	3.968761765
f(realcompθ$_4$)	0.240181082	-0.128446106	-0.190728505	2.068210205	…	3.968224709
f(realcompθ$_5$)	0.075589753	0.006191188	-1.397826607	2.008126692	…	3.972403926
f(realcompθ$_6$)	-0.100815673	0.137344615	-0.871652971	-2.084192635	…	3.97891703
f(realcompθ$_7$)	-0.261931246	0.18753193	0.738587381	-1.982841577	…	3.984927088
f(realcompθ$_8$)	-0.382884119	0.126873709	1.42967892	2.113703737	…	3.988057261

f(realcompθ_9)	-0.444967683	-0.008853876	0.339475788	1.94843228	…	3.98700773
f(realcompθ_{10})	-0.438608554	-0.139321065	-1.173551291	-2.145423451	…	3.981867019
f(realcompθ_{11})	-0.364873947	-0.187394963	-1.225301375	-1.916498815	…	3.97411109
f(realcompθ_{12})	-0.23527244	-0.124897321	0.245670763	2.168677509	…	3.966290747
f(realcompθ_{13})	-0.069888284	0.010996029	1.410988871	1.899235353	…	3.961414769
f(realcompθ_{14})	0.105831899	0.140232547	0.831591077	-2.17330916	…	3.962036951
f(realcompθ_{15})	0.265100597	0.187376794	-0.770641603	-1.908953891	…	3.969047491
f(realcompθ_{16})	0.38395501	0.125619481	-1.426631292	2.148872191	…	3.980157941

Table 36 shows the results of the complex multiply realized for each point for the imaginary part. For example, for point 1 of f(realcompθ_1), which is the complex multiply for the real part of θ_1, the following was performed:

$$f(imagcomp\theta_{1,1}) = (-I_{1,\theta 1} \times I_{1d}) + (R_{1,\theta 1} \times Q_{1d})$$
$$f(imagcomp\theta_{1,1}) = [(-f(imag\theta_{1,1})) \times f(I\theta_{1,1})] + [f(real\theta_{1,1}) \times f(Q\theta_{1,1})]$$
$$f(imagcomp\theta_{1,1}) = [(-(-0.19167888))(-0.422123)] + [(-0.981457696)(-0.158288)] = 0.074441231$$

Table 36. Imaginary Part after Complex Multiply

	1	2	3	4	…	16
f(imagcompθ_1)	0.074441231	-0.187538404	1.400647215	-2.094429289	…	0.190234821
f(imagcompθ_2)	-0.100432291	-0.12813933	0.874668942	-2.004586177	…	0.327588605
f(imagcompθ_3)	-0.260594249	0.005962873	-0.724974625	2.068892793	…	0.393365752
f(imagcompθ_4)	-0.381517697	0.136833917	-1.433159503	2.013870325	…	0.398747068
f(imagcompθ_5)	-0.444442228	0.187572899	-0.369329528	-2.073787435	…	0.354702139
f(imagcompθ_6)	-0.439407448	0.127899882	1.153492359	-1.997325261	…	0.272076878
f(imagcompθ_7)	-0.366926052	-0.007327935	1.242904745	2.097976744	…	0.161748763
f(imagcompθ_8)	-0.237996757	-0.138293114	-0.21527125	1.966068068	…	0.034725329
f(imagcompθ_9)	-0.072432492	-0.187466083	-1.405375293	-2.129971546	…	-0.097856637
f(imagcompθ_{10})	0.10423647	-0.125744041	-0.844453013	-1.931405021	…	-0.224814598
f(imagcompθ_{11})	0.264782378	0.010249449	0.767437335	2.158749506	…	-0.33503374
f(imagcompθ_{12})	0.384564148	0.140080629	1.424769946	1.905257201	…	-0.417545536
f(imagcompθ_{13})	0.445374374	0.187352637	0.315331461	-2.17395313	…	-0.461518783
f(imagcompθ_{14})	0.438226328	0.124726725	-1.182700218	-1.899972219	…	-0.456146644
f(imagcompθ_{15})	0.364642809	-0.010576405	-1.223288618	2.16542425	…	-0.390472252
f(imagcompθ_{16})	0.236265222	-0.139433386	0.234620292	1.927567235	…	-0.253277166

The sum column of Table 37 shows the sum of all the points for each of the functions for the real part after the complex multiply, while the amplitude column shows the squared value of the sum column and corresponds to the amplitude at that angle for the real part.

Table 37. Amplitude for the Real Part of the Sixteen Functions

	Sum	Amplitude
$\mathbf{f(re\theta_1)}$	15.772399	248.76857
$\mathbf{f(re\theta_2)}$	-1.006651	1.0133455
$\mathbf{f(re\theta_3)}$	-0.327206	0.1070634
$\mathbf{f(re\theta_4)}$	15.731508	247.48035
$\mathbf{f(re\theta_5)}$	-0.10471	0.0109643
$\mathbf{f(re\theta_6)}$	0.0179447	0.000322
$\mathbf{f(re\theta_7)}$	0.0911412	0.0083067
$\mathbf{f(re\theta_8)}$	16.070567	258.26313
$\mathbf{f(re\theta_9)}$	0.1798936	0.0323617
$\mathbf{f(re\theta_{10})}$	0.1854129	0.0343779
$\mathbf{f(re\theta_{11})}$	0.1733442	0.0300482
$\mathbf{f(re\theta_{12})}$	0.1410176	0.019886
$\mathbf{f(re\theta_{13})}$	16.091311	258.9303
$\mathbf{f(re\theta_{14})}$	0.0916746	0.0084042
$\mathbf{f(re\theta_{15})}$	-0.067137	0.0045074
$\mathbf{f(re\theta_{16})}$	0.4089471	0.1672378

The sum column of Table 38 shows the sum of all the points for each of the functions for the imaginary part after the complex multiply, while the amplitude column shows the squared value of the sum column and corresponds to the amplitude at that angle for the imaginary part.

Table 38. Amplitude for the Imaginary Part of the Sixteen Functions

	Sum	Amplitude
$\mathbf{f(im\theta_1)}$	-1.068907	1.1425626
$\mathbf{f(im\theta_2)}$	0.3490256	0.1218189
$\mathbf{f(im\theta_3)}$	0.1009696	0.0101949
$\mathbf{f(im\theta_4)}$	0.3704309	0.137219
$\mathbf{f(im\theta_5)}$	0.2885457	0.0832586
$\mathbf{f(im\theta_6)}$	0.2944188	0.0866825
$\mathbf{f(im\theta_7)}$	0.2184722	0.0477301
$\mathbf{f(im\theta_8)}$	0.1627602	0.0264909
$\mathbf{f(im\theta_9)}$	0.0823559	0.0067825
$\mathbf{f(im\theta_{10})}$	0.0201988	0.000408
$\mathbf{f(im\theta_{11})}$	-0.05388	0.002903
$\mathbf{f(im\theta_{12})}$	-0.08327	0.0069339
$\mathbf{f(im\theta_{13})}$	-0.153013	0.0234131
$\mathbf{f(im\theta_{14})}$	-0.109271	0.0119401

f(imθ_{15})	-0.307563	0.0945951
f(imθ_{16})	-0.04602	0.0021179

The following Table 39 shows each amplitude that correspond to each of the corresponding sixteen angles by using Equation 20 in which $real_{\theta n}$ represents the amplitude for the real part and $imag_{\theta n}$ represents the amplitude for the imaginary part.

$$A_n = 20 \times \log[(real_{\theta n} + imag_{\theta n})^{1/2}]$$

Equation 20: Amplitude Calculation for Each Angle

Table 39. Corresponding Amplitudes for each Angle

Amplitude	Theta
23.977856	-9
0.5505877	-7.8
-9.308564	-6.6
23.937815	-5.4
-10.25844	-4.2
-10.60458	-3
-12.51527	-1.8
24.12107	-0.6
-14.07332	0.6
-14.58596	1.8
-14.82128	3
-15.71543	4.2
24.132221	5.4
-16.91556	6.6
-10.03916	7.8
-7.712004	9

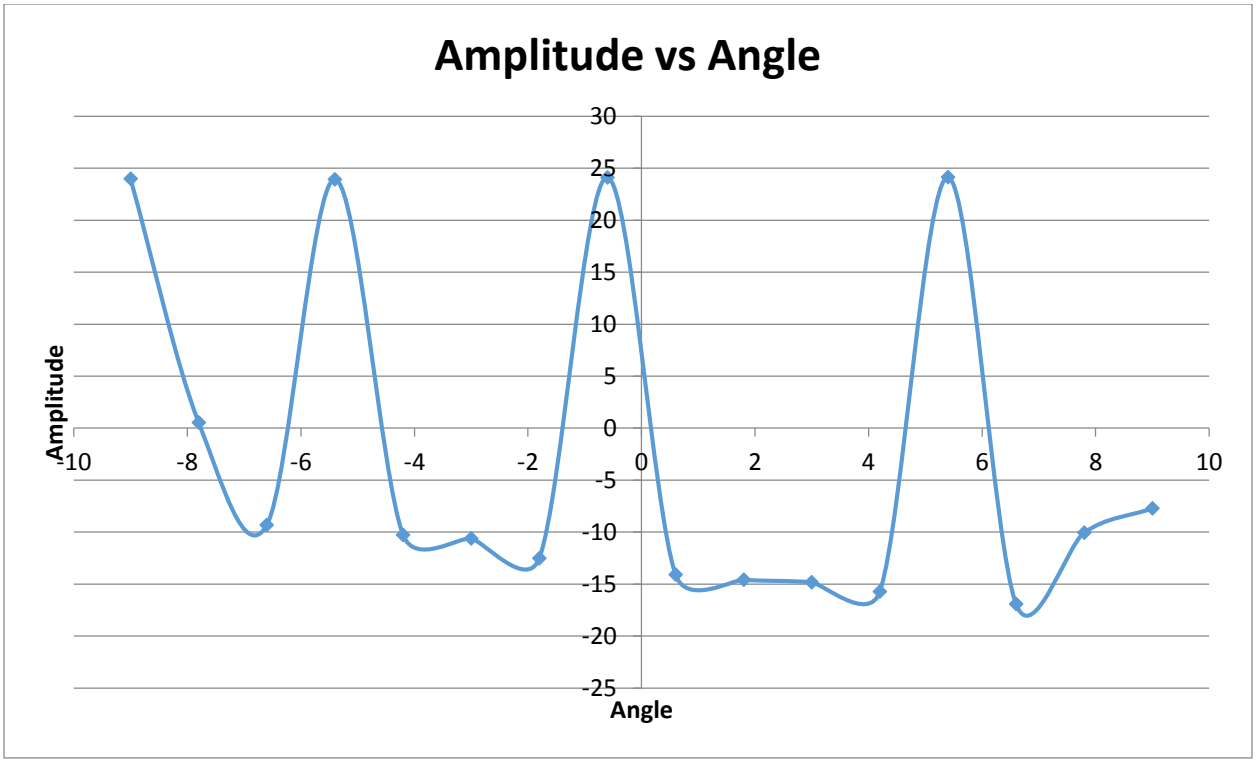


Figure 49. Amplitude vs Angle Graph

Figure 49 shows the graph for the amplitude vs angle that were obtained from all the calculations realized. It is basically the one-dimensional image, which tells the used where the energy is coming in from different angles in the scene. Since there was energy coming in at three different angles for this example, each of the three peaks of the figure represents that information. When forming the image out of the three peaks, the display would have three strikes across it, informing the user that there is energy coming in from those three angles.

10.2 SAR - 1

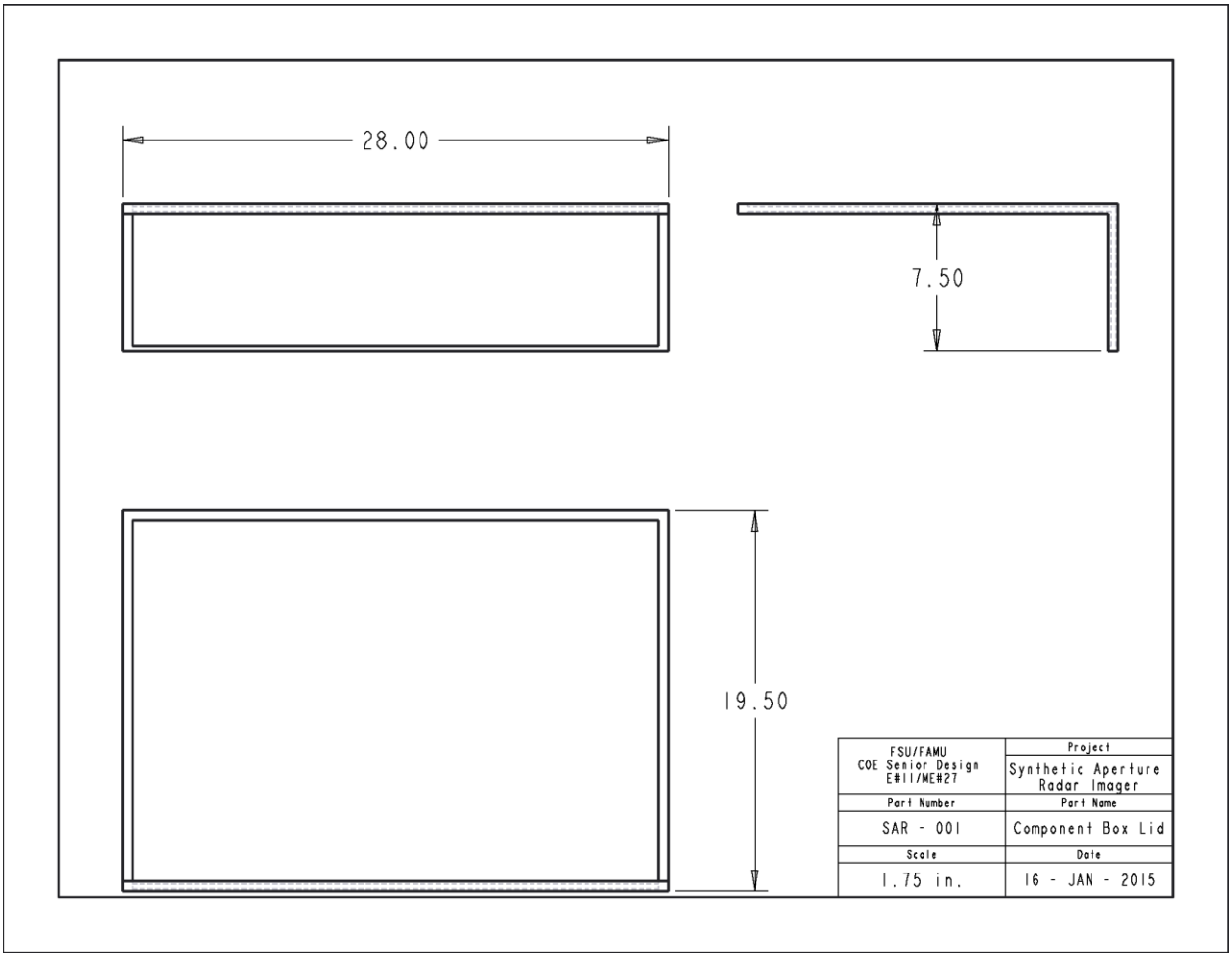


Figure 50: Plexiglas Lid

10.3 SAR – 2

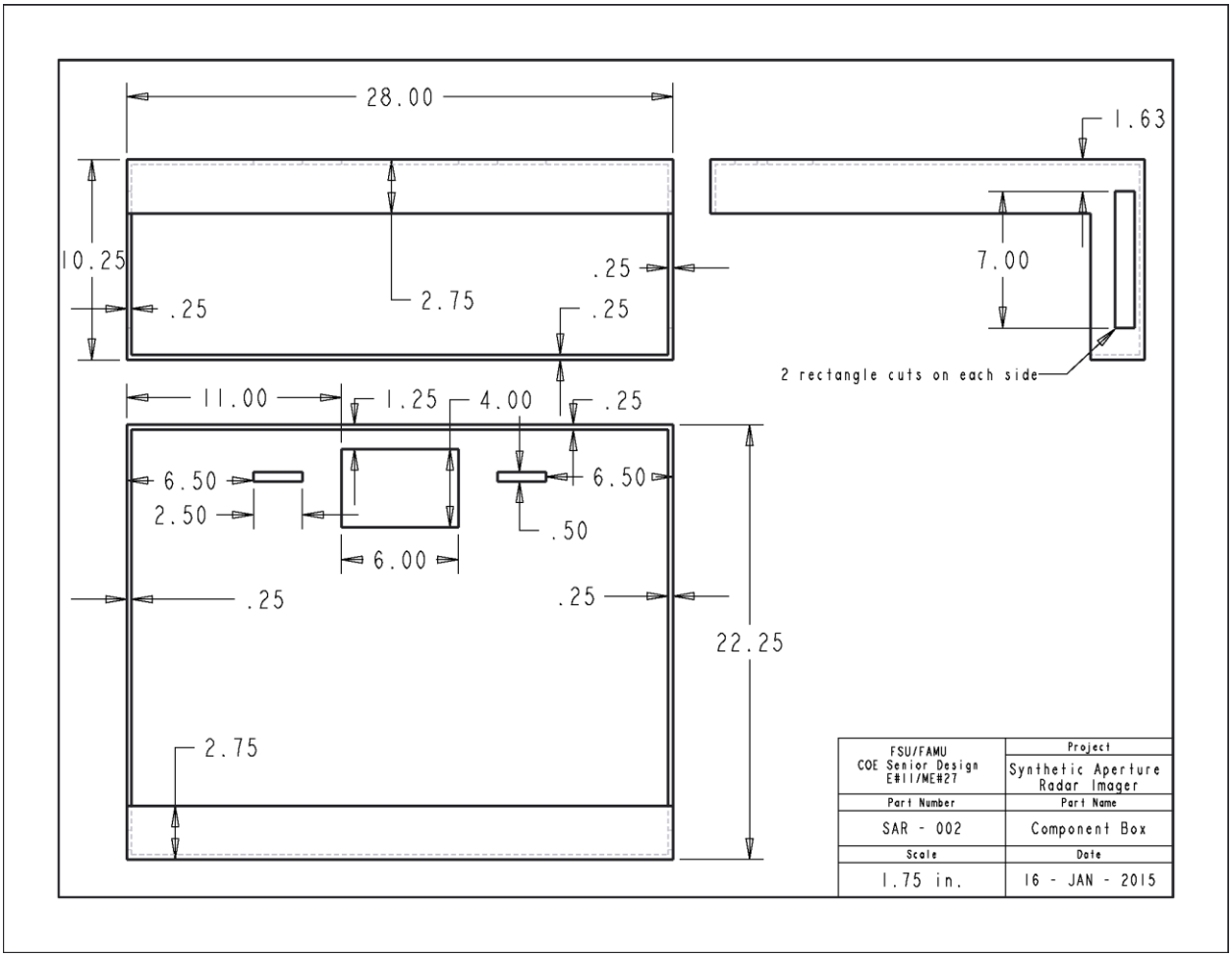


Figure 51: Component Box

10.4 SAR – 3

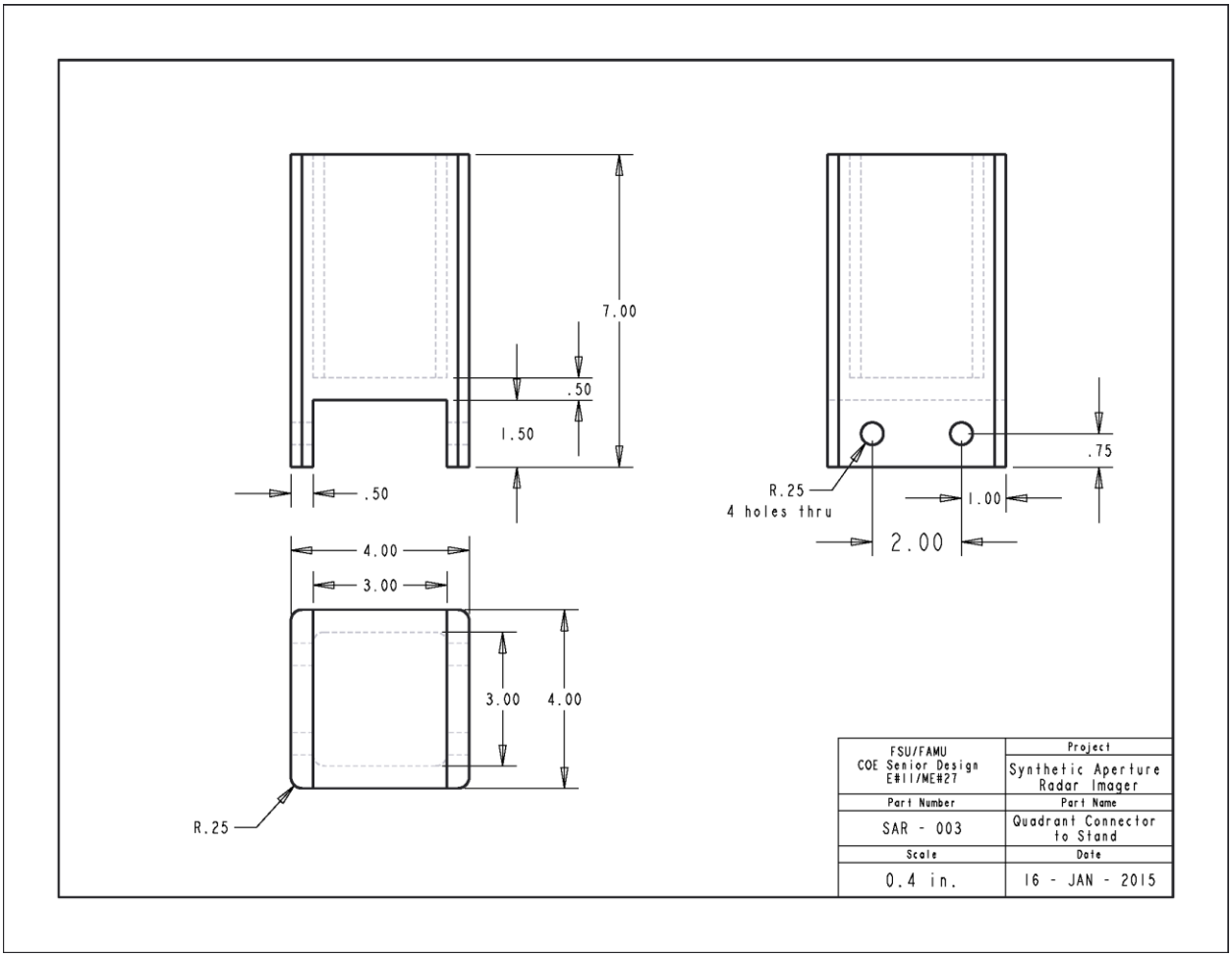


Figure 52: Quadrant Connector to Stand

10.5 SAR – 4

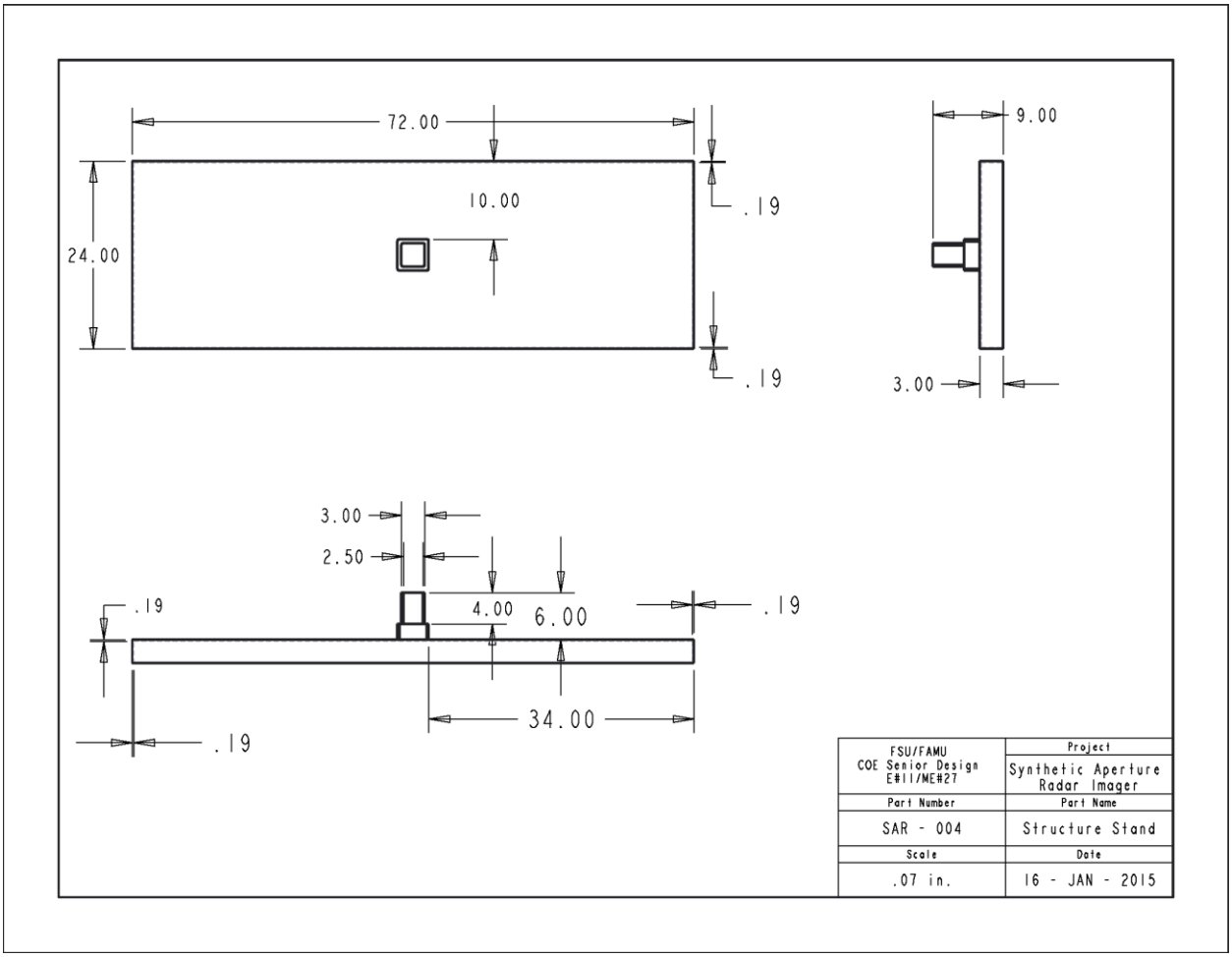


Figure 53: Structure Stand

10.6 SAR – 5

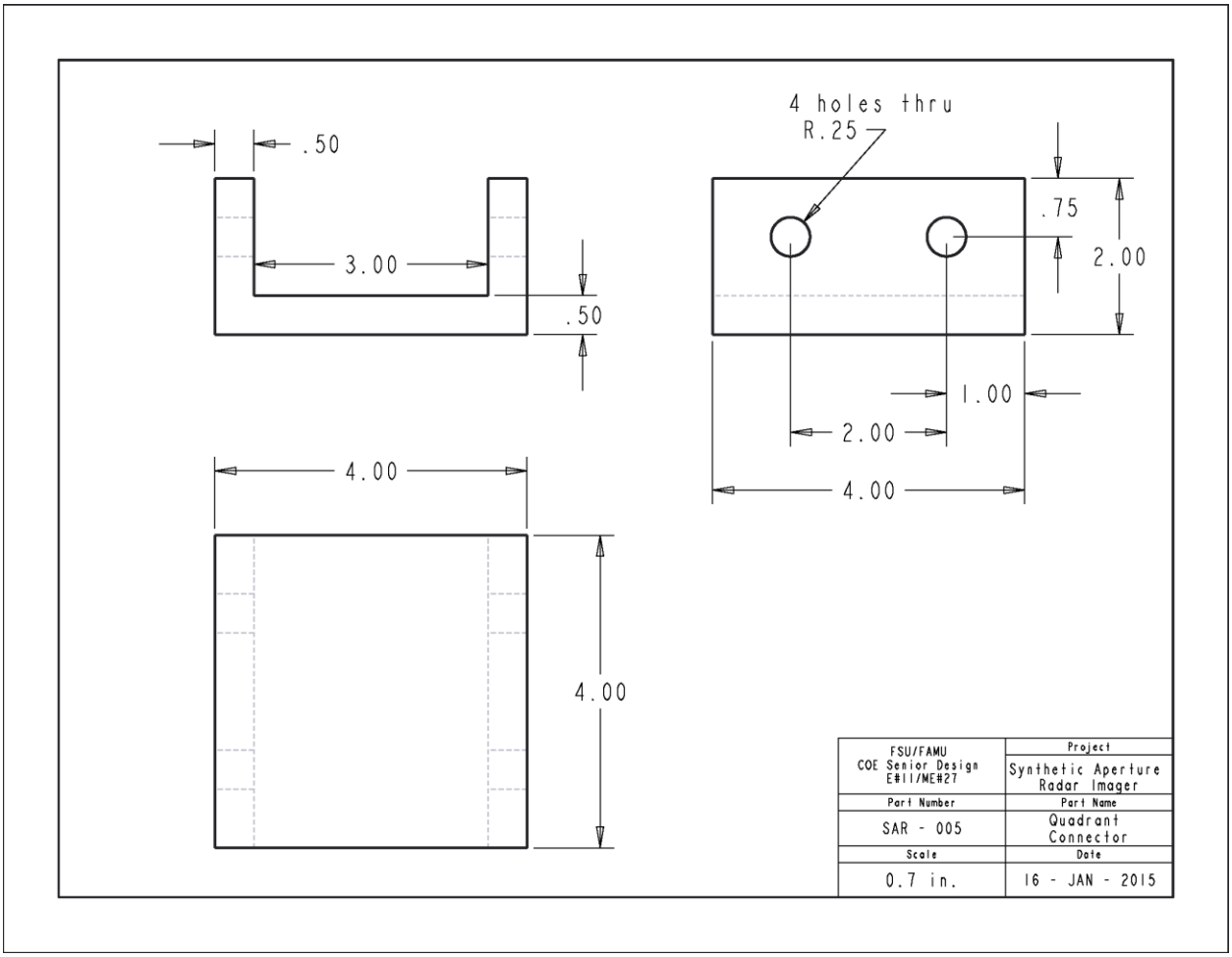


Figure 54: Quadrant Connector

10.7 SAR -6

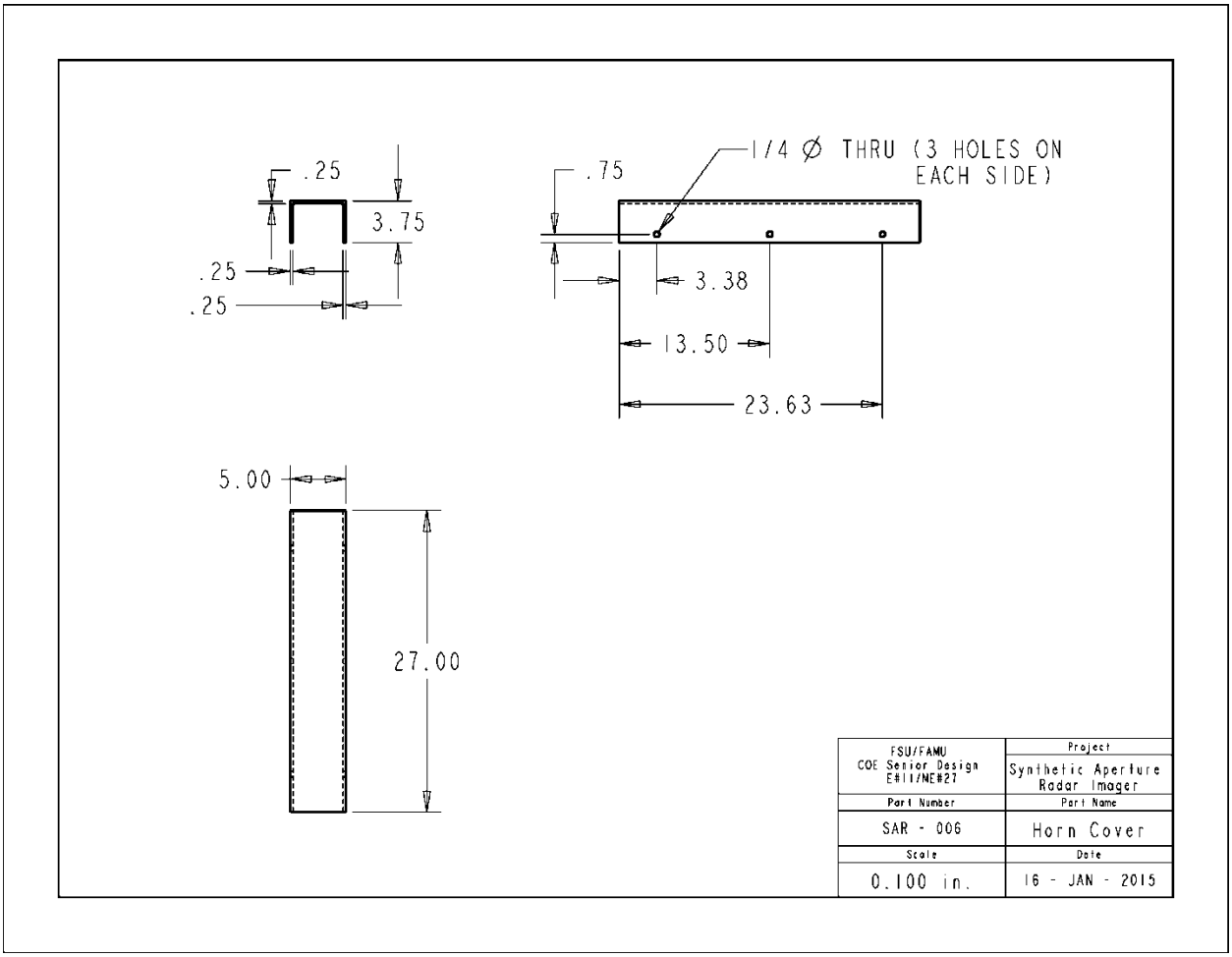


Figure 55: Horn Cover

10.8 SAR – 7

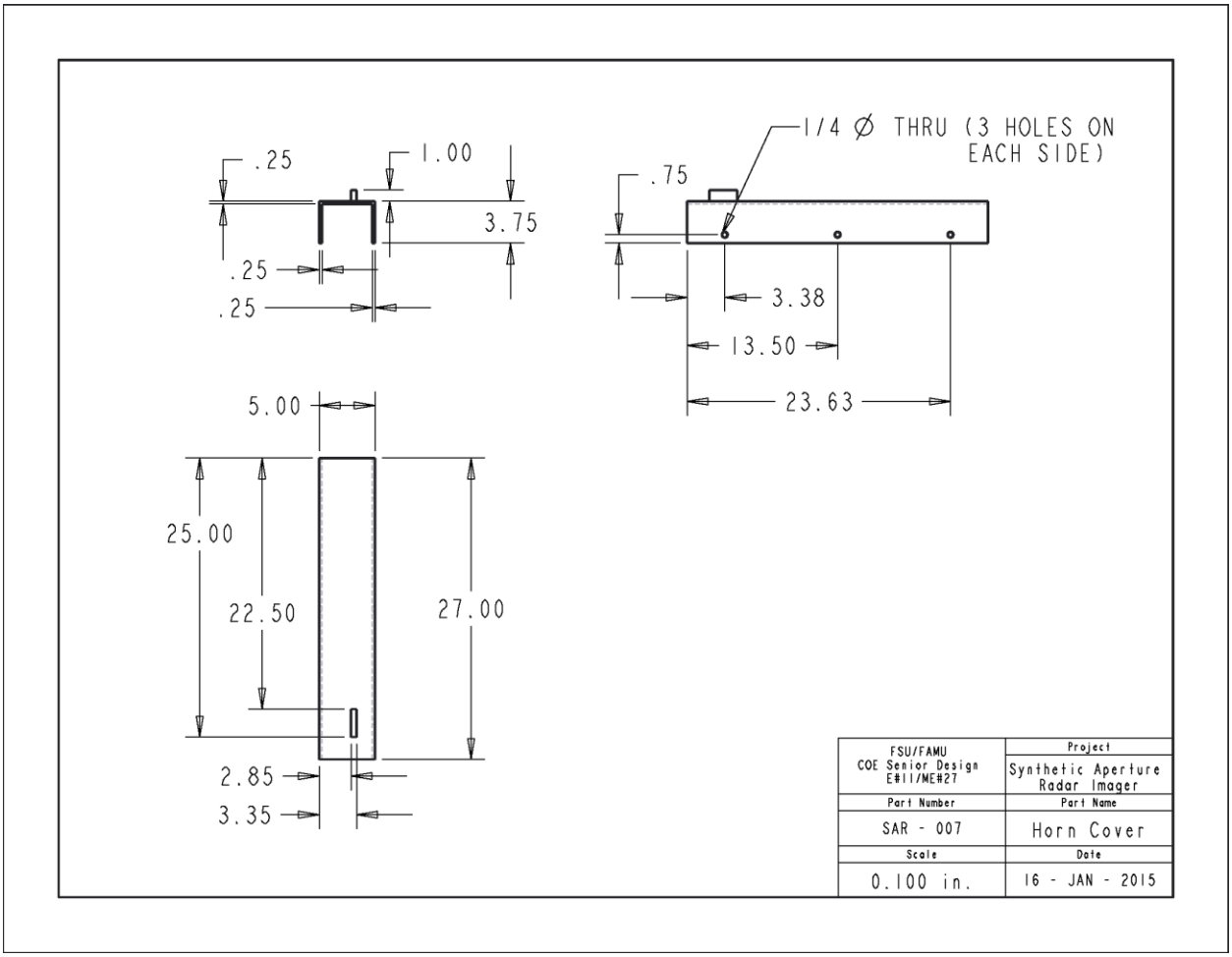


Figure 56: Horn Cover (2)

10.9 SAR – 8

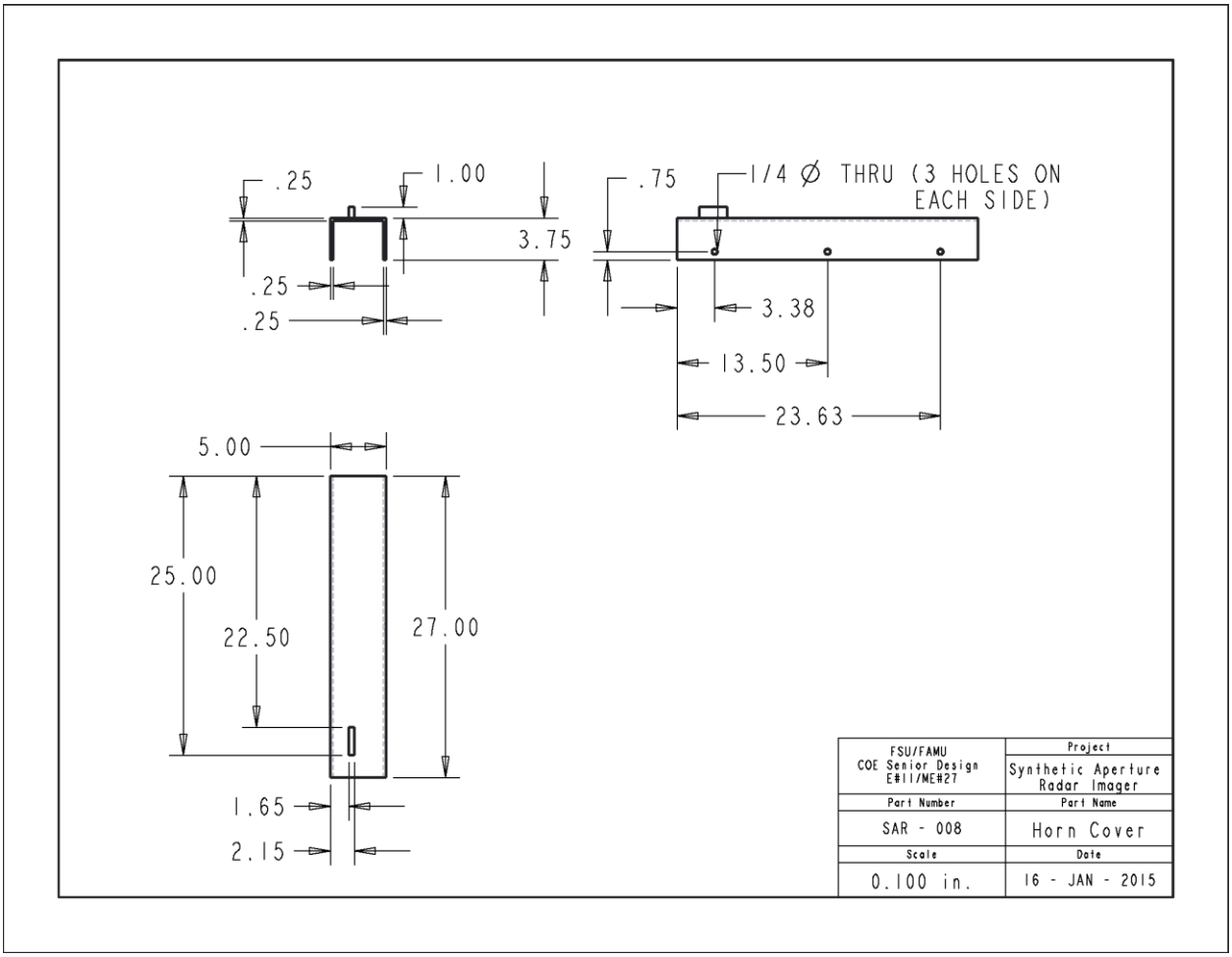


Figure 57: Horn Cover (3)

SAR – 9

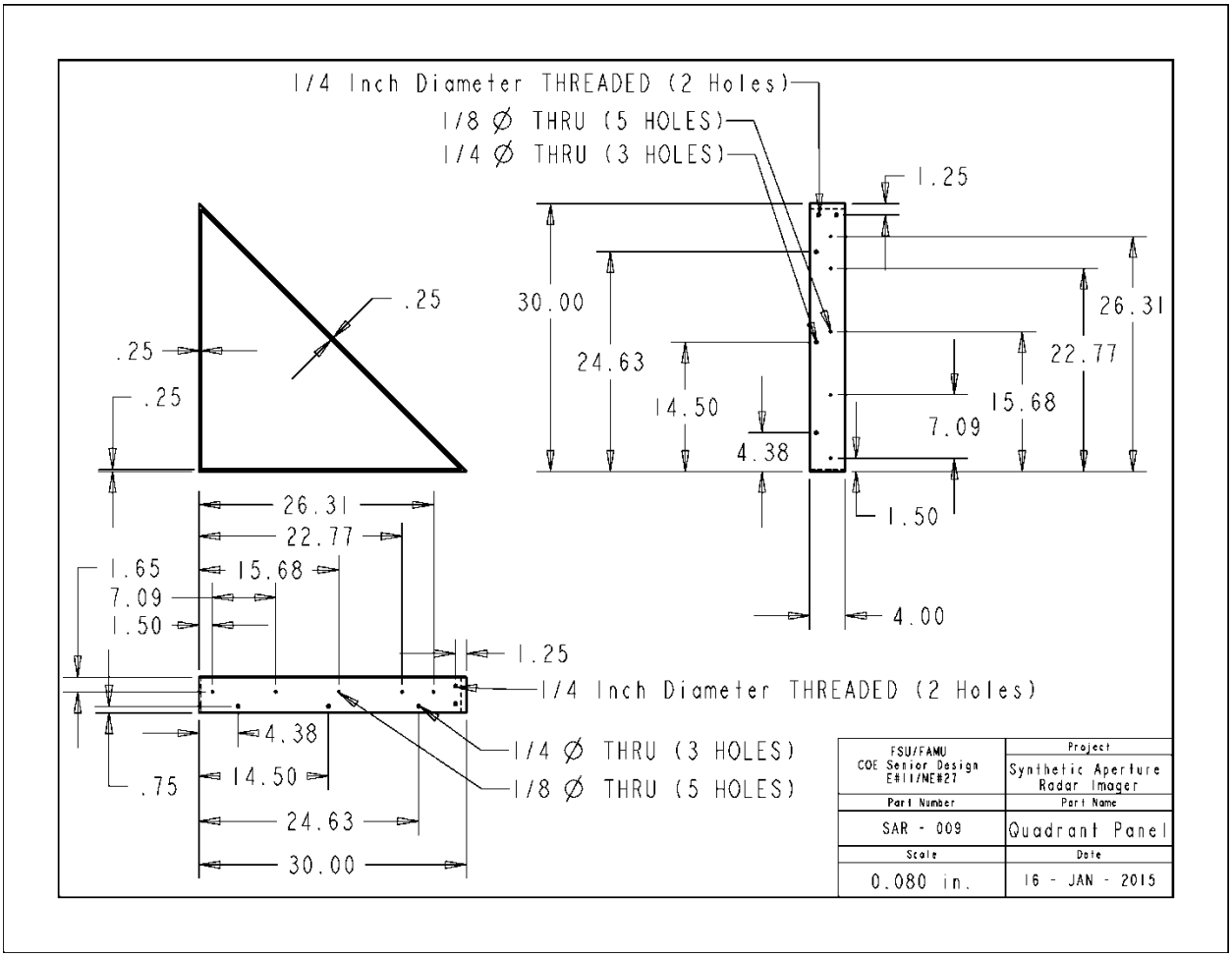


Figure 58: Quadrant Panel

10.10 Power Supply Schematic

10.10.1 DC Power Supply Inputs

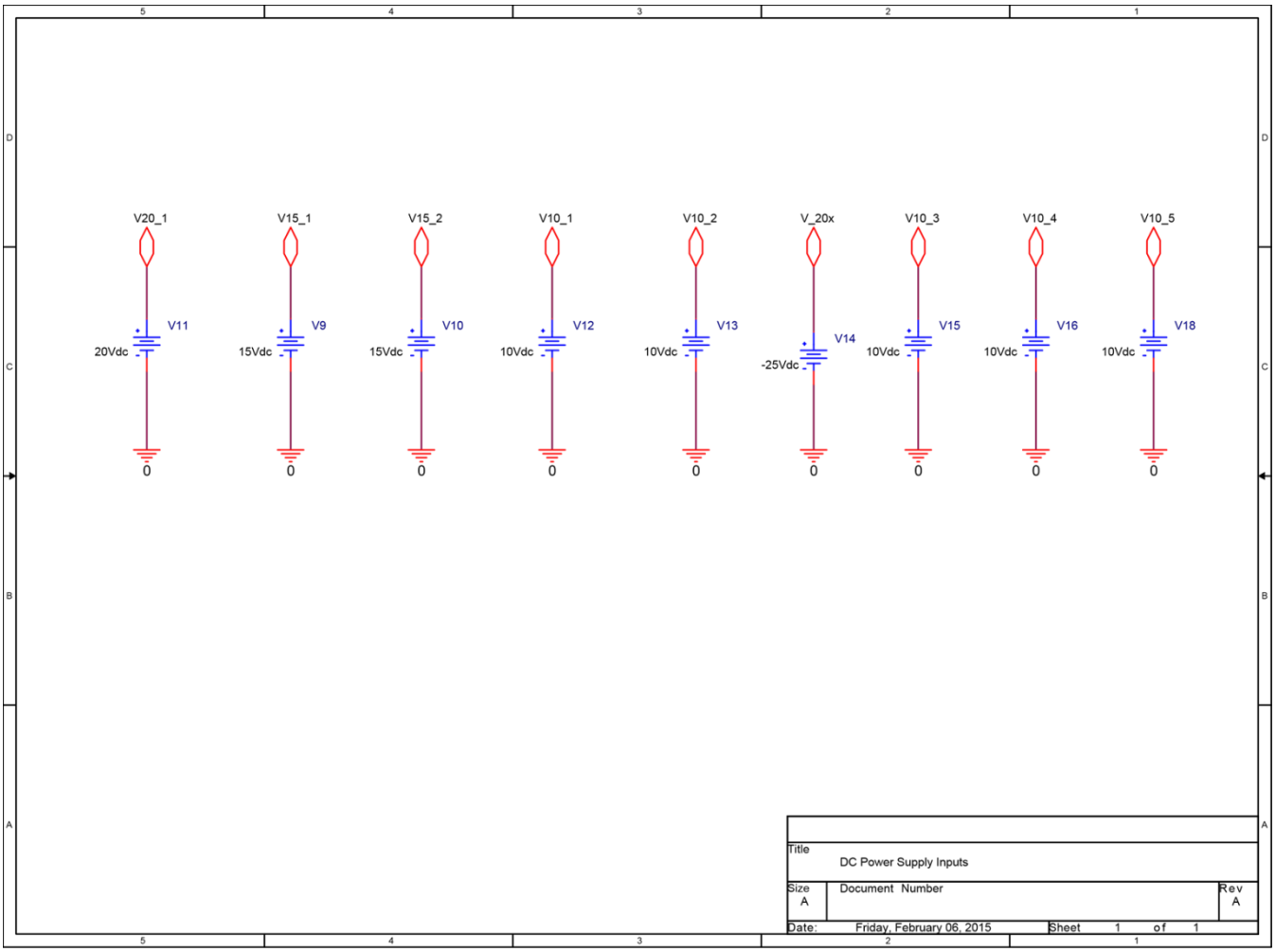


Figure 59: DC Power Supply Inputs

10.10.2 +3.3Vdc VCO/FPGA Supply

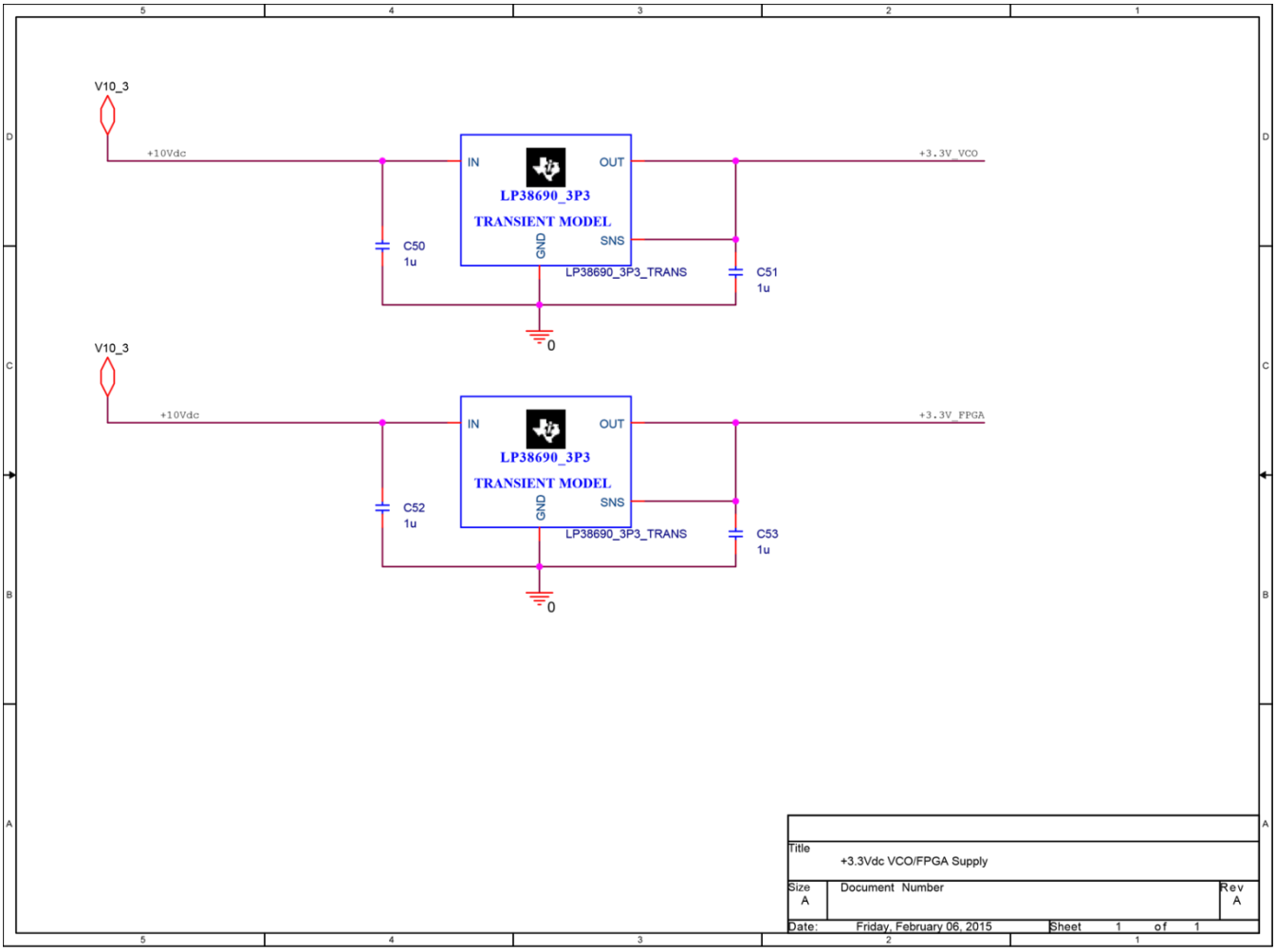


Figure 60: +3.3Vdc VCO/FPGA Supply

10.10.3 +3.5Vdc Op Amp Supply

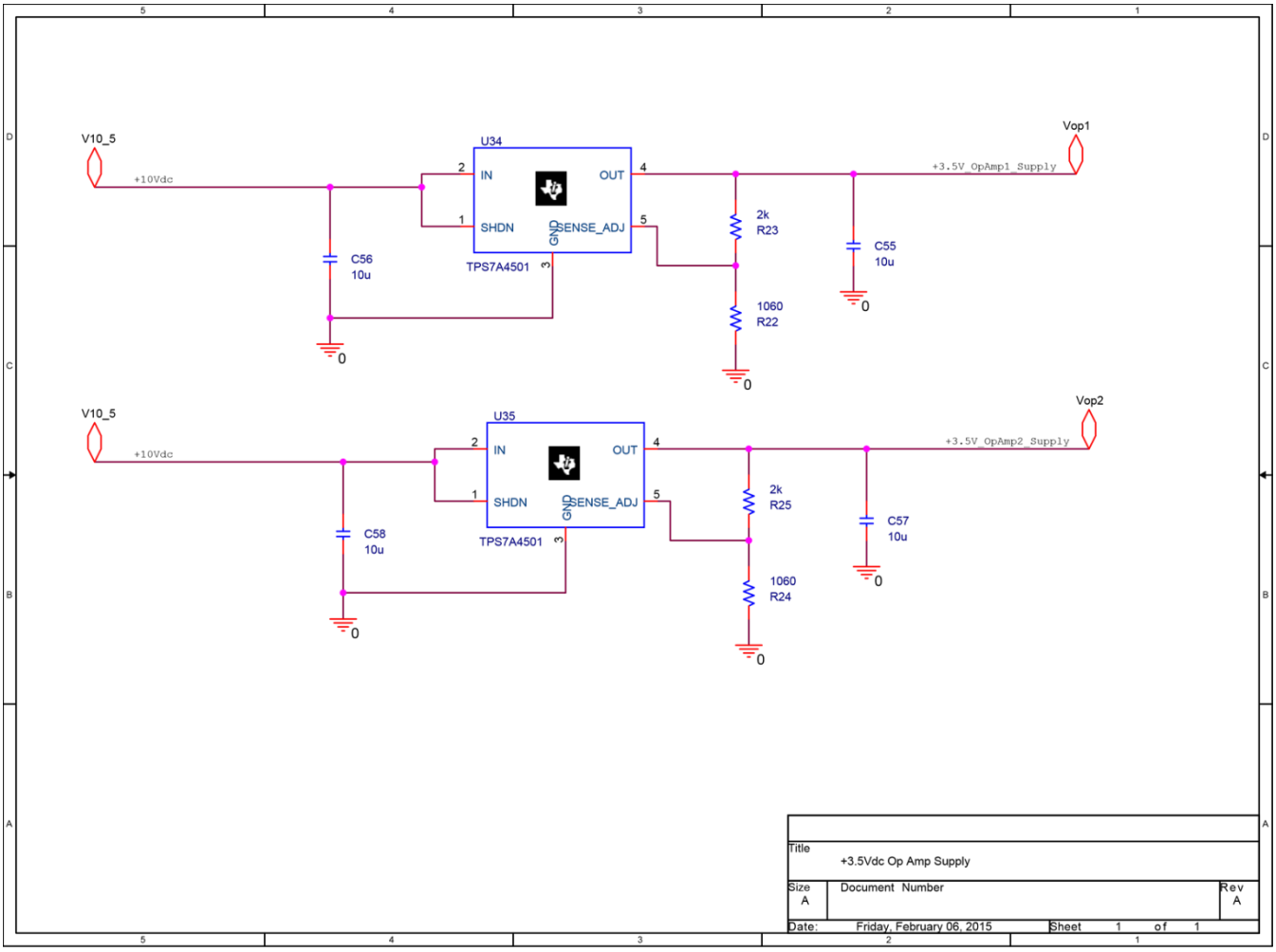


Figure 61: +3.5Vdc Op Amp Supply

10.10.4 Dual Level Shift Circuit

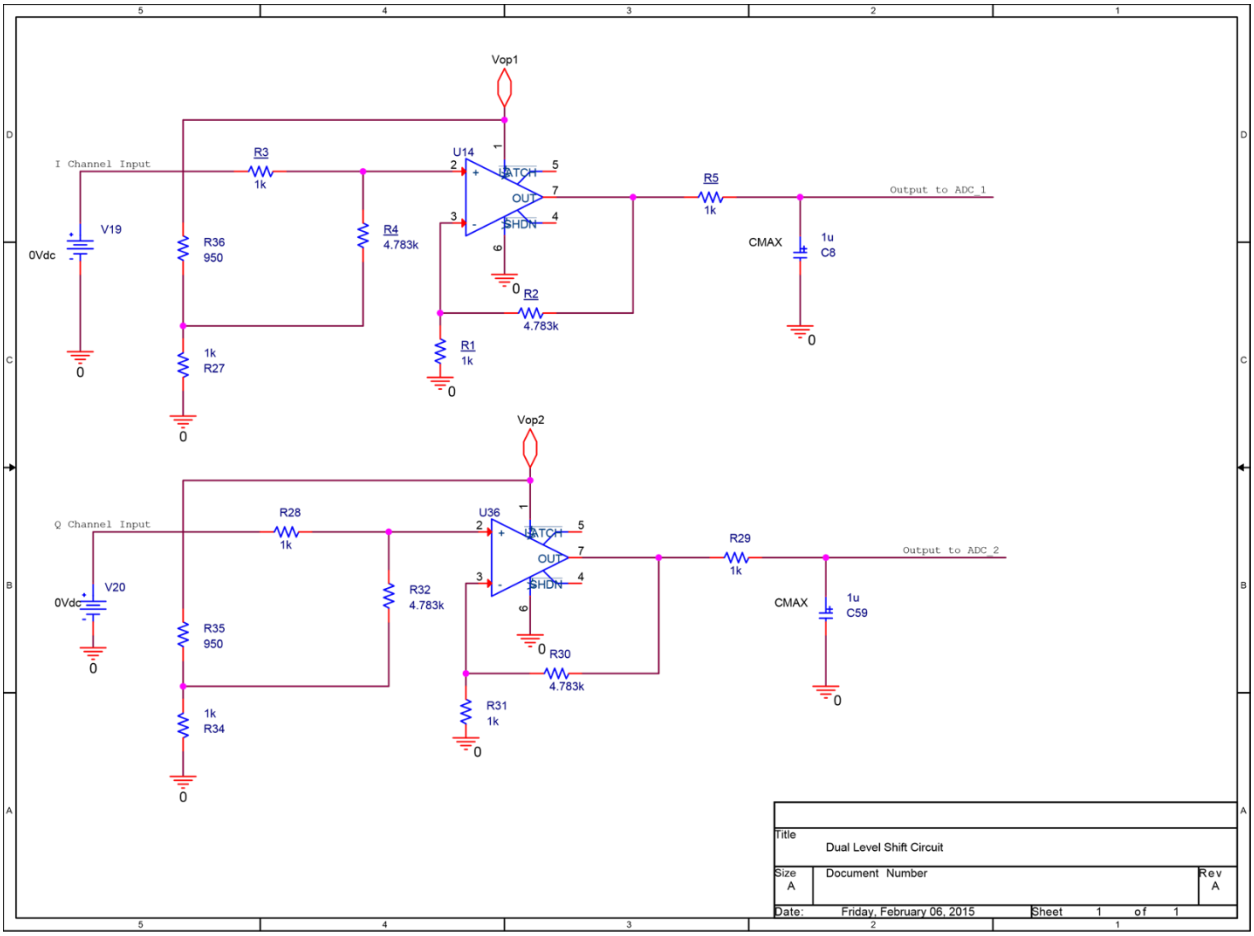


Figure 62: Dual Level Shift Circuit

10.10.5 +5Vdc Supply

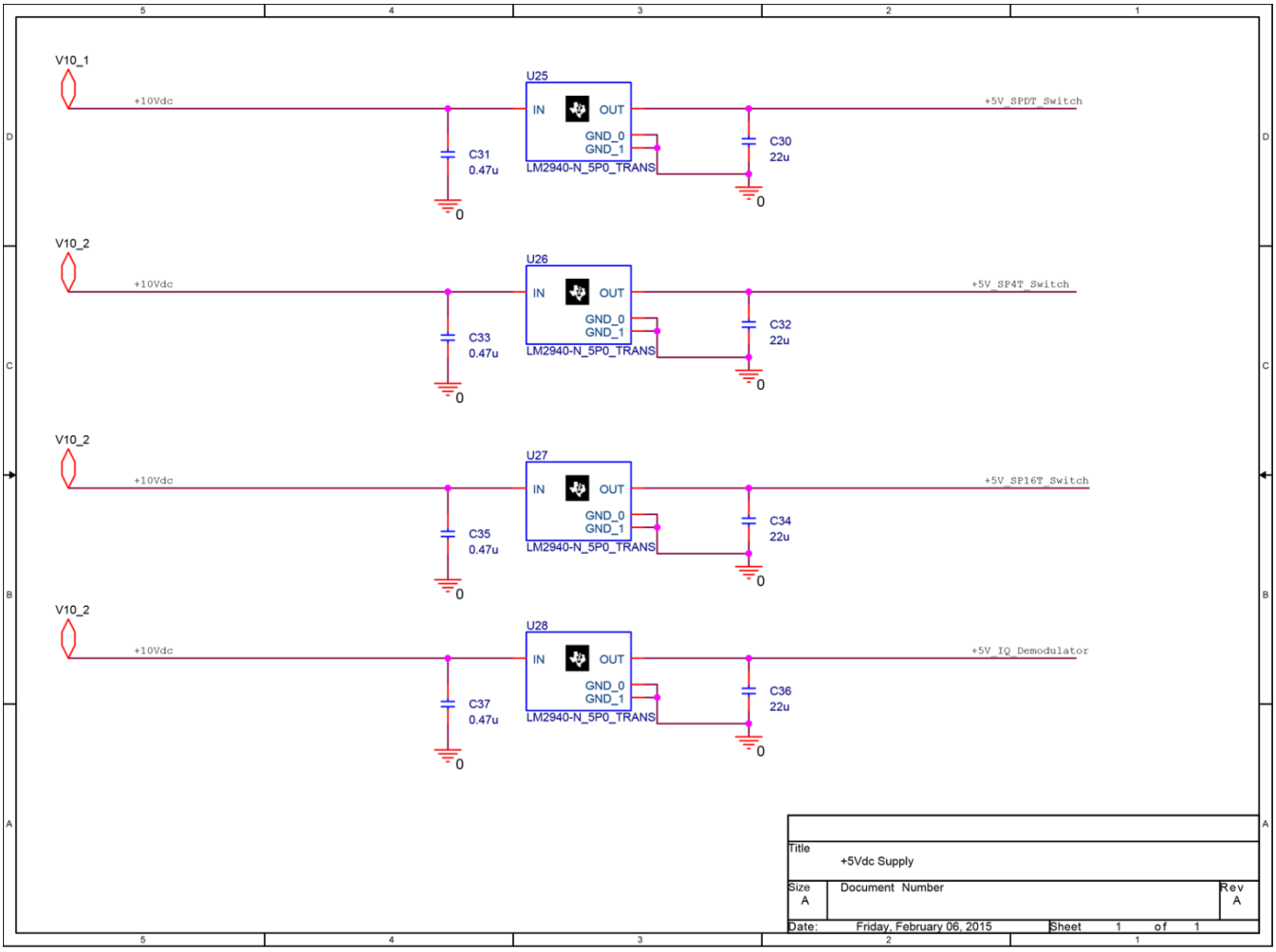


Figure 63: +5Vdc Supply

10.10.6 +21Vdc LNA Supply

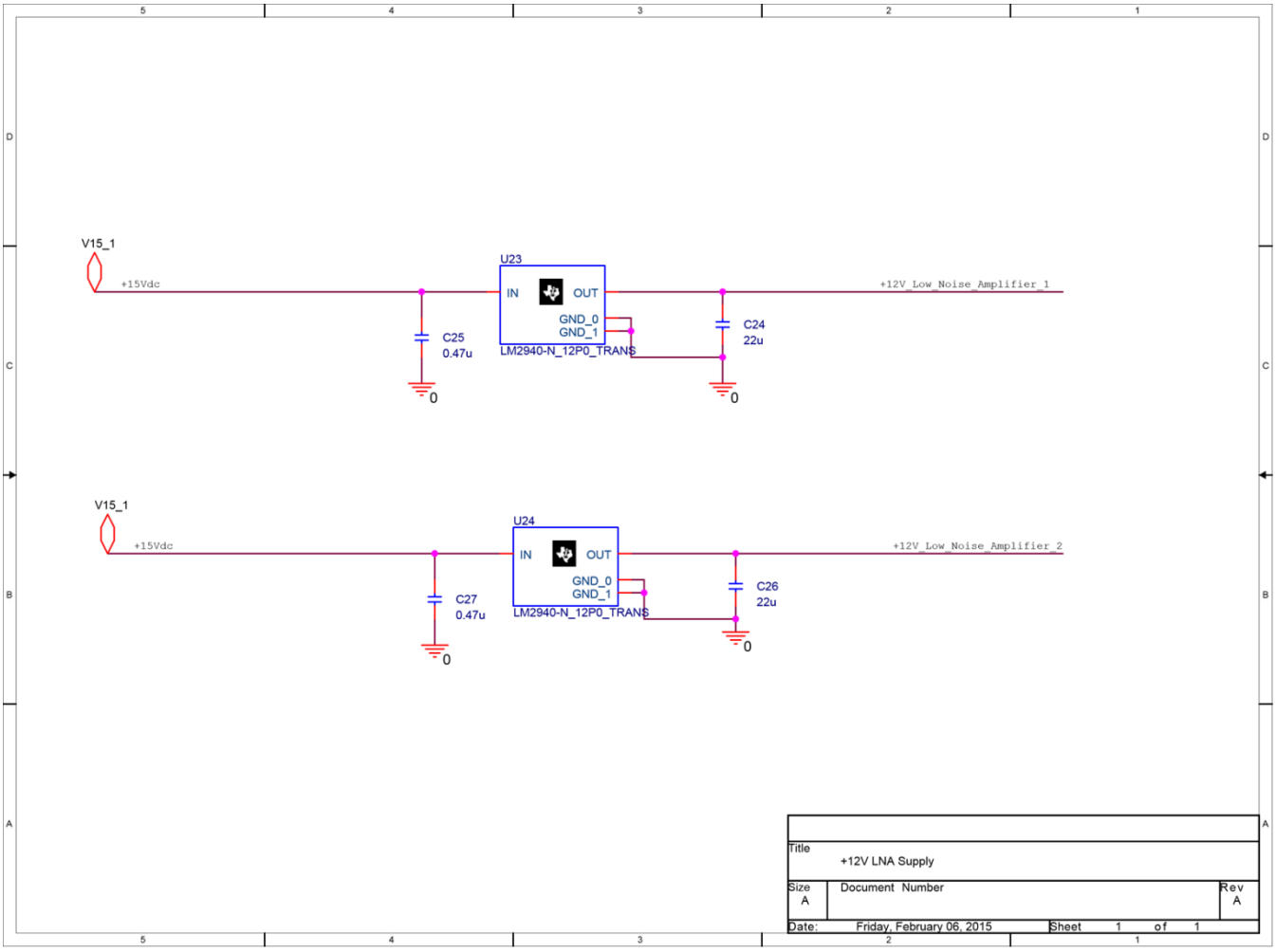


Figure 64: +21Vdc LNA Supply

10.10.7 +12Vdc Amplifier Supply

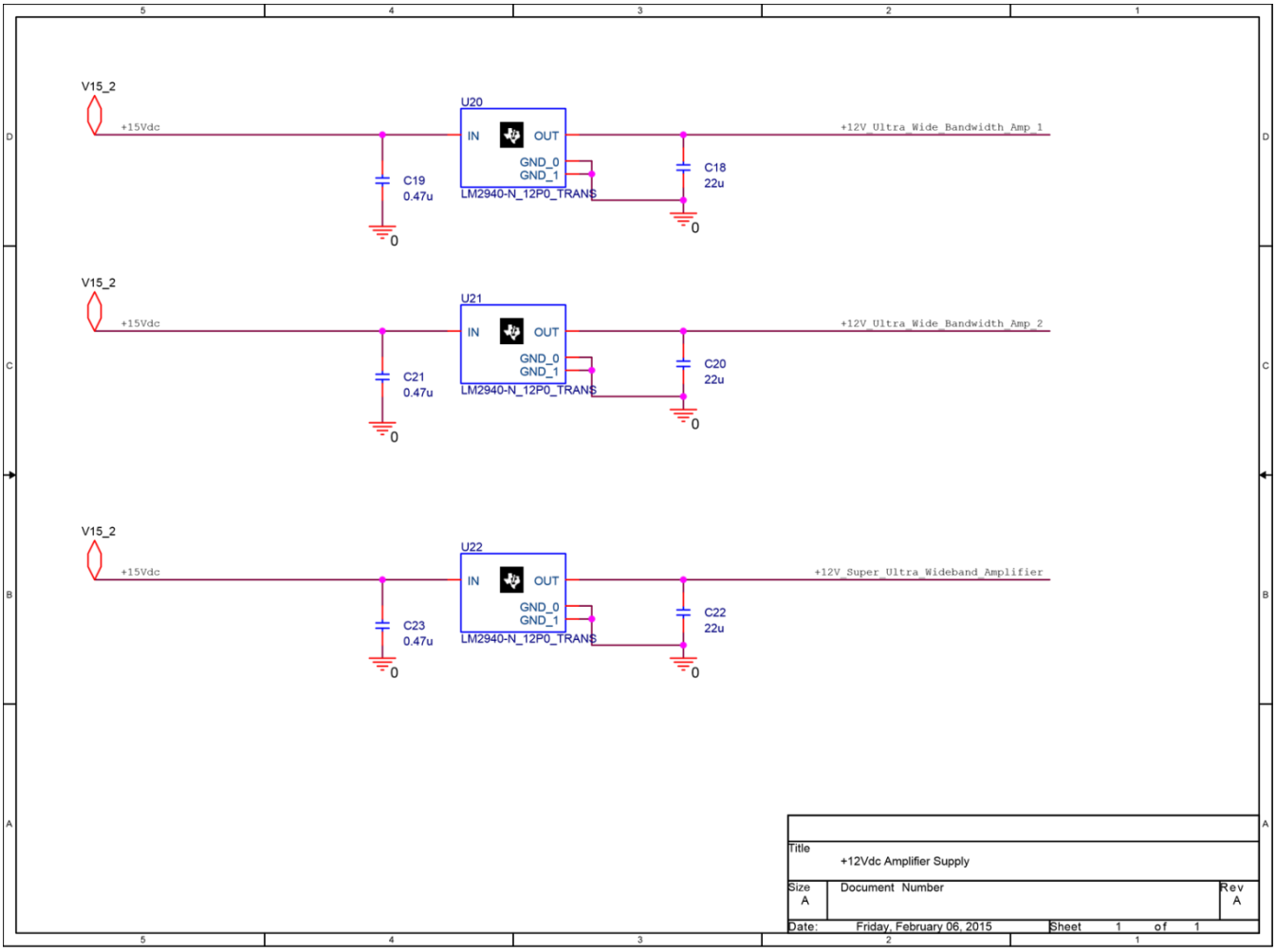


Figure 65: +12Vdc Amplifier Supply

10.10.8 +15Vdc Power Amplifier Supply

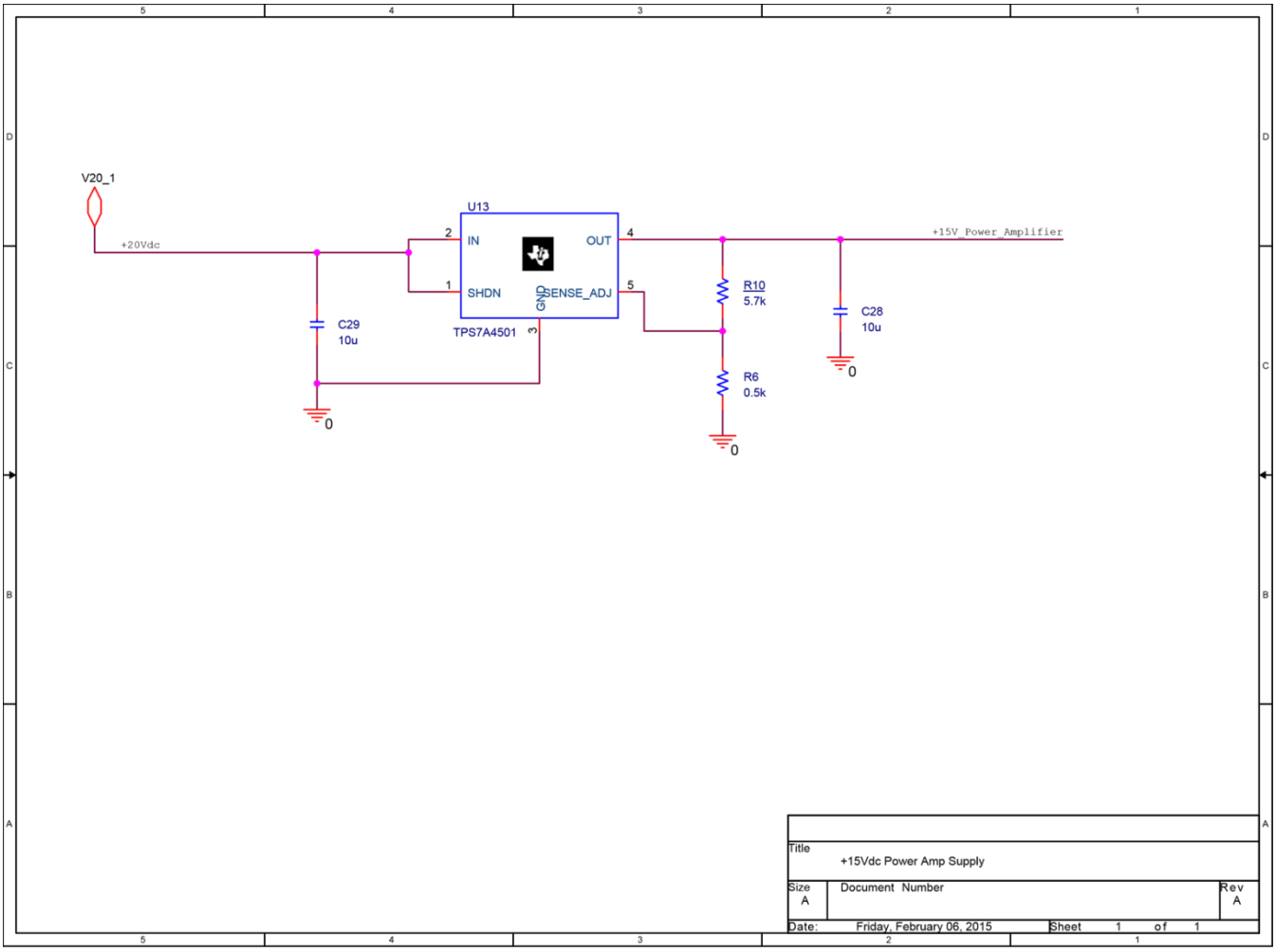


Figure 66: +15Vdc Power Amplifier Supply

10.10.9 -5Vdc_-12Vdc Supply

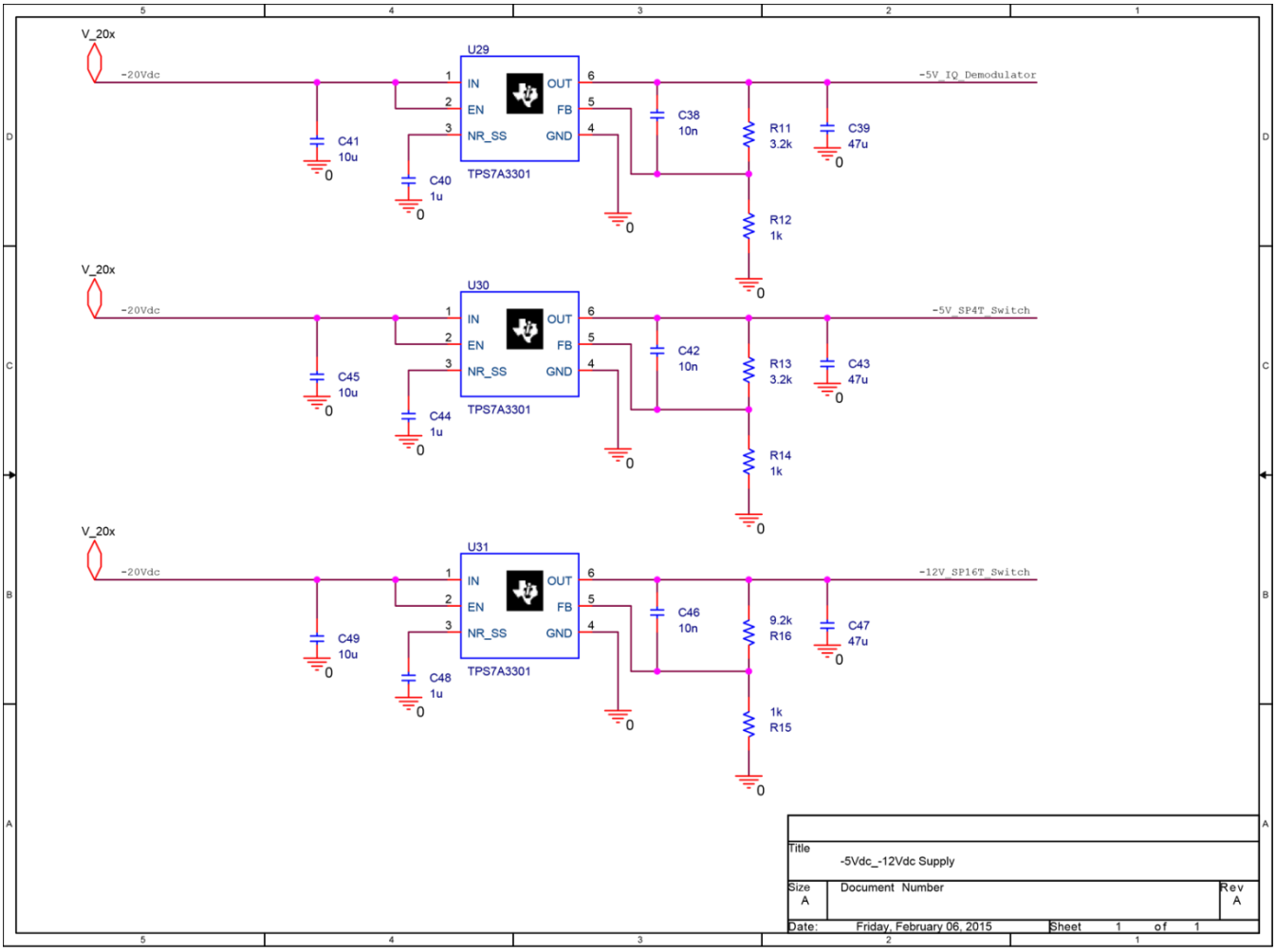


Figure 67: -5Vdc_-12Vdc Supply

10.11 Reference Code

10.11.1 Declarations

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.std_logic_unsigned.ALL;


ENTITY timing_practice IS
PORT( clk,rst : IN std_logic;
      B,C : IN std_logic_vector(11 DOWNTO 0);
      clk_div_by2,clk_div_by4,clk_div_by8,clk_div_by16,clk_div_by32,
      clk_div_by64,clk_div_by128,buff_pulse : BUFFER std_logic;
      P,Q,dec_place  : BUFFER std_logic_vector(12 DOWNTO 0);
      pulse,spdt : OUT std_logic;
      sp4t : OUT std_logic_vector(0 TO 3);
      seg_7_display_Real, seg_7_display_dec_place, seg_7_display_Imag: OUT std_logic_vector(0 TO 6);
      sp16t: OUT std_logic_vector(0 TO 15)
      );
END timing_practice;

ARCHITECTURE rtl of timing_practice IS
   signal clk_div: std_logic;
   signal clk_div2: std_logic;
   signal clk_div4: std_logic;
   signal clk_div8: std_logic;
   signal clk_div16: std_logic;
   signal clk_div32: std_logic;
   signal clk_div64: std_logic;
   signal blink: std_logic;
   signal pulse_practice: std_logic;
   signal sp4t_transmit : std_logic_vector(0 TO 3);
   signal sp16t_recieve : std_logic_vector(0 TO 15);

```

Figure 68: Declaration of libraries, inputs, buffers, outputs, and signals.

10.11.2 Code for clock division

```
BEGIN

      divide_by_2: PROCESS(rst,clk)      --This PROCESS uses 100 MHZ clock to get 200MHz timer.  Result is 10 ns on, 10 ns off.
      BEGIN
            IF(rst='1') THEN
               clk_div <='0';
            ELSIF(rising_EDGE(clk)) THEN
               clk_div <= NOT clk_div;
            END IF;
      END PROCESS divide_by_2;
      clk_div_by2 <= clk_div;


      divide_by_4: PROCESS(rst,clk_div)   --This is a divide by 4 PROCESS.   Result is 20 ns on, 20 ns off.
         BEGIN
            IF(rst='1') THEN
               clk_div2 <='0';
            ELSIF(rising_EDGE(clk_div)) THEN
               clk_div2 <= NOT clk_div2;
            END IF;
         END PROCESS divide_by_4;
         clk_div_by4 <= clk_div2;


      divide_by_8: PROCESS(rst,clk_div2)
         BEGIN
            IF(rst='1') THEN
               clk_div4 <='0';
            ELSIF(rising_EDGE(clk_div2)) THEN
               clk_div4 <= NOT clk_div4;
            END IF;
         END PROCESS divide_by_8;
         clk_div_by8 <= clk_div4;


      divide_by_16: PROCESS(rst,clk_div4)
         BEGIN
            IF(rst='1') THEN
               clk_div8 <='0';
            ELSIF(rising_EDGE(clk_div4)) THEN
               clk_div8 <= NOT clk_div8;
            END IF;
         END PROCESS divide_by_16;
         clk_div_by16 <= clk_div8;

```

Figure 69 Screenshot showing the first part of the code for the clock division

```
80
81          divide_by_32: PROCESS(rst,clk_div8)
82             BEGIN
83                IF(rst='1') THEN
84                   clk_div16 <='0';
85                ELSIF(rising_EDGE(clk_div8)) THEN
86                   clk_div16 <= NOT clk_div16;
87                END IF;
88             END PROCESS divide_by_32;
89             clk_div_by32 <= clk_div16;
90
91
92          divide_by_64: PROCESS(rst,clk_div16)
93             BEGIN
94                IF(rst='1') THEN
95                   clk_div32 <='0';
96                ELSIF(rising_EDGE(clk_div16)) THEN
97                   clk_div32 <= NOT clk_div32;
98                END IF;
99             END PROCESS divide_by_64;
100            clk_div_by64 <= clk_div32;
101
102
103         divide_by_128: PROCESS(rst,clk_div32)
104            BEGIN
105               IF(rst='1') THEN
106                  clk_div64 <='0';
107               ELSIF(rising_EDGE(clk_div32)) THEN
108                  clk_div64 <= NOT clk_div64;
109               END IF;
110            END PROCESS divide_by_128;
111            clk_div_by128 <= clk_div64;
112
```

Figure 70 Screenshot showing the second part of the code for the clock division

10.11.3 Code for timing of switches

```
113
114         timing_for_pulse: PROCESS(clk_div_by4, clk_div_by8, clk_div_by16)
115            BEGIN
116
117               blink<=clk_div_by4 AND clk_div_by8 AND clk_div_by16;
118
119            END PROCESS;
120            buff_pulse <= blink;
121            pulse <= buff_pulse;
122            spdt <=buff_pulse;
123
124
125
126
127         transmit_path: PROCESS(buff_pulse, clk_div_by32, clk_div_by64, clk_div_by128)
128            BEGIN
129                  sp4t(0) <= clk_div_by32 AND buff_pulse AND clk_div_by64;
130                  sp4t(1) <= NOT clk_div_by32 AND buff_pulse AND clk_div_by64;
131                  sp4t(2) <= clk_div_by32 AND buff_pulse AND NOT clk_div_by64;
132                  sp4t(3) <=  buff_pulse AND NOT clk_div_by128;
133            END PROCESS;
134
135
136
137
138         recieve_path: PROCESS(clk_div_by8, clk_div_by64,clk_div_by4,clk_div_by16)
139            BEGIN
140                  sp16t(0) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
141                  sp16t(1) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
142                  sp16t(2) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
143                  sp16t(3) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
144                  sp16t(4) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
145                  sp16t(5) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
146                  sp16t(6) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
147                  sp16t(7) <= clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
148
149                  sp16t(8) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
150                  sp16t(9) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
151                  sp16t(10) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
152                  sp16t(11) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
153                  sp16t(12) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
154                  sp16t(13) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
155                  sp16t(14) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
156                  sp16t(15) <=  NOT clk_div_by64 AND clk_div_by4 AND clk_div_by16 AND NOT clk_div_by8;
157
158            END PROCESS;
159
160
161
```

Figure 71 Screenshot of the logic used for the timing of the pulse, transmit path, and receive path

10.11.4 Logic for A/D conversion

```
162
163     bcd1: process(B)
164     variable z: std_logic_vector (26 downto 0);
165        begin
166
167           for i in 0 to 26 loop
168              z(i) :='0';
169           end loop;                                                    --sets all bits in z to zero
170
171     z(14 downto 3) :=B;
172
173           for i in 0 to 8 loop
174              if z(15 downto 12) > 4 then
175                 z(15 downto 12) := z(15 downto 12) + 3;
176              end if;
177
178              if z(19 downto 16) > 4 then
179                 z(19 downto 16) := z(19 downto 16) + 3;
180              end if;
181
182              if z(23 downto 20) < 4 then
183                 z(23 downto 20) := z(23 downto 20) + 3;
184              end if;
185
186     z(26 downto 1) := z(25 downto 0);
187
188           end loop;
189
190
191     P <= z(26 downto 14);
192        end process bcd1;
193
```

Figure 72 Screenshot showing the binary to binary coded decimal conversion of the Real Voltage

```
194
195
196        bcd2: process(C)
197     variable z: std_logic_vector (26 downto 0);
198        begin
199
200           for i in 0 to 26 loop
201              z(i) :='0';                                              --sets all bits in z to zero
202           end loop;
203
204     z(14 downto 3) :=B;
205
206           for i in 0 to 8 loop
207              if z(15 downto 12) > 4 then
208                 z(15 downto 12) := z(15 downto 12) + 3;
209              end if;
210
211              if z(19 downto 16) > 4 then
212                 z(19 downto 16) := z(19 downto 16) + 3;
213              end if;
214
215              if z(23 downto 20) < 4 then
216                 z(23 downto 20) := z(23 downto 20) + 3;
217              end if;
218
219     z(26 downto 1) := z(25 downto 0);
220
221           end loop;
222
223
224     Q <= z(26 downto 14);
225        end process bcd2;
226
```

Figure 73 Screenshot showing the binary to binary coded decimal conversion of the Imaginary Voltage

10.11.5 Code for 7 segment display

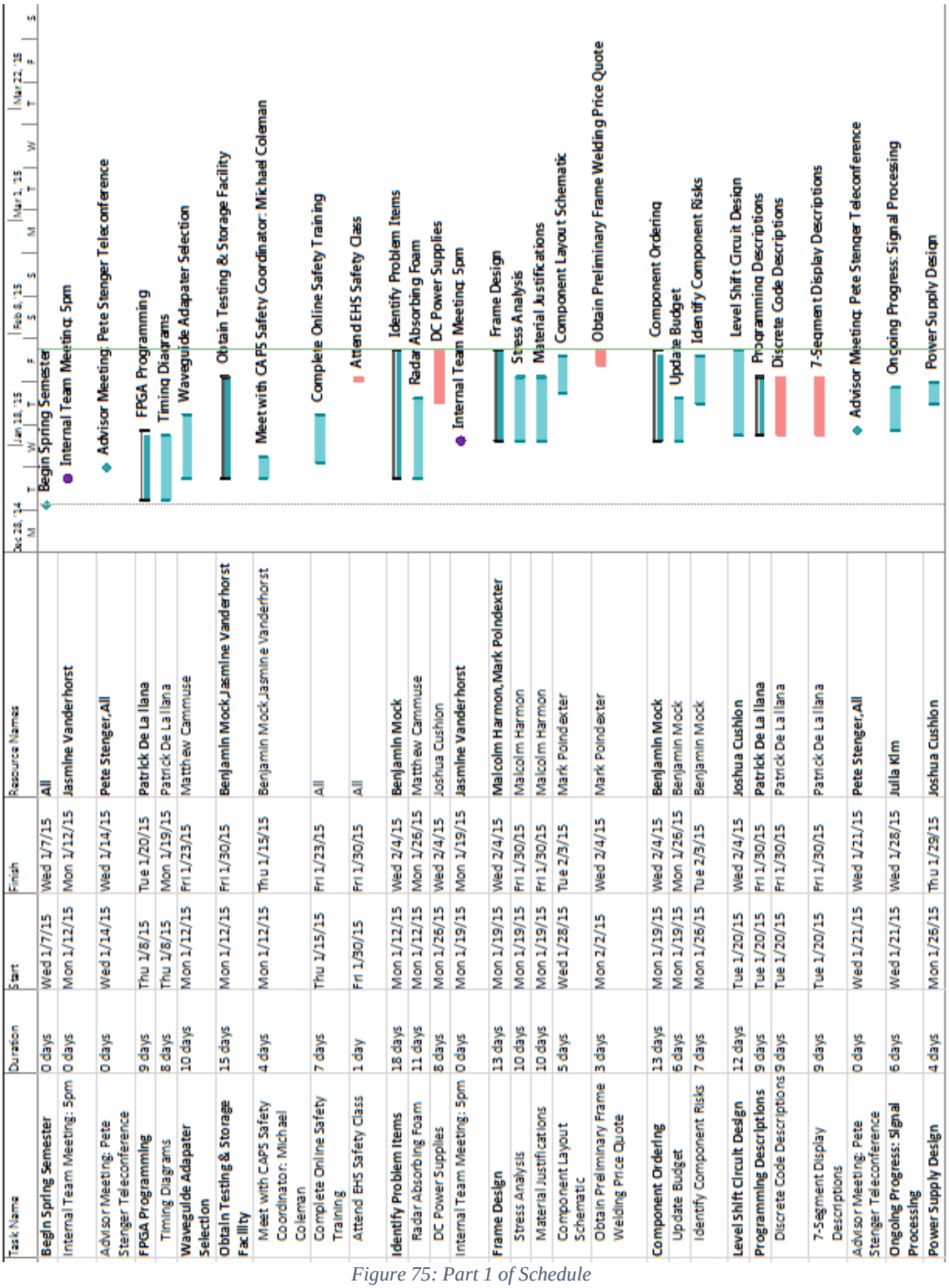
```
Real_num_v: PROCESS(P)
      BEGIN
         case P IS
            WHEN  "0000000000000"=> seg_7_display_Real <= "0111111";    --0
            WHEN  "0000000000001"=> seg_7_display_Real <= "0000110";    --1
            WHEN  "0000000000010"=> seg_7_display_Real <= "1011011";    --2
            WHEN  "0000000000011"=> seg_7_display_Real <= "1001111";    --3
            WHEN  "0000000000100"=> seg_7_display_Real <= "1100110";    --4
            WHEN  "0000000000101"=> seg_7_display_Real <= "1101101";    --5
            WHEN  "0000000000110"=> seg_7_display_Real <= "1111101";    --6
            WHEN  "0000000000111"=> seg_7_display_Real <= "0000111";    --7
            WHEN  "0000000001000"=> seg_7_display_Real <= "1111111";    --8
            WHEN  "0000000001001"=> seg_7_display_Real <= "1101111";    --9
            WHEN OTHERS => seg_7_display_Real <= "1111111";
      END CASE;
   END PROCESS;


Dec_place_v: PROCESS(dec_place)
   BEGIN
   case dec_place IS
   WHEN  "0000000000000"=> seg_7_display_dec_place <= "0001000";        --This is simply an underscore as a decimal place
   WHEN OTHERS => seg_7_display_dec_place <= "0001000";
   END CASE;
   END PROCESS;


Imag_num_v: PROCESS(Q)
      BEGIN
         case Q IS
            WHEN  "0000000000000"=> seg_7_display_Imag <= "0111111";    --0
            WHEN  "0000000000001"=> seg_7_display_Imag <= "0000110";    --1
            WHEN  "0000000000010"=> seg_7_display_Imag <= "1011011";    --2
            WHEN  "0000000000011"=> seg_7_display_Imag <= "1001111";    --3
            WHEN  "0000000000100"=> seg_7_display_Imag <= "1100110";    --4
            WHEN  "0000000000101"=> seg_7_display_Imag <= "1101101";    --5
            WHEN  "0000000000110"=> seg_7_display_Imag <= "1111101";    --6
            WHEN  "0000000000111"=> seg_7_display_Imag <= "0000111";    --7
            WHEN  "0000000001000"=> seg_7_display_Imag <= "1111111";    --8
            WHEN  "0000000001001"=> seg_7_display_Imag <= "1101111";    --9
            WHEN  OTHERS => seg_7_display_Imag <= "1111111";
         END CASE;
   END PROCESS;
```

Figure 74 Screenshot of the logic for the 7 segment display

10.12 Project Gantt Chart



Task Name	Duration	Start	Finish	Resource Names
Begin Spring Semester	0 days	Wed 1/7/15	Wed 1/7/15	All
Internal Team Meeting: 5pm	0 days	Mon 1/12/15	Mon 1/12/15	Jasmine Vanderhorst
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/14/15	Wed 1/14/15	Pete Stenger,All
FPGA Programming	9 days	Thu 1/8/15	Tue 1/20/15	Patrick De La Ilana
Timing Diagrams	8 days	Thu 1/8/15	Mon 1/19/15	Patrick De La Ilana
Waveguide Adapater Selection	10 days	Mon 1/12/15	Fri 1/23/15	Matthew Cammuse
Obtain Testing & Storage Facility	15 days	Mon 1/12/15	Fri 1/30/15	Benjamin Mock,Jasmine Vanderhorst
Meet with CAPS Safety Coordinator: Michael Coleman	4 days	Mon 1/12/15	Thu 1/15/15	Benjamin Mock,Jasmine Vanderhorst
Complete Online Safety Training	7 days	Thu 1/15/15	Fri 1/23/15	All
Attend EHS Safety Class	1 day	Fri 1/30/15	Fri 1/30/15	All
Identify Problem Items	18 days	Mon 1/12/15	Wed 2/4/15	Benjamin Mock
Radar Absorbing Foam	11 days	Mon 1/12/15	Mon 1/26/15	Matthew Cammuse
DC Power Supplies	8 days	Mon 1/26/15	Wed 2/4/15	Joshua Cushion
Internal Team Meeting: 5pm	0 days	Mon 1/19/15	Mon 1/19/15	Jasmine Vanderhorst
Frame Design	13 days	Mon 1/19/15	Wed 2/4/15	Malcolm Harmon,Mark Poindexter
Stress Analysis	10 days	Mon 1/19/15	Fri 1/30/15	Malcolm Harmon
Material Justifications	10 days	Mon 1/19/15	Fri 1/30/15	Malcolm Harmon
Component Layout Schematic	5 days	Wed 1/28/15	Tue 2/3/15	Mark Poindexter
Obtain Preliminary Frame Welding Price Quote	3 days	Mon 2/2/15	Wed 2/4/15	Mark Poindexter
Component Ordering	13 days	Mon 1/19/15	Wed 2/4/15	Benjamin Mock
Update Budget	6 days	Mon 1/19/15	Mon 1/26/15	Benjamin Mock
Identify Component Risks	7 days	Mon 1/26/15	Tue 2/3/15	Benjamin Mock
Level Shift Circuit Design	12 days	Tue 1/20/15	Wed 2/4/15	Joshua Cushion
Programming Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	Patrick De La Ilana
Discrete Code Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	Patrick De La Ilana
7-Segment Display Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	Patrick De La Ilana
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/21/15	Wed 1/21/15	Pete Stenger,All
Ongoing Progress: Signal Processing	6 days	Wed 1/21/15	Wed 1/28/15	Julia Kim
Power Supply Design	4 days	Mon 1/26/15	Thu 1/29/15	Joshua Cushion

Figure 75: Part 1 of Schedule

Task Name	Duration	Start	Finish	Resource Names
Internal Team Meeting: 5pm	0 days	Mon 1/26/15	Mon 1/26/15	Jasmine Vanderhorst
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/28/15	Wed 1/28/15	Pete Stenger,All
Ongoing Progress: Signal Processing	6 days	Wed 1/28/15	Wed 2/4/15	Julia Kim
Develop Testing Plans	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
Individual Component Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
Subassembly Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
System Integration Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse
Gather Appropriate Safety Signage	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock
Anechoic Foam Layout	11 days	Fri 1/30/15	Fri 2/13/15	Matthew Cammuse
Shipping Arrangements	11 days	Fri 1/30/15	Fri 2/13/15	Benjamin Mock
RF Lambda Vendor Parts	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock
Marki: Bandpass Filter	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock
Fairview Vendor Parts	7 days	Fri 1/30/15	Mon 2/9/15	Benjamin Mock
Digikey Vendor Parts	9 days	Fri 1/30/15	Wed 2/11/15	Benjamin Mock
Minicircuits Vendor Parts	11 days	Fri 1/30/15	Fri 2/13/15	Benjamin Mock
Team Meeting & Preparation for VP of Northrop Grumman	1 day	Mon 2/9/15	Mon 2/9/15	All
Internal Team Meeting: 5pm	0 days	Mon 2/2/15	Mon 2/2/15	Jasmine Vanderhorst
Calibration Plan: Hardware & Software Compatibility	3 days	Mon 2/2/15	Wed 2/4/15	Joshua Cushlon
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/4/15	Wed 2/4/15	Pete Stenger,All
Team Members Submit Report Sections	0 days	Wed 2/4/15	Wed 2/4/15	All
Milestone 4 Report Due	0 days	Thu 2/5/15	Thu 2/5/15	All
Ongoing Progress: Signal Processing	6 days	Wed 2/4/15	Wed 2/11/15	Julia Kim
Data Storing Software for FPGA to PCU	12 days	Thu 2/5/15	Fri 2/20/15	Matthew Cammuse,Patrick De La Llana
Finalize Frame Design	3 days	Tue 2/10/15	Thu 2/12/15	Malcolm Harmon,Mark Poindexter
GO/NO-GO Design Stopping Point	2 days	Tue 2/10/15	Wed 2/11/15	Mark Poindexter,Malcolm Harmon,Pete Stenger
Submit Final Design Welding Vendors	2 days	Wed 2/11/15	Thu 2/12/15	Malcolm Harmon,Mark Poindexter,Pete Stenger
Prepare Presentation	4 days	Mon 2/9/15	Thu 2/12/15	Jasmine Vanderhorst

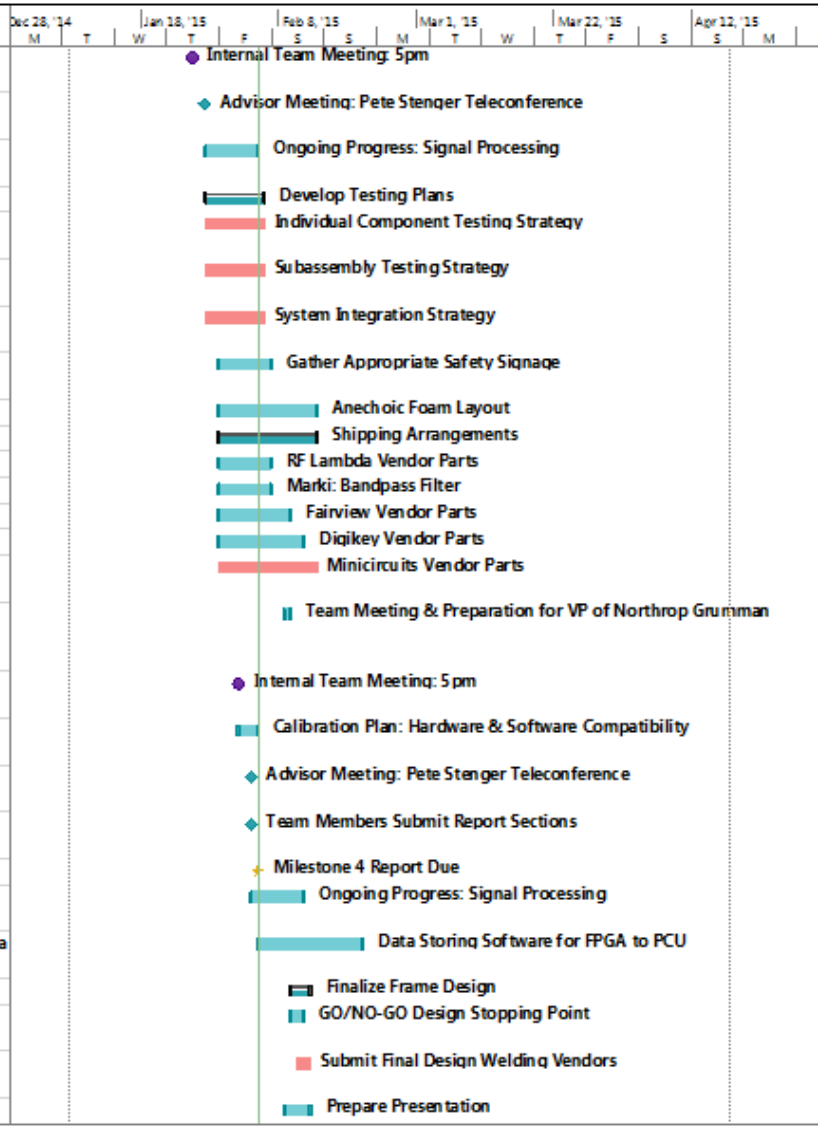


Figure 76: Part 2 of Schedule

Task Name	Duration	Start	Finish	Resource Names
Milestone 4: Detailed Design Review & Test Plan Presentation	5 days	Mon 2/9/15	Fri 2/13/15	**All**
Northrop Grumman VP Visit and Project Update	2 days	Tue 2/10/15	Wed 2/11/15	**Pete Stenger,All**
Programming & Testing	20 days	Mon 2/9/15	Fri 3/6/15	**Patrick De La llana**
Analog To Digital Conversion Code	11 days	Mon 2/9/15	Mon 2/23/15	Patrick De La llana
FPGA Code Simulation and Testing	15 days	Mon 2/16/15	Fri 3/6/15	Patrick De La llana
Build Component Box and Attach to Frame	15 days	Mon 2/9/15	Fri 2/27/15	**Mark Poindexter**
Receive Completed Antenna Frame	0 days	Fri 2/27/15	Fri 2/27/15	**Malcolm Harmon**
Transmit and Modulator LO Chain Component Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Matthew Cammuse,Joshua Cushlon**
Programming Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Patrick De La llana**
Subassembly Testing	10 days	Mon 2/9/15	Fri 2/20/15	**Joshua Cushlon,Matthew Cammuse**
Transmit Signal and Modulator LO Chain	5 days	Mon 2/9/15	Fri 2/13/15	Joshua Cushlon,Matthew Cammuse
Power Supply Board	3 days	Wed 2/18/15	Fri 2/20/15	Joshua Cushlon,Matthew Cammuse
Data Gathering, Analysis, and Reporting	10 days	Mon 2/9/15	Fri 2/20/15	Julia Kim
Miscellaneous Task	10 days	Mon 2/9/15	Fri 2/20/15	Julia Kim
Receive Signal Chain	6 days	Fri 2/13/15	Fri 2/20/15	Joshua Cushlon,Matthew Cammuse
Ongoing Progress: Signal Processing	6 days	Wed 2/11/15	Wed 2/18/15	**Julia Kim**
Build Power Supply Board	3 days	Mon 2/16/15	Wed 2/18/15	**Joshua Cushlon**
Internal Team Meeting: 5pm	0 days	Mon 2/16/15	Mon 2/16/15	**Jasmine Vanderhorst**
Ongoing Progress: Signal Processing	6 days	Wed 2/18/15	Wed 2/25/15	**Julia Kim**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/18/15	Wed 2/18/15	**All**
Software Demonstration	5 days	Mon 2/23/15	Fri 2/27/15	**Patrick De La llana**
Discrete Code Switch Display	2 days	Mon 2/23/15	Tue 2/24/15	Patrick De La llana
A-to-D Conversion Display	2 days	Tue 2/24/15	Wed 2/25/15	Patrick De La llana
Tentative: VGA Imaging Display	2 days	Thu 2/26/15	Fri 2/27/15	Patrick De La llana
Internal Team Meeting: 5pm	0 days	Mon 2/23/15	Mon 2/23/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete	0 days	Wed 2/25/15	Wed 2/25/15	**All**

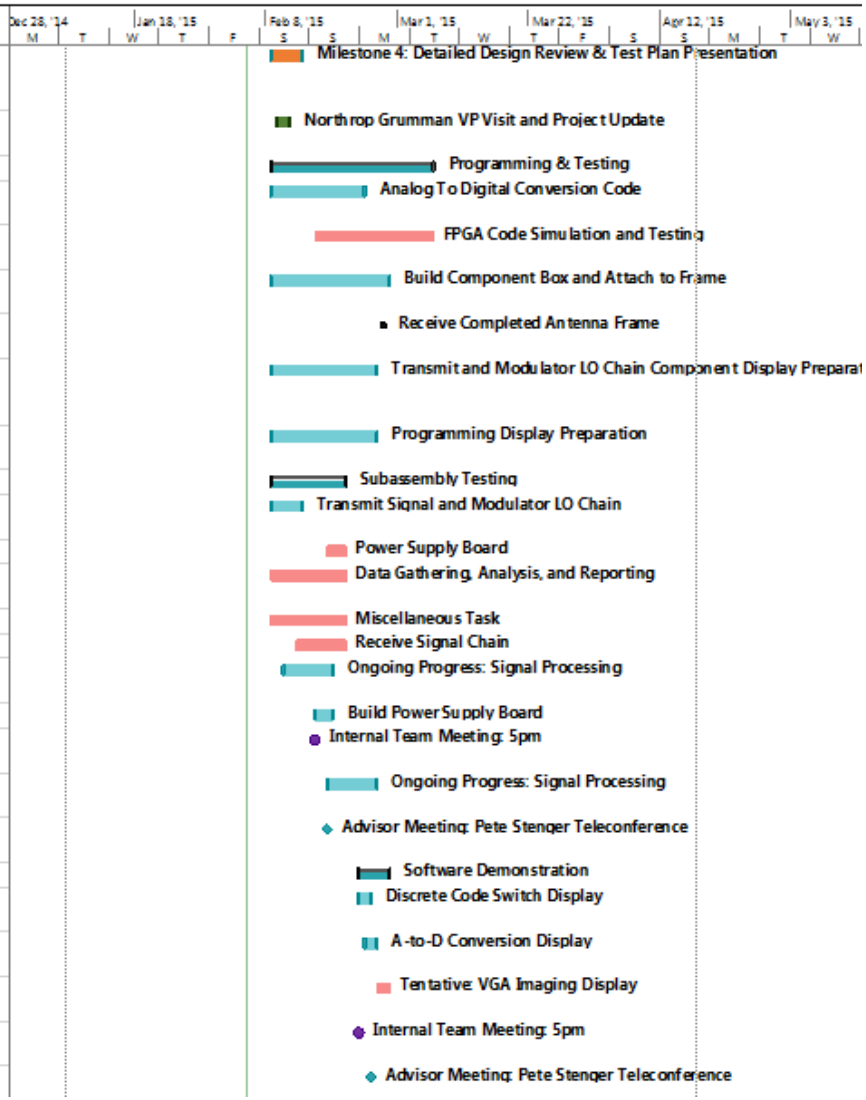


Figure 77: Part 3 of Schedule

Task Name	Duration	Start	Finish	Resource Names
Milestone 5: Midterm Hardware/Software Reviews	5 days	Mon 2/23/15	Fri 2/27/15	**All**
DC Wire Harness	**23 days**	**Mon 2/16/15**	**Wed 3/18/15**	**Mark Poindexter**
Wire Design Support for Pre-Fab	8 days	Mon 2/16/15	Wed 2/25/15	Julia Kim
Design DC Wire Harness	8 days	Mon 2/16/15	Wed 2/25/15	Mark Poindexter
Build DC Wire Harness	8 days	Wed 2/25/15	Fri 3/6/15	Malcolm Harmon
Troubleshooting	9 days	Fri 3/6/15	Wed 3/18/15	Malcolm Harmon,Julia Kim,Mark Poinde
Ongoing Progress: Signal Processing	6 days	Wed 2/25/15	Wed 3/4/15	**Julia Kim**
VGA Coding	20 days	Mon 3/2/15	Fri 3/27/15	**Patrick De La Ilana**
Spring Break: No School	5 days	Mon 3/9/15	Fri 3/13/15	**All**
Ongoing Progress: Signal Processing	11 days	Wed 3/4/15	Wed 3/18/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/16/15	Mon 3/16/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/18/15	Wed 3/18/15	**All**
Hardware Integration	25 days	Mon 3/2/15	Fri 4/3/15	**Joshua Cushion,Julia Kim,Mark Poinde**
Soldering Components	13 days	Mon 3/2/15	Wed 3/18/15	Matthew Cammuse,Patrick De La Ilana
Install and Fasten Components	13 days	Mon 3/2/15	Wed 3/18/15	Malcolm Harmon,Mark Poindexter
Cabling	5 days	Thu 3/19/15	Wed 3/25/15	Mark Poindexter
Power Connection	10 days	Mon 3/23/15	Fri 4/3/15	Joshua Cushion,Julia Kim
Software Integration	25 days	Mon 3/2/15	Fri 4/3/15	**Patrick De La Ilana**
Integrate all codes with FPGA Board	22 days	Mon 3/2/15	Tue 3/31/15	Patrick De La Ilana
Sync Hardware with Code	15 days	Mon 3/16/15	Fri 4/3/15	Patrick De La Ilana,Joshua Cushion
Troubleshooting	10 days	Mon 3/23/15	Fri 4/3/15	Joshua Cushion,Julia Kim,Matthew Cam
Ongoing Progress: Signal Processing	6 days	Wed 3/18/15	Wed 3/25/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/23/15	Mon 3/23/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/25/15	Wed 3/25/15	**All**
System Testing	11 days	Mon 3/23/15	Mon 4/6/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 3/25/15	Wed 4/1/15	**Julia Kim**
Internal Team Meeting: 5pm	0 days	Mon 3/30/15	Mon 3/30/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 4/1/15	Wed 4/1/15	**All**
Design Project Poster	5 days	Wed 4/1/15	Tue 4/7/15	**Jasmine Vanderhorst**
Finallze Signal Processing	6 days	Wed 4/1/15	Wed 4/8/15	**Julia Kim**

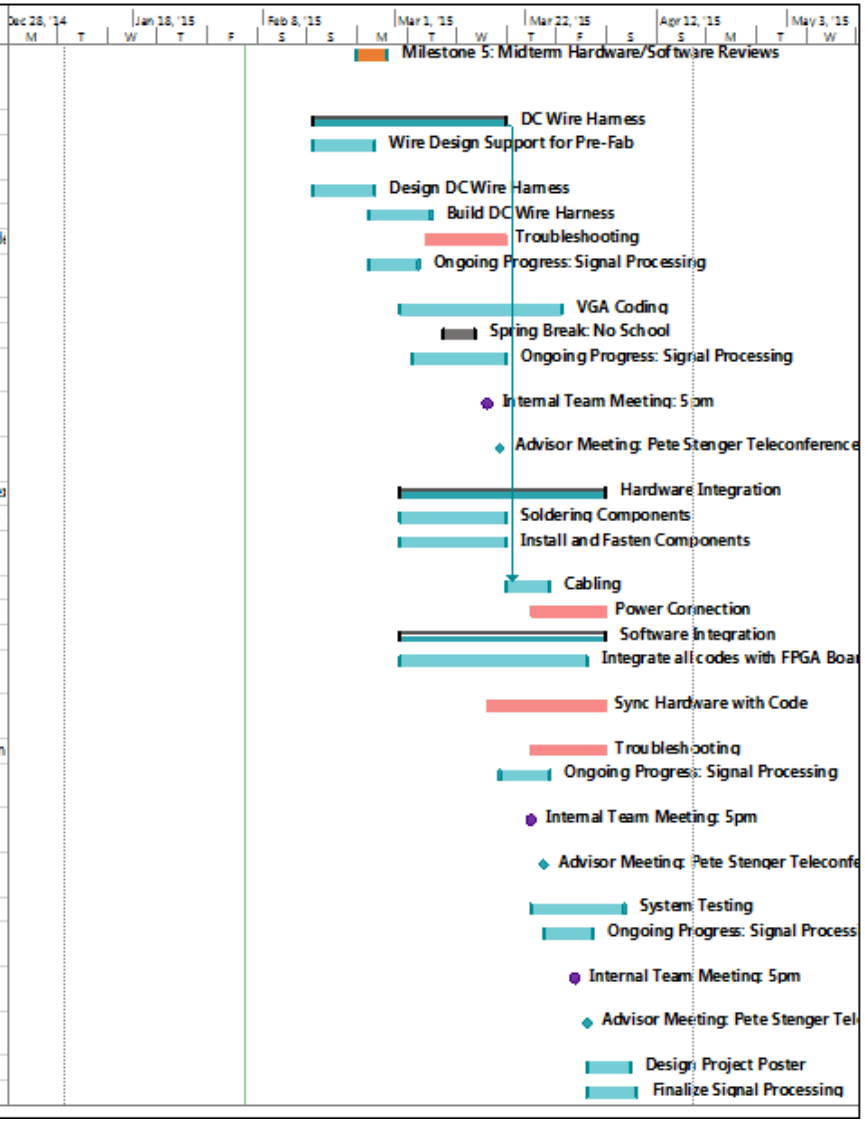


Figure 78: Part 4 of Schedule