FAMU-FSU College of Engineering
Department of Electrical and Computer Engineering

SYSTEM-LEVEL DESIGN REVIEW

EEL4911C – ECE Senior Design Project II

Project Title: **Synthetic Active Array Radar Aperture (SAR)**

Team #: E11

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Executive Summary

The purpose of the electronic Synthetic Active Aperture Radar (SAR) Imager project, sponsored by Northrop Grumman, is to design and develop a low-cost detection system capable of providing a low, but useful, imagery resolution as a learning experience. In theory, the application of the electronic SAR Imager focuses on security applications and its ability to detect potentially threatening objects such as handguns. This project is sponsored through the FAMU-Foundation with a $50,000.00 budget with an expected time line of eight months to completion.
A radar is an object detection system that uses radio waves to measure characteristics of certain objects and is typically composed of antennas in which transmit pulses of radio waves bounce off the target in the designated range. The wave is reflected off the target and returns a wave to the receiving end of the system which is usually a dish, horn, or some form of waveguide usually located at the same site as the transmission of the wave. In a typical radar, the antenna which usually acts as a transmitter and/or receiver is in a static position. The electronic SAR Imager is a more complicated scenario of radar imaging which allows for the detection of a much greater range by movement of the transmission antenna. This can be seen such applications as aircraft topography; the antenna on the plane would transmit signal to a landscape while the antenna is moving. To create a fixed electronic SAR imager, the design will be constructed with multiple stationary antennas that emit or receive pulses to emulate the theory of an SAR.

This project will consist of twenty horn antennas: sixteen receive and four transmit. The antenna structure will consist of two linear antenna apertures. Each aperture will contain eight receive antennas placed between two transmit antennas. Two antenna apertures will be utilized and laid across each other creating a T-shaped design with each horn directed towards the target. Besides the center horn antennas, each horn will be angled directionally towards the target. Overall, the design will create four rows of five antennas being placed orthogonal to each other, creating sixteen phase centers per linear antenna aperture and thirty-two phase centers for the whole design. A phase center is the half-way distance between one transmit and one receive antenna in an aperture and represents a receive antenna's center absorbance point or maximum absorbance point. One transmit is responsible for eight phase centers. When placing receive antennas next to each other, additional maximum absorbance points are created. One aperture may only have eight receive antennas but eight additional phase or maximum absorbance points are created. More phase centers results in a better chance to receiving a return signal. For this project, radar system is required to reach a target twenty feet away and cover a human's body.

The system will be controlled via an FPGA which will sequentially transmit pulse from an antenna and then turn on the receiving antennas/turn off the transmitting antenna pulse to receiving a signal bouncing off the target. This will be done from every orthogonal direction one after the other to give the most data possible. The data would get sampled on a scope and get recorded. If time permits, the FPGA can do more complicated tasks such as storing some of the data that can be output and operated on. This sampled data could then be captured and sent to a PC for image processing. This would most likely be done using software such as Simulink. Overall the goal of this project is to apply engineering design practices and technical knowledge to create a physical schematic of an SAR Imager which would transmit and receive pulse from at least one row of antennas out of the four orthogonal rows.

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1 Introduction

1.1 Acknowledgements

The electronic Synthetic Active Aperture Radar (SAR) Imager team would like to extend thanks to the stakeholders of this project from Northrop Grumman and the FAMU-FSU College of Engineering sponsors. First and foremost to the corporate sponsors at Northrop Grumman, we are most grateful for the generous $50,000 financial contribution to the FAMU Foundation to support research, equipment procurement, and work efforts on the project. In addition to financial contributions, the team also thanks Northrop Grumman for resource support from Peter Stenger, who continually provided technical support, guidance, and direction throughout the duration of the project. We would like to thank Dr. Michael Frank, Dr. Simon Foo, Dr. Shonda Bernadin, Dr. Bruce Harvey, and Dr. Rajendra Arora from the Electrical & Computer Engineering Department for their continued efforts to advise the team in making practical engineering design decisions. Also, we would like to thank Dr. Nikhil Gupta, Dr. Emmanuel Collins, Ricardo Aleman, and Samuel Botero from the Mechanical Engineering department for their contributions in developing professionalism, providing continuous feedback for improvement, and supporting the mechanical design of the SAR Imager system. The team also thanks Dr. Okenwa Okoli, Dr. James Dobbs, Emily Hammel, and Margaret Scheiner from the Industrial Engineering department for their help in project management, scheduling, and quality engineering. Finally, we extend our deepest gratitude to Mrs. Donna Butka for her patience and diligence in processing purchase orders and handling all of our large purchase needs throughout the duration of this project. We also thank her for continuously working with us to process team reimbursements and communicating with the FAMU Foundation to provide the team with the most up to date information pertaining to team finances.

1.2 Problem Statement

1.2.1 General Problem Statement

The number one priority of this project is to create a physical schematic of a radar system with synthetic-aperture radar theory using COTS (commercial off the shelf) components. The theory behind an SAR Imager requires a mobile transmission and receiving antenna to capture a greater range and/or clearer image of what is being targeted. Since a mobile antenna would require a device which moves the antenna and the team does not have the capability or timeframe to make such a device, we will supplement the framework of a single moveable antenna with a system having multiple antennas to emit and receive signal from different locations. The theory behind emitting and receiving signals on a single target from multiple locations will still be implanted, but instead of using one moving antenna the team will use multiple stationary antennas that emit and receive signals from different locations.

1.2.2 General Problem Solution

The solution will be tackled in several steps. There are three disciplines to this project: Electrical/Computer Engineering, Mechanical Engineering, and Industrial Engineering.

The Electrical/Computer Engineers will design a stationary schematic of a radar system which has twenty antennas overall with sixteen being receive antennas and four being transmit antennas. These antennas will be separated into four rows of five antennas each. Each of these four rows will be placed orthogonal to each other, and there will be an epicenter between these four rows which is where the target will be. The rows of five will be separated by twenty feet in each direction from the target, and the system that controls the emitting and receiving of signal from the antennas will be controlled via an FPGA. It is the job of the Electrical/Computer engineers to design a workable schematic of the system that receive and emit signals from at least one row of antennas. This also includes the programming of the FPGA board, signal processing, and possibly even image processing of data if the project goes further than expected. The Electrical/Computer Engineers will be the ones to determine almost all of the theory and components of the system, thus making them the base of the project.

The Mechanical Engineers will design the physical structure of the antennas and the associated horns that go with them. The Mechanical engineers will work very closely with the Electrical engineer who specializes in antennas to design the proper horn shape and the spacing between each of the antennas. The Mechanical Engineers also have a role in helping the Electrical Engineers set up all of the components and equipment of the system and making sure that they are working properly as well. It is vitally important for the Mechanical and Electrical Engineers to work in close contact since the Mechanical portion of this project deals with the physical design of the antennas which transmit and emit signal.

The Industrial Engineers have a primary role in managing the human factors, risk analysis, the project schedule, and the overall budget of the system. The Industrial Engineers will also be in charge of helping the Electrical Engineers acquire and order the specific components needed for the system. Industrial Engineers will also be in close contact with the school and the sponsor since they will be the ones who actually go and submit the orders for purchase. Industrial Engineers will also be of utmost importance when making administrative decisions within the team due to their knowledge of cost engineering and optimization.

1.3 Operating Environment

The operating environment will be those locations of primary concern for homeland security applications such as airports, public schools, museums, etc. These locations will demand that the SAR Imager properly functions at average room temperature (293.15 – 298.15 K) and within average humidity (30 – 50%) [1]. The SAR Imager should be able to operate in the presence of other electronics and RADARs and not be influenced by them in their main operation: determining the hidden threat of hidden weaponry. This system should be able to operate at a nonstop pace when needed and also be equipped with adjustments to be set-up in the specified location on interest.

1.4 Intended Use(s) and Intended User(s)

1.4.1 Intended Use

The intended use for the SAR Imager will be for theoretical implementation and testing. Tests to check for the transmission and receiving of pulse by the antennas of this project will be the primary use for the system. A mannequin will act as the target to abide by FSU campus medical standards. If time allows, more complicated aspects such as image processing can be used to generate an image.

1.4.2 Intended Users

The intended users for the SAR Imager will primarily be the student members of the team. Any advisors or the sponsor may want to test out the system for themselves to check progress and that is a viable option as well. As a research project, this project only intends for an operating physical schematic of the project, not a fully functional prototype. The end result should have a physical system that transmits and receives signal that is controlled/timed via an FPGA.

1.5 Assumptions and Limitations

1.5.1 Assumptions

This project is based upon the following assumptions:

- The radar should operate at frequencies safe for human interaction.
- The radar must be capable of detecting metal and/or threatening objects on a person's body from a distance.
- The radar must be operating at near real-time.
- The data from the receiver should generate polynomial images on a display screen. Then based on color identification, it should be easy to pin point an object's location. A selected color would represent a received signal, and if that color appears on the screen, an object has been located.
- The field programmable gate array (FPGA) board must have a clock of 100 MHz.
- The FPGA board should have Peripheral Module (Pmod) connectors to add analog-to-digital (A/D) and digital-to-analog (D/A) converters.

1.5.2 Limitations

The decisions in this project are confined by the following limitations:

- The distance to the scene to be imaged must be 20 feet. (REQF-002)
- The area to be imaged, also known as scene extent, must cover the width of a person and should ideally cover the person's torso and legs. However, the scene extent will be based on the type of horn antennas selected. (REQF-003)
- The frequency range should be within the X- or Ku- band operating frequency, which is a range of 8 to 12 GHz for X-band and 12 to 18 GHz for Ku-band. (REQF-001)
- The cross range and down range resolution are determined based on the employed beamwidth and distance between the antennas and target. (REQF-004)

- The down range resolution must be low so it does not take a thorough image of the body, but has enough depth. (REQF-005)
- The pulse width should be at about 20 nanoseconds so the pulse can travel to and from the scene. (REQF-006)
- The number of phase centers for the system is sixteen. (REQF-010)
- The number of antennas to be used for the system is sixteen receive antennas and four transmit antennas. (CONS-001)
- Antennas must be placed close together at equal distances apart and be precisely pointed at target. (CONS-002)
- To use the system for testing, the room must be bigger than 20 feet x 15 feet.

1.6 End Product and Other Deliverables

1.6.1 Synthetic Active Aperture Radar Imager

The SAR Imager system will be designed and physically implemented by April 2015. The sponsor in particular does not have a deadline, but the College of Engineering's deadline for completion of projects is April 2015. The end product of this project will be a testable conceptual design of an electronic SAR Imager. The electronic SAR Imager will have the ability to receive and transmit pulses on at least one row of antennas out of the four 90º rows on the whole prototype. A list of the electrical system components are shown below:

- 1 Field Programmable Gate Array (FPGA) board
- 4 Transmit Antennas
- 16 Receive Antennas
- 1 Voltage Controlled Oscillator (VCO)
- 1 IQ Demodulator
- 1Single Pole Double Throw (SPDT) Switch
- 1Single Pole Four Throw (SP4T) Switch
- 1Single Pole Sixteen Throw (SP16T) Switch
- 2 Frequency Multipliers
- 2 Low Noise Amplifiers (LNA)
- 1 Super Ultra Wideband Amplifier
- 2 Ultra Wide Bandwidth Amplifiers
- 3 Fixed Attenuators
- 2 Variable Attenuators
- 1 Power Amplifier
- 2 Band Pass Filters (BPF)
- 1 VGA Display
- 4 Analog-to-Digital Converters
- 1 Power Supply Board
- 1 Computer

1.6.1 Documentation and Configuration Flash Drive

1.6.1.1 Electronic Circuit Schematics

The electronic circuit model developed will be saved in different formats to the Documentation and Configuration flash drive. This will be completed by April 2015.

1.6.1.2 Antenna Structural Schematics

The structural design of the antennas and the supporting system will be saved to the Documentation and Configuration flash drive. This will be completed by April 2015.

1.6.1.3 Code and Configuration Files

The VHDL code and configuration files developed for the electronic SAR imager will be organized in a .zip file and saved into the Documentation and Configuration flash drive. This will be completed by April 2015.

2 System Design

2.1 Overview of the System

The goal of the project is to create a functioning, two-dimensional, static Synthetic Aperture Radar (SAR) and have it detect metal in a scene extent of 30x30 inches. A typical SAR is active, utilizing the movement of one antenna to simulate multiple receive antennas after transmitting a signal, generating multiple phase centers. A phase center is the midpoint between transmit and receive antennas. Based on the time the signal takes to return and the phase center the reflected signal collides with will determine the phase of the signal. From the signal's phase, the location and formation of the object can be established with advanced signal processing. The radar system for this project is static, meaning immovable and relies on the moment of the object. To create a static SAR, multiple horns antennas will be aligned together, similar to the layout of a phased array system. Then, one of the end horn antennas will transmit a signal and have the neighboring horn antennas switch on and off to create the multiple phase centers, similar to an active SAR. If multiple radar components are configured correctly (as described by the User Manual located in Appendix A) and the signal processing is efficient, the static SAR design for this project will be able to determine where an object with a high radar cross section is located on a screen, based on two-dimensional imaging.

2.1.1 Electrical System Overview

The diagram in Figure 1 shows the electrical system of the multiple antenna radar system. The electrical system is responsible for generating the radio frequency signal that transmits into the scene extent; this is accomplished using a voltage controlled oscillator along with a power amplifier to amplify the power and the 4 transmit antennas to emit the signal. The electrical subsystem is also responsible for receiving the reflected waveform scatterings of the return signal from the target and converting them to digital voltages in order to do the signal processing. This is accomplished through the use the 16 receive antennas, the IQ demodulator, the analog to digital converters, the FPGA and the other components in the receive chain. Another responsibility of this subsystem is to perform the signal processing to generate the imagery. This will be conducted by the computer using signal processing software. Lastly the electrical subsystem will display the imagery on the VGA display.

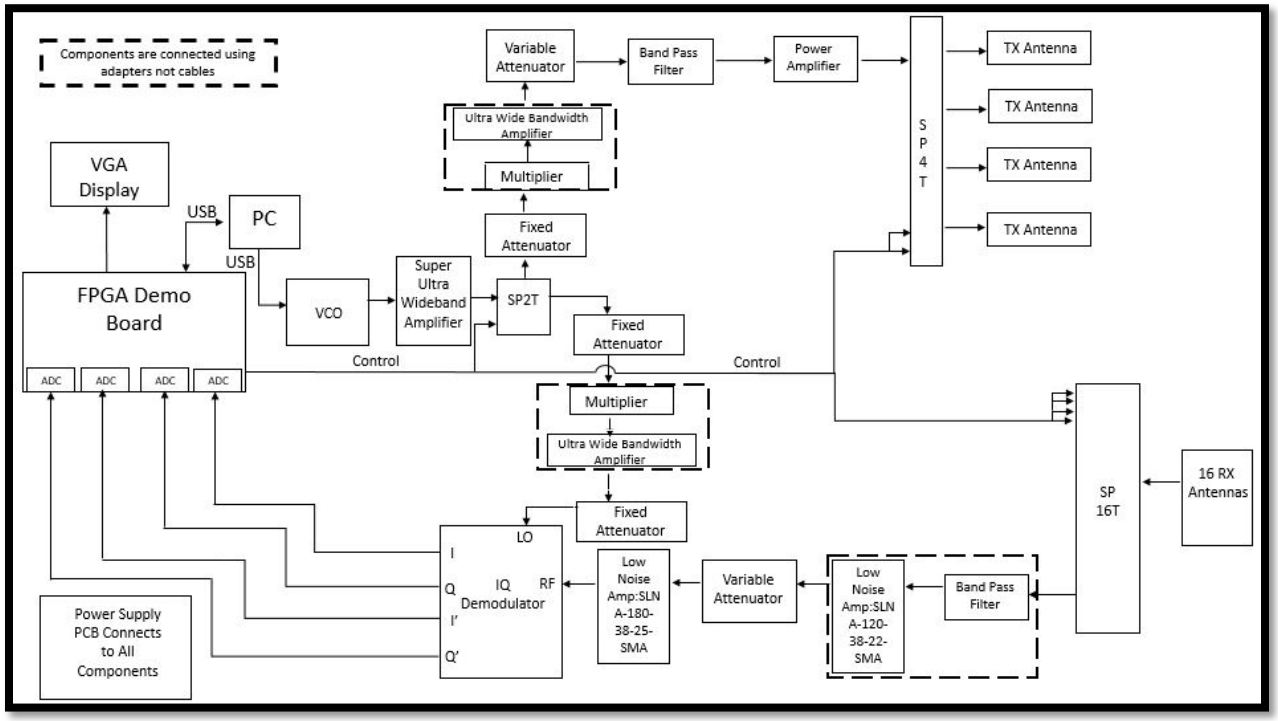


Figure 1: SAR Imager Electrical System

2.1.2 Signal Processing Overview

Figure 2 shows the sixteen phase centers from each transmit and receive antenna pair to the scene. The variable d is the distance between phase centers, θ is the angle from a line with origin at center of array that is 90º to antenna ray to a line from the origin at the center of the array to a point elsewhere in the scene, and θ_n represents the sixteen θs that go to sixteen points in the scene. For each θ, a function with 16 points is generated. The following Table 1 is generated with each of the functions.

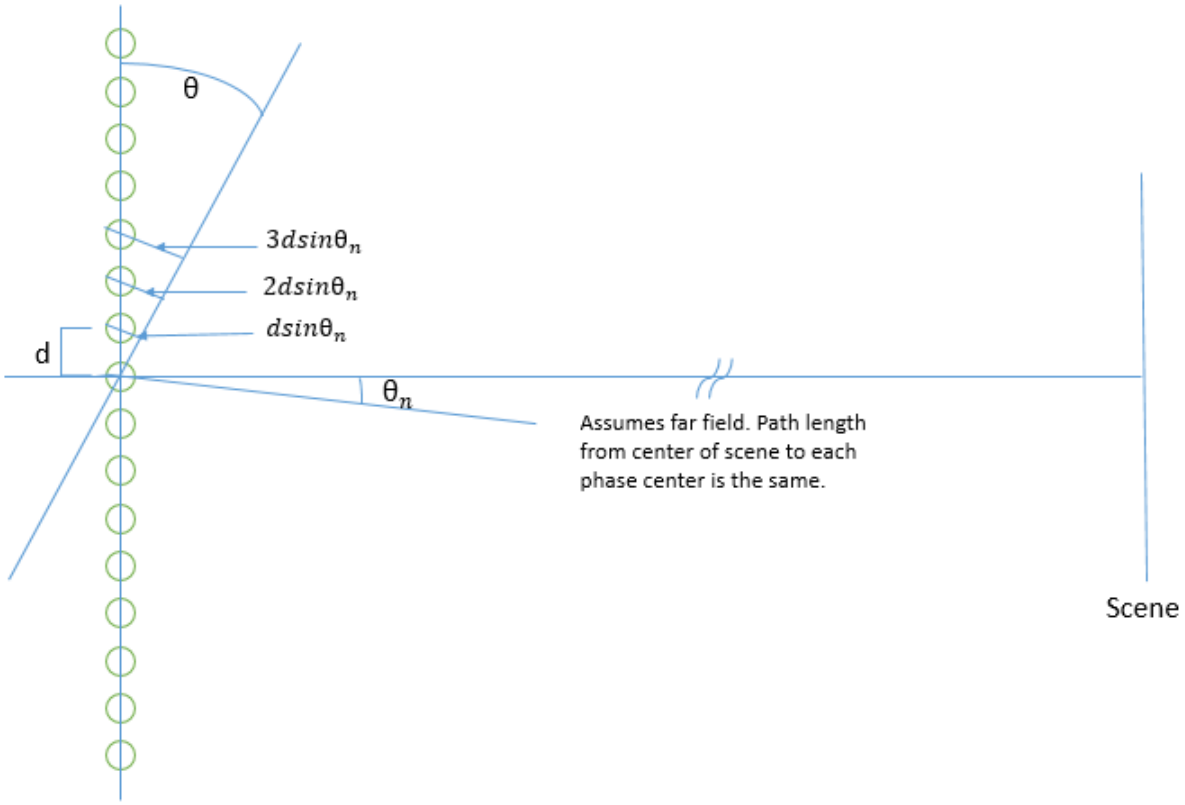


Figure 2: Sixteen Phase Centers from each Tx/Rx Pair to Scene

Table 1: Sixteen Function

	1	2	3	…	15	16
$f(\theta_1)$	$1*d*\sin\theta_1$	$2*d*\sin\theta_1$	$3*d*\sin\theta_1$	…	$15*d*\sin\theta_1$	$16*d*\sin\theta_1$
$f(\theta_2)$	$1*d*\sin\theta_2$	$2*d*\sin\theta_2$	$3*d*\sin\theta_2$	…	$15*d*\sin\theta_2$	$16*d*\sin\theta_2$
$f(\theta_3)$	$1*d*\sin\theta_3$	$2*d*\sin\theta_3$	$3*d*\sin\theta_3$	…	$15*d*\sin\theta_3$	$16*d*\sin\theta_3$
…	$1*d*\sin\theta_n$	$2*d*\sin\theta_n$	$3*d*\sin\theta_n$	…	$15*d*\sin\theta_n$	$16*d*\sin\theta_n$
$f(\theta_{15})$	$1*d*\sin\theta_{15}$	$2*d*\sin\theta_{15}$	$3*d*\sin\theta_{15}$	…	$15*d*\sin\theta_{15}$	$16*d*\sin\theta_{15}$
$f(\theta_{16})$	$1*d*\sin\theta_{16}$	$2*d*\sin\theta_{16}$	$3*d*\sin\theta_{16}$	…	$15*d*\sin\theta_{16}$	$16*d*\sin\theta_{16}$

Each of these functions generates a linear phase slope versus frequency that can be evaluated in Excel. Then each of the functions can be taken and broken into real and imaginary parts. Table 2 is generated with each of the functions for the real part and Table 3 is generated for the imaginary part.

Table 2: Real Part for the Sixteen Functions

	1	2	3	…	15	16
f($real\theta_1$)	cos(d*sinθ_1)	cos(2*d*sinθ_1)	cos(3*d*sinθ_1)	…	cos(15*d*sinθ_1)	cos(16*d*sinθ_1)
f($real\theta_2$)	cos(d*sinθ_2)	cos(2*d*sinθ_2)	cos(3*d*sinθ_2)	…	cos(15*d*sinθ_2)	cos(16*d*sinθ_2)
f($real\theta_3$)	cos(d*sinθ_3)	cos(2*d*sinθ_3)	cos(3*d*sinθ_3)	…	cos(15*d*sinθ_3)	cos(16*d*sinθ_3)
…	cos(d*sinθ_n)	cos(2*d*sinθ_n)	cos(3*d*sinθ_n)	…	cos(15*d*sinθ_n)	cos(16*d*sinθ_n)
f($real\theta_{15}$)	cos(d*sinθ_{15})	cos(2*d*sinθ_{15})	cos(3*d*sinθ_{15})	…	cos(15*d*sinθ_{15})	cos(16*d*sinθ_{15})
f($real\theta_{16}$)	cos(d*sinθ_{16})	cos(2*d*sinθ_{16})	cos(3*d*sinθ_{16})	…	cos(15*d*sinθ_{16})	cos(16*d*sinθ_{16})

Table 3: Imaginary Part of the Sixteen Functions

	1	2	3	…	15	16
f($imag\theta_1$)	sin(d*sinθ_1)	sin(2*d*sinθ_1)	sin(3*d*sinθ_1)	…	sin(15*d*sinθ_1)	sin(16*d*sinθ_1)
f($imag\theta_2$)	sin(d*sinθ_2)	sin(2*d*sinθ_2)	sin(3*d*sinθ_2)	…	sin(15*d*sinθ_2)	sin(16*d*sinθ_2)
f($imag\theta_3$)	sin(d*sinθ_3)	sin(2*d*sinθ_3)	sin(3*d*sinθ_3)	…	sin(15*d*sinθ_3)	sin(16*d*sinθ_3)
…	sin(d*sinθ_n)	sin(2*d*sinθ_n)	sin(3*d*sinθ_n)	…	sin(15*d*sinθ_n)	sin(16*d*sinθ_n)
f($imag\theta_{15}$)	sin(d*sinθ_{15})	sin(2*d*sinθ_{15})	sin(3*d*sinθ_{15})	…	sin(15*d*sinθ_{15})	sin(16*d*sinθ_{15})
f($imag\theta_{16}$)	sin(d*sinθ_{16})	sin(2*d*sinθ_{16})	sin(3*d*sinθ_{16})	…	sin(15*d*sinθ_{16})	sin(16*d*sinθ_{16})

When the real part is graphed, each function plots out as sinusoidal functions of different frequencies, and these are 90° out of phase with the imaginary part. The real and imaginary functions become the basis functions and they will be stored in the VHDL code. They will need to be converted from decimal to fixed point so that they can be operated on.

The hardware provides sixteen I and Q values based on measured data from each of the sixteen phase centers. The IQ demodulator generates sixteen Is at sixteen points, which are the real part, and sixteen Qs at sixteen points, which are the imaginary part, and they are analog voltage values that represent real and imaginary parts of measured return from the scene where the energy is coming in from different angles.

For each angle θ, the image energy at θ can be calculated doing the complex multiply using the following Equation 1:

$$\left[\left(R_{n,\theta n}\right) - j\left(I_{n,\theta n}\right)\right] \times \left[\left(I_{nd}\right) + j\left(Q_{nd}\right)\right]$$

Equation 1: Complex Multiply for Basis Function and I and Q Data

This equation can be applied sixteen times for each of the sixteen points with all θs. It can be simplified in the following manner with Equation 2 for the real part and Equation 3 for the imaginary part:

$$f(realcomp\theta_n) = \left(R_{n,\theta 1} \times I_{nd}\right) + \left(I_{n,\theta n} \times Q_{nd}\right)$$

Equation 2: Complex Multiply for the Real Part

$$f(imagcomp\theta_n) = \left(-I_{n,\theta n} \times I_{nd}\right) + \left(R_{n,\theta n} \times Q_{nd}\right)$$

Equation 3: Complex Multiply for the Imaginary Part

In order to get the amplitude for each of the sixteen functions, the real part of each of the sixteen functions for each of the thetas will have to be summed and the total sum will be squared, and the same will be done for the imaginary part of each of the sixteen functions for each of the θs. Then these squared values obtained, named $real_{\theta n}$ and $imag_{\theta n}$ in this case, will be used to finally calculate the amplitude to be graphed with the following Equation 4:

$$A_n = 20 \times \log\left[\left(real_{\theta n} + imag_{\theta n}\right)^{1/2}\right]$$

Equation 4: Amplitude for Each Angle

For image formation, the sum of the energy from some of the scatterers is taken and they are decomposed by multiplying them by the basis functions. The basis function represents the energy that will come in from a different angle, so if it is multiplied by the total energy, it decomposes it into just that part.

With Fourier transform, the amplitude versus time is being calculated; however, in this case, the amplitude versus angle is being calculated. Fourier transform is used to decompose the waveform into the amounts of energy that come in from different angles. Instead of having a coefficient that represents energy at a frequency, the coefficient of energy that come in at a certain angle is being represented. All of these calculations are part of the long version of the complex Fourier transform at a more physical sense. Appendix 10.1 shows an example done for the signal processing for further explanation.

2.2 Major Components of the Electrical Subsystem

2.2.1 Transmit Chain

The transmit signal chain is responsible for generating the radio frequency (RF) signal that will propagate throughout the entire radar system. The transmit chain is designed such that the frequency of the signal will be in the X band frequency range, 10 GHz. In order to generate the RF signal a voltage controlled oscillator was used in the design. The VCO however generates a low frequency and low power signal. In order to compensate for the low power signal a couple of amplifiers are used in the transmit chain as well as a frequency multiplier. The transmit chain also has two switches, a SPDT and a SP4T switch. The SPDT allows the system to switch between transmit and receive mode. The SP4T switch in allows the system to switch between the four transmit antennas.

2.2.2 Receive Chain

The receive signal chain is responsible for receiving the reflected RF signal scatterings from the target objects in the scene extent. This will be accomplished by using the 16 receive antennas of which will be sampled from one at a time through the use of the SP16T switch. The

receive signal chain is also responsible for passing the signal to PC where the signal processing will take place. In order for the signal processing to take place the necessary phase and amplitude of the signal must be obtained. This is handled by the IQ demodulator. However before the phase and amplitudes of the received signal can be processed they have to be converted to digital voltages, this is done by the analog to digital converters onboard the FPGA. Once those voltages are converted they are sent to the PC for signal processing. The PC then returns the processed imagery to the FPGA and it is sent to the VGA to be displayed.

2.2.3 IQ Demodulator

The IQ demodulator is a very important component in the electrical subsystem. As stated earlier, it is responsible for interpreting the phase and amplitude of the received signal and converting that information into voltages. The IQ demodulator is connected to both the transmit and receive chains. In short, this is based on the fact that the phase and amplitude are generated when a signal is applied to the LO channel; so each time the system switches to receive mode i.e. when a signal is inputted into the LO channel, the IQ demodulator outputs the phase and amplitude information from the I and Q channels.

2.3 Subsystem Requirements

2.3.1 Transmit Signal Chain

The purpose of this subsystem is to generate and transmit a radio frequency (RF) signal that will be emitted into the area to be scanned by the radar. This subsystem is also responsible for establishing an operating frequency for the entire radar. The signal generation starts with the voltage controlled oscillator (VCO). The VCO used in the design has an output power of -4dBm (0.398 mW) and operates at a frequency range of 4.38 GHz – 5.1 GHz. The next component in the signal transmit chain is the super ultra wideband amplifier. This amplifier was placed here because it was needed to provide enough input power into the frequency multiplier. The gain of this amplifier is 26dB. An important concept that was taken into consideration is the 1dB compression point (P1dB). This is the point in which the gain for linear amplifiers is no longer fixed for that specific frequency range. It is at this point where the output power becomes compressed and is no longer linearly proportionate to the input power. The P1dB for this component is 24 dBm, thus while completing the analysis the output power from the wideband amplifier was confined to less than 24 dBm. Also it is good engineering practice to leave a margin of error when calculating the output power therefore the output power from this component was designed to be 21.804 dBm (151.501 mW). The VCO and wideband amplifier are connected by a cable of which the calculated gain is -0.200 dB. The next component in the chain is single pole double throw (SPDT) switch. This component allows the radar to switch between transmit and receive modes. The SPDT switch has a P1dB value of 27 dBm and a gain of -2 dB; with an input power of 21.530 dBm the output power from the SPDT was calculated to be 19.530 dBm. The next major component in the signal transmit chain was the frequency multiplier. The purpose of the frequency multiplier is to double the input frequency. As stated before, the frequency generated by the VCO is in the range of 4.38 GHz – 5.1 GHz, once the signal reaches the frequency multiplier it is then doubled to the desired range of approximately 10 GHz. Due to the restriction of the input power to the frequency multiplier being 12 dBm, a

fixed attenuator was added to the signal transmit chain between the SPDT and the frequency multiplier. The attenuation level set in the calculations is -10 dB; this is considered a loss to the overall gain of the chain.

The next component in the transmit signal chain is a variable attenuator. The attenuation was set to -12dBm. The input power into this component was 8.795 dBm results in an output power of -3.205 dBm. This attenuator precedes a band pass filter as well as power amplifier. This meant that the output power from the amplifier had to be less than 30 dBm which it was calculated to be 25.482 dBm. The band pass filter was used to provide a more accurate frequency for the transmit signal chain. Its center frequency value is 10.5 GHz which is aligned with the frequency that the customer specified. The band pass filter contributes a loss of 3dB to the chain. Next is the power amplifier. The power amplifier has a gain of 30 dB and a P1db compression value of 30 dBm. The output power of the amplifier is 25.482 dBm. After the power amplifier follows a 3dB attenuator and the single pole four throw (SP4T) switch. The SP4T is used to switch the output signal from being emitted by the four transmit antennas. It has an input P1db compression point of 24 dBm and a gain of -2 dB. The output power calculated from this component was 20.364 dBm and was followed by a cable loss of 1.41 dB. The final transmit power generated by this chain was 18.954 dBm. The overall goal in the analysis of the transmission chain is to calculate the power progressed through the path up until the antennas. This is the value that was used in the signal to noise ratio equation. This was accomplished by accounting for the gains and losses of the components in the chain. The transmit power of this signal is to be within the limits of safety as set by the rules regarding safe human exposure to electromagnetic RF fields, set forth by the Federal Communications Commission (FCC). The limit is 10 W/m^2 or 1mW/cm^2, with a scene extent of 40 in^2 (258cm^2) our peak transmit power of 18.954 dBm (78.599 mW) results in 0.0076mW/cm^2. Which is well within the safety limits.

2.3.2 Receive Signal Chain

The purpose of this subsystem is to receive the RF signal scatterings that are reflected from the target and convert those signals to digital voltages to be used in the signal processing. The analysis for this chain includes calculating the power of the signal that it transmitted through this chain as well as the noise figure and noise temperature contributed by each component. The noise figure for components that have a negative gain (loss) is equal to that gain in dB. For components with a positive gain the noise figure is given in the datasheet. Equation 1 for noise temperature for all components is shown below:

$$nt = 290°K(10^{\frac{nt(dB)}{10}} - 1)$$

Equation 5: Noise Temperature

The actual signal power received by the receive antenna is discussed in a later section; for now this value is to be considered as -51.841 dBm. The value seen by the input to the single pole 16 throw (SP16T) switch is added to the gain of -1.41 dB from the cable that connects the SP16T switch to the receive antennas. In total the calculated input power to the SP16T was -53.251 dBm. The SP16T switch has a gain of -4.7 dB and a P1db compression point of 24 dBm. The calculated output power of the SP16T switch is -57.951 dBm which is well below the 24 dBm

compression value. Also because the SP16T switch has negative gain the noise figure is equal to 4.7 dB. The next component in the receive signal chain is the band pass filter. The band pass filter is used to provide precision to the frequency of the received signal scatterings reflected off of the target. The calculated received power for this component is -58.068 dBm, the gain is -3 dB and the output power is -61.068 dBm. The next component in this chain is a low noise amplifier. This component is used to amplify the power of the receive signal and amplify the noise as least as possible. The gain of this amplifier is 38 dB which results in a calculated output power of -23.068 dBm. The calculated output power of this component is less than the P1dB compression point which is 24 dBm. The noise figure listed in the data sheet is 2.2 dB. A variable attenuator was placed in the chain after the low noise amplifier. The purpose of using a variable attenuator is to allow for the power in the chain after this point to be adjusted. In the calculations the attenuation used was -14 dB. This will limit the input power to the RF channel of the IQ demodulator. The next component in the chain is another low noise amplifier. This was added to increase the signal power input into the RF channel of the IQ demodulator. In short the reason that the input power of the RF channel of the IQ demodulator deals with the output DC voltage that will be generated by the IQ demodulator. This concept will be elaborated on later in the paper. The point to note now is that the output power of this low noise amplifier was calculated as 0.540 dBm due to the gain of 38 dB.

The overall goal of the analysis for the receive chain was to calculate the noise power received from the reflections off of the target. This value is with respect to the analog to digital converters which act as the receiver for the entire radar system. In order to calculate this value the noise figure for the entire receive chain was needed as well as the gain. Calculating the gain after the first LNA was straightforward the value was 16.14 dB. However for the entire noise figure the analysis required more thought. In order to calculate the chain noise figure a cascade model was used. This involved calculating the noise figure of the chain as each additional component was added to the chain. At the end of the last component which was the IQ demodulator the noise figure for the entire chain was equal to that value calculated. The equations are shown below:

$$nf_N\,(\text{magnitude}) = nf_1 + \frac{nf_2 - 1}{gain_1} + \ldots + \frac{nf_N - 1}{gain_1 * \ldots * gain_{N-1}}$$

Equation 6: Cascaded Noise Figure

$$nt_N\,(\text{magnitude}) = nt_1 + \frac{nt_2 - 1}{gain_1} + \ldots + \frac{nt_N - 1}{gain_1 * \ldots * gain_{N-1}}$$

Equation 7: Cascaded Noise Temperature

$$N\ (\text{dBm}) = N_n\ (\text{dB/Hz}) + G_{Rx}\ (\text{dB}) + NF\ (\text{dB})$$

Equation 8: Noise Power at the Receiver

$$N\ (\text{dBm/500kHz}) = N\ (\text{dBm}) + 10*\log(500{,}000)$$

Equation 9: Noise power/500kHz

N_n: Thermal noise due to nature = -174dBm/Hz
G_{Rx}: Gain of the receive signal chain after the first LNA = 16.14 (dB)

NF: Noise figure of the receive chain using the cascaded approach = 33.765 (dB)
B_L: Limiting bandwidth of receiver (ADC) = 500 kHz
L_B: Baseband loss approximately 5 dB
P_{RF}: Received signal power at RF channel of IQ demodulator

When calculating the cascaded noise figure it was noticeable that after the first low noise amplifier the cascaded noise figure did not change much. This was due to the relatively high gain of the low noise amplifier in comparison to the other components in the chain. After performing the calculations the noise figure for the receive chain was 33.765dB.

The next step in the calculations was to calculate the noise power at the receiver. This is shown in Equation 8 above. The noise power calculated at the receiver was -124.1dBm/Hz and -67.107dBm per 500 kHz.

2.3.3 Signal to Noise Ratio

$$\frac{S}{N} = \frac{Received\ Power\ at\ Receiver}{\text{Noise Power at Receiver}} = P_{RF} - L_B - N(\text{dBm/500kHz})$$

Equation 10: Signal to Noise Ratio

$$P_r = \frac{P_t G_t G_r \sigma}{4\pi R^2}\ (\text{mW}) = 10*\log(\frac{P_t G_t G_r \sigma}{4\pi R^2})\ (\text{dBm})$$

Equation 11: Received Power

The signal to noise ratio (SNR) is the measure of the ability of a radar to detect a target at a distance away from the radar. Equation 10 is a way in which the target, the radar, the range of the target and the properties of the medium through which the signal will travel are related mathematically. The physical properties of the target that affect the SNR is the target's radar cross section. The radar cross section is the measure of how detectable the object is by a radar. In the analysis the radar cross section was calculated for a trihedral corner reflector. This shape was chosen by the customer; it would have been much simpler to use a sphere however the trihedral was chosen. The lengths of its sides are 0.0508 meters. Equation 12 is used to calculate the maximum radar cross section this trihedral is shown below:

$$\sigma_{\max} = \frac{12\pi L^4}{\lambda^2}\ (m^2) = 10*\log(\frac{12\pi L^4}{\lambda^2})\ (\text{dBsm})$$

Equation 12: Maximum radar cross section of a trihedral corner reflector

The value solved for the radar cross section used in the SNR equation was -5.545 dBsm. The radar characteristics that were used in the SNR equation included the power transmitted and the characteristics of the antenna aperture. As explained before the transmitted power (P_t) was determined by the components in the signal transmission chain and the value calculated was 18.954 dBm (78.599 mW). The properties of the antenna aperture that are used in this equation

are the gain of both transmit and receive antennas. The gain for the transmit and receive antennas are 17 dB.

The signal to noise ratio as shown in Equation 5 uses the signal power at the input of the receiver which in this case is the output power from the IQ demodulator (5dBm). The SNR equation also uses the noise power at the input of the receiver which was calculated using Equation 4 shown above (-25.4dBm). Since these values are calculated in dBm, the SNR results in a value of 55.177dB.

Table 4: Receive Chain Noise Characteristics

Component	NF (dB)	NF	NF (cascade)	Noise Temp (K)	Noise Temp cascade (K)
RX Antenna Cable (36 inches)	1.41	1.384	1.384	111.234	108.800
Single Pole 16 Throw Switch	4.7	2.951	4.083	565.851	452.536
Cable (3 inches)	0.12	1.027	4.195	7.953	471.931
Band Pass Filter	3	1.995	8.370	288.626	1702.715
LNA:SLNA-120-38-22-SMA	2.2	1.660	12.361	191.280	4704.482
Cable (7 inches)	0.27	1.065	12.361	18.898	4704.506
Variable Attenuator	14	25.119	12.369	6994.471	4713.858
Cable (3 inches)	0.47	1.027	12.369	7.953	4713.992
LNA:SLNA-180-38-25-SMA	2.5	1.778	33.764	225.701	689579.460
Cable (12 inches)	0.47	1.114	33.764	33.145	689653.724
RF (IQ Demodulator)	7	5.012	33.765	1163.443	689769.379

2.3.4 IQ Demodulator Chain

The IQ demodulator is a key component in the electrical system. It is used to relay the amplitude and phase of the incoming RF signal to the analog to digital converters. The IQ Demodulator converts the amplitude and phase information to DC voltages. This is done based on the theory of the IQ demodulator. In short this process involves generating a amplitude from the I(t) and Q(t) signals. The amplitude is generated using the equations shown below:

$$\mathrm{A(t)} = \sqrt{I^2(t) + Q^2(t)}$$

Equation 11: Amplitude of RF signal input to IQ Demodulator

$$\phi(\mathrm{t}) = \arctan\left(\frac{Q(t)}{I(t)}\right)$$

Equation 12: Phase of RF signal input to IQ Demodulator

The input power to the RF channel of the IQ demodulator was calculated to be 0.07 dBm, the IQ demodulator has a conversion loss of 7 dB, resulting in an output power of -6.930 dBm (0.203 mW). The output impedance of this component is 50Ω. The next step in the analysis was to calculate the voltage range of the I and Q outputs. This was done by using the equation below:

$$V_{dc} = \sqrt{Pout(W) + Zout(\Omega)}\ (V)$$

Equation 13: Output voltage range

This led to a calculated value for the maximum voltage output by the IQ demodulator as 100mV, which occurs when the phase angle is 45° between signals I(t) and Q(t). However when the phase angle between the two signals is -45° the output voltage of the IQ demodulator is 100mV, which results in an output voltage range of approximately -104mV to 104mV. The DC offset error of this particular model IQ demodulator at the extreme is +/-8mV. As stated before the large increase in gain in the receive path due to the two low noise amplifiers is necessary to increase the power of the input signal in order to allow the IQ demodulator to produce a DC voltage that is high. The DC output voltage needs to be high in order to make the DC offset error negligible. At 8 mV to 100 mV the DC offset error is low compared to the actual voltage. This is causes the DC offset to be negligible which is desirable.

This process occurs when a signal is input into the LO channel of the IQ demodulator or in other words when the SPDT switch is not driving the transmit signal chain. This is the reason for the SPDT switch which switches the radar between transmit and receive modes. The input signal must have a power of 5 dBm. This is the reason for the variable attenuator that comes after the SPDT switch, it is necessary to decrease the signal power that is amplified by the wideband amplifier to 5.599 dBm.

2.3.5 Power Supply Board

The power supply board was designed to generate and distribute the necessary operating voltages and currents to the components in the electrical system. Table 5 below lists the requirements for the components.

Table 5: Power Supply Output Requirements

QTY	Part Name	V+(Vdc)	I+ (mAdc)	V-(Vdc)	I-(mAdc)
1	SPDT Switch	5	1.4	-	-
1	SP4T Switch	5	160	-5	50
1	SP16T Switch	5	550(max)	-12	200(max)
1	IQ Demodulator	5	110	-5	-

1	Super Ultra Wideband Amplifier	12	400(max)	-	-
2	Ultra Wide Bandwidth Amplifier	12	62	-	-
1	Low Noise Amplifier SLNA-120-38-22-SMA	12	250	-	-
1	Low Noise Amplifier SLNA-180-38-25-SMA	12	280	-	-
1	Power Amplifier	15	900	-	-

2.4 Performance Assessment

- ***CAP-001: The radar should roughly have a range of 20 feet.***
  The electrical system is designed such that the range of the radar is 20 feet (6 meters). In the design of the system the 6 meter range was set constant when doing the calculations for other quantities such as the peak transmit power and receive power.

- ***CAP-002: The radar's operating frequency needs to exist within the standard radar spectral bands, typically around X or Ku bands.***
  The operating frequency of the electrical system is 10 GHz, which is within the X band frequency range. This frequency is established using the VCO which outputs a signal at the frequency of 5 GHz and the frequency multiplier doubles the frequency of the signal.

- ***CAP-003: The radar should operate at frequencies/signal levels safe for human interaction.***
  The operating frequency is 10 GHz. The peak transmit power of the signal 18.97 dBm (78.886 mW) at this operating frequency and power the system is safe for humans to interact with. According to the Federal Communication Commission's rules on electromagnetic radiation the limit is $10W/m^2$.

- ***CAP-004: The radar must be capable of detecting metal and/or threatening objects on a person's body from a distance.***
  From a distance of 20 ft, a reflected signals from the trihedral device used was able to be picked up by one of the receive antennas. To justify that the trihedral was actually reflecting the transmitted signal, it was moved in different direction and noticeably the return voltage readings would change based on the position of the trihedral. The highest return voltage level was when the trihedral was positioned directly in front of the antenna at the desired range of 20 ft., which was theoretically expected.

- ***CAP-005: The radar must be operating at near real-time.***

  The radar system is designed to be a near time display that corresponds to where a metal object is in the scene. As a backup, non real time display of results from the transmit receive aspect of the project is implemented. For the system demonstration, non real time display of results was shown using switches on the FPGA to show the different results depending on the transmit receive antenna combinations. To make the system real time, all that needs to be done is to add a counter to give a certain amount of time each transmit receive combinations is on for. The code in the project was implemented in such a way that the logic of the code for the timing does not have to be changed, and that the only thing that needs to be added is a counter instead of using switches.

- ***CAP-006: The radar's width of detection should cover the narrowness of an individual person.***
  The beamwidth of each horn antenna, employed in the radar system, needed to cover at least a 40x40 inch area. This area is the projected scene extent to cover the human torso where weapons or dangerous material would be carried on the human body. The horn antennas utilized in the design have gain levels of 17 dBi, which corresponds to each antenna having a beamwidth that covers an area of 9x9 feet, which easily covers the scene extent and is almost too large. A large beamwidth means reflections from objects outside the desired scene extent.

- ***CAP-007: The data from the receiver should generate an image.***
  The signal processing calculations for image formation were not implemented by the end of the project. The sixteen receives were not fully tested as the SP16T switch arrived very late. The RF foam was not acquired on time; therefore any I and Q data obtained by performing the transmit and receive would not yield accurate values. The signal processing calculations were realized on an Excel spreadsheet, and these functions were not translated into code for the FPGA to process and output an image on the VGA display.

2.5 Design Process Changes

2.5.1 Level Shift Circuit

The level shift circuit was initially designed to allow the two analog to digital converters to sample the negative voltages generated by the I and Q channels of the IQ demodulator. The level shift circuit was removed from the overall design and was replaced by using two additional analog to digital converters which sampled the I' and Q' channels of the IQ demodulator. In total there are four analog to digital converters. Changes to the software allows the FPGA to recognize when the I and Q channel generate negative voltages. This design works because when the I channel voltage is negative the I' channel voltage is positive, same for the Q and Q' channels. The ADCs can only accept positive voltages, thus when the ADC for the I channel is negative the ADC for the I' channel will be positive and the FPGA will do the signal processing on the positive voltage only. This also applies to the Q and Q' channel. Figure 2 shows the changes in the Level Shift Circuit Design.

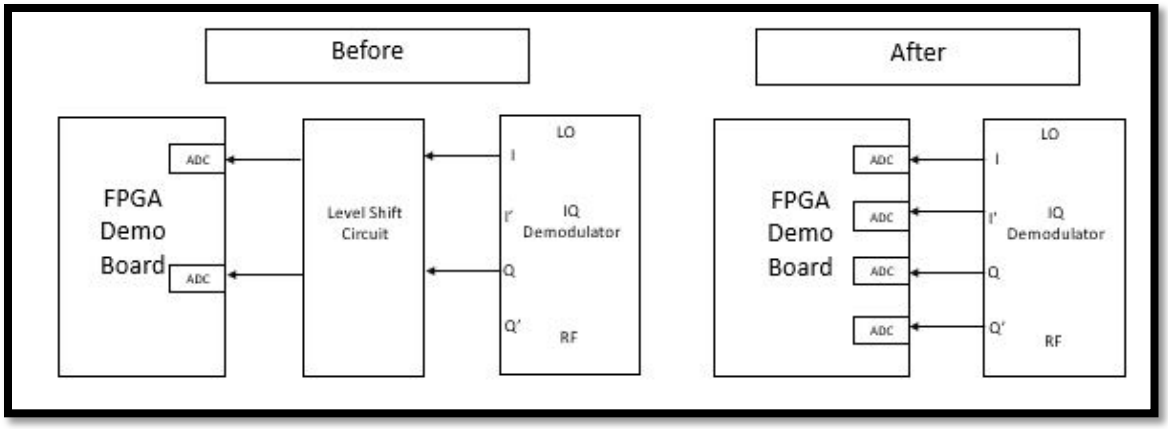


Figure 3: Level Shift Design Change

2.5.2 Improvises

2.5.2.1 VCO

The signal from the VCO is designed to have a frequency of 5 GHz and once it is multiplied by a factor of two with the multiplier, the transmit signal is to be 10 GHz. However the VCO would never generate a signal with a frequency of 5 GHz, the maximum frequency obtained was 4.631 GHz, 9.26 GHz once it was output by the frequency multiplier. The minimum frequency of the passband of the band pass filter is 9.75 GHz. Therefore the VCO was replaced by using a RF signal generator that could generate a signal of -4dBm and 5 GHz.

2.5.2.2 FPGA to SPDT Switch

The FPGA is cable of generating a 20nS pulse with a period of 60nS to drive the SPDT switch. However to generate such signal with a good enough fidelity the pulse had to be delivered through the VHDCI connector on the FPGA board. The VHDCI connector could not be used because it was impossible to solder wires to the pins that would be connected to the SPDT switch. The VHDCI breakout board that would allow the FPGA to interface with the SPDT switch was not delivered in time to perform testing. If available it would have eliminated the need to use a signal generator to pulse the SPDT switch at 20nS.

2.6 Overall Risk Assessment

The construction of the Imager had a critical path as defined on the Gantt Chart in Appendix E. The following sections outline the potential threats to the successful flow along the critical path and overall project completion. The risks are defined in three strata, Technical Risks, Scheduling Risks, and Budgeting Risks; these sections encompass all potential hazards to the team's ability to reach the expected end product and its deliverables. All risk components will be categorized by their description, probability, consequence, mitigation strategy, and team response.

2.6.1 Technical Risks

The first stratum encompasses all technical risks associated with facilitating the Imager's design, construction, and testing. These risks stem from the hardware implemented, the role of the antenna horns, and influence of the electrical systems on the mechanical structure and vice versa.

2.6.1.1 Mechanical Structure Risks

The following subsections define and mitigate the risks associated with the mechanical frame and structural components integration within the Imager's electrical systems. These risks highlight the ability for the team to effectively accomplish their scope deliverables and define the mitigation strategies necessary to overcome said threats.

2.6.1.2 *Structure Risk 1*: Quadrant Stress Increased by Antenna Horns

Description:
Each quadrant of the structure will have 5 antenna horns attached using a pin and bolt to tighten the antenna after it has been correctly aligned. The risk is associated with the arm of each quadrant. The arm will have increasing deflection as each horn is placed on the structure and if the deflection in the arm becomes too great then the horns will lose their alignment. The horn must be vertically and horizontally aligned to receive the optimal response from the signal pulses. Misaligned horns will distort the image generated from the pulse.

Probability: Very Low
Although deflection is a valid risk to be concerned with, the probability of it occurring is very low. The overall weight of the horns placed in the structure will not cause too much deflection. The material chosen, steel, for the structure will be sufficiently strong enough to avoid deflection.

Consequences: Catastrophic
As time passes, if the material chosen does not withstand the weight of the horns, the arm of each quadrant will progressively bend. Ultimately, it could reach its yield point and become deformed to the point where it will lose its elasticity. This will bring the material to eventually fracture. This is catastrophic and will permanently disrupt the signal pulses until the structure is repaired.

Strategy:
Approaches to prevent risk:

1) One way to prevent the effects of over deflection is to be sure the material chosen has been analyzed and calculated to have a yield strength beyond the force of the horns against the arm of the quadrants. This will reduce the amount of deflection in the material and allow the horns to be correctly aligned with one another.

2) Another way to prevent deflection in the quadrants is to properly assembly quadrants with the C-shape brackets. The brackets all custom made to hold the quadrant in a rigid manner to prevent the arm of each quadrant from deflecting. When each quadrant is assembled, the forces acting on it will provide for a more secure yield strength. When

each horn is placed into the structure, the forces are equally distributed amongst all of the quadrants.

Team Response:
The Mechanical Team opted to utilize C-Brackets to secure the weight of each quadrant panel and to ensure that all possible deflection of the steel panels was not absorbed by the antennas or the mechanisms use to support them.

2.6.1.3 *Structure Risk 2*: Vertical Component Box Increases Power Loss Risk

Description:
Due to the arrangement of the electrical components, the box must be made in an L shape to provide the best electrical flow through all the wires. The reason the box is made into an L shape is because the FPGA Demo Board must be laid horizontally to the bottom surface while the rest of the components are vertically placed into vertical side of the box. Each component must not fall down the component box. This box will be placed on the back of the structure for the convenience of the consumer.

Probability: Very High
Internal flow through the wires already have major loss applied to them. When the wire is bent in any direction, minor losses are formed reducing the current of the wire. This has a very high potential to occur because the design specifies that the FPGA Demo Board will be laid horizontally. The wires from the FPGA to the resulting components must be bent to properly connect the components. This concludes a minor loss in the wires.

Consequences: Moderate
The main consequence of the component box is that the wires will lose current flow due to minor losses. The consequence is minor because the loss in the wires, from appropriate calculations, do not cause a significant difference. To reduce the amount of loss in the wire is vital, but if the L shape box causes bends in the wire, it will still not be enough to effect the remaining components.

Strategy:
The strategy to reduce/prevent loss in the wire is to lay the whole component box flat. To have all the components on a horizontal plane will remove the minor losses formed from the L-shape component box. Although this is an ideal decision to make, to remove the box for the back of the structure and lay flat on a standing stool, the consumer will be at an disadvantage because the structure should be used as a whole.

Team Response:
A wiring diagram was construct and a heat analysis was performed to ensure that the correct placement of components was ensured.

2.6.1.4 Structure Risk 3: Unaligned Structure Stand can Increase Redirect Signal

Description:
The antenna structure must be held upright for proper use of the antennas. This allows each antenna to be directed to the target with much precision. The structure will be held up by a base stand that can support the weight of the entire structure including the component box. The way the stand is joined to the structure is through a pin and slot joint. A rectangle male end on the stand will be inserted into a female end of the structure. If the joint connection is not perfectly fabricated or wears over time the structure will not properly stand upright and may fall to one side of the stand. The leaning will be caused by the uneven center of gravity on the structure.

Probability: Moderate
The probability of this risk occurring is moderate. With the dimension we chose for the joint and the results produced when Metal Fabrications constructs the product, there can be error that will cause the joint to not fit as desired. This company has proven its ability to perform to our satisfaction; which is why the probability is at Moderate and no higher.

Consequences: Moderate
The consequences associated with this risk are also moderate. Through calculations of the bore sight for each antenna, it can be noted that even with a slight alignment, the signal pulses have a wide enough range to capture the target as intended. The beam width was calculated to be 25 degrees which is appropriately wide enough to account for error of misalignment in the stand for the structure.

Strategy:
Approaches to prevent risk:

1) The first approach to prevent risk is to be sure all error has been calculated. After calculation, find the appropriate way to reduce the error in the calculation so that the joint connecting the stand to the structure will be rigid enough to hold the antennas in the necessary alignment.
2) If the risk has come to fruition, then a way to repair the problem is to use a seal that will close the gap in the joint. This is called a square cut O-ring that will replace the air gape in the joint and provide a rigid body for the structure-to-stand connection.

Team Response:
This risk did not occur, but the Mechanical Team kept an open communication with the company to ensure that the product was being produced correctly. There were errors with the quadrant panels and horn holding apparatuses, but these were corrected once a problem had been noticed at the fault of the manufacturer.

2.6.2 Electrical Systems Risks

The following subsections define the risks and threats presented by the challenges that are encompassed under the electrical systems of the imager. The risks analyze the factors that are needed to establish the subsection and illustrate the ability for that step to delay the project

schedule. Each subsection provides a clear definition of the mitigation strategies that the team will employ in the event that these risks develop into issues.

2.6.2.1 Component Failure

Description:
The components in the electrical system all have absolute maximum values for characteristics such as input and output voltage, current, power as well as other characteristics. These limits are set by the vendor with the guarantee that the components will operate as they were designed to do so. However if any of these maximums are exceeded the components can become electrically stressed and it is no longer guaranteed that they will operate as they were designed to.

Probability: Low
During the design process the absolute maximum values for each of the characteristics specified were taken into consideration. Good engineering practice was used when designing the electrical system in order to ensure that the maximums were not reached. For example, for components such as the amplifiers and the switches the output power from those components was calculated with enough margins so that P1dB compression points would not be reached.

Consequence: High
If any of the components in the electrical system were to become electrically stressed this could cause the entire electrical system to fail. For example, if the VCO was to become stressed there would be not RF signal generated, or if the SPDT switch was to fail the radar could get stuck in either transmit mode or receive mode.

Strategy:
When designing the electrical system the maximum thresholds were taken into consideration. In order to ensure that they were not exceeded the values used to calculate each characteristic were below the absolute maximums.

Team Response:
The team responded to these threats by ensuring that a binder containing all data sheets for the components was kept with the components at all times so that if any team member was utilizing them then they would be able to clearly look up these values. These values were also noted with the Testing Plans to ensure proper use and operation did not destroy these devices.

2.6.2.2 Software Development Risk

Description:
During the design process, the software design may be inadequate or incomplete as far as the scope of the project is hoped to reach. This includes generating code that will allow the FPGA to generate pulses, control timing of the switches, and if needed the signal processing of the results recorded. This may delay the testing strategies of the project time line and/or completion of the whole project itself.

Probability: Moderate
The coding level required to generate the pulses and timing for the system is not inherently difficult. The only difficulty that may arise will be just figuring out how to match the correct timing with the physical implementation of the project which could include unknown factors. If the PC cannot be used to do image processing using a program like Labview, then the image processing on the FPGA would be another factor that might be difficult to complete. This is because the FPGA used for the system (Digilent Nexys 3) does not come with image processing software.
Consequence: High
If the pulses and timing cannot be generated properly, then it is very hard to show results from the work of this project. This is a vital portion of the project that must be at least partially working to get some results. These results include anywhere from detecting signal with an RF meter, to having imaging on the VGA display.

Strategy:
If the FPGA cannot be programmed in such a way to generate the signals and the timing required for the SAR system, a very simplified version of the system can be utilized by using test equipment. This new system would include a pulse generator to generate the pulse, and a scope to display the image and that would do the image processing. With this new system the FPGA would not be needed. Overall this is just an extreme backup in case nothing else works for this project. If the PC cannot be used to do the Image processing, then the image processing would have to be done on the FPGA.

Team Response:
This risk did not occur as it was mitigated by taking into account the rise and switching times of all incoming and outgoing signals. The constraints of the FPGA board were also noted when coding. The unfinished sections of the signal processing VHDL code was noted as future work.

2.6.2.3 Interface Outside of Scene Extent

Description:
Radiating antennas propagate a main lobe beam with the strongest signal but also weaker grating lobe beams at symmetrical angles directed away from the target. Grating lobe beams need to be absorbed to allow a clean calibration process of the main lobe beam. If the testing room for the radar system is not properly installed with a type of radio frequency absorbing material, calibration of the SAR Imager could be flawed.

Probability: Moderate
After installing radio frequency absorbance material, the worry about excessive grating lobe beams returning a signal should be obsolete. However, the horn antennas being utilized have low gain values, thus the beamwidths cover a large scene extent.

Consequence: Severe

In order to calibrate the radar system, the only radiating beam from the antennas that can create a return signal is the main lobe beam. If grating lobes bounce off of objects away from the scene, the signal processing of the radar system will become slightly or largely flawed.

Strategy:
In order to prevent unnecessary return signals from objects outside of the desired scene extent, radio frequency absorbance materials needs to be installed around the scene extent. A lab room installed with absorbance material would solve the problem of grating lobes interfering with the return signal from the main lobe beam.

Team Response:
The Anechoic Absorber was never ordered due to the high cost and frequent changes as well as its lateness within the project schedule. This was noted as it being impossible to officially calibrate the reading of the signal. The ordering and design of a proper anechoic chamber was transitioned as future work to ensure a proper operating environment is reached.

2.6.3 Antenna Design Risk

2.6.3.1 *Antenna Design Risk 1*: Phase Center Amount

Description:
The overall antenna design is meant create 16 phase centers per linear antenna array. If the spacing between the phase centers is not relatively precise, the amount of phase centers could fail to equal 32 overall.

Probability: Low
Properly spacing the antennas should not be a challenging task. Multiple tests, using laser pointers and other measuring tools, can reassure the distances between each antenna and theoretically the right amount of phase centers should be create.

Consequences: Severe
If 16 phase centers are not properly created per antenna array, the signal processing calculations could become erroneous. The location where the receive signal generated from could be inaccurate.

Strategy:
Checking the alignment of the antennas will have be a priority to confirm the creation of 16 phase centers. Alignment tools like laser points and measuring apparatus will have to be utilized.

Team Response:
The team procured an aligning laser from Home Depot and focused all antennas into a 1 ft diameter scene to ensure that the antenna were transmitting and receiving as defined by the 3 and 6 lambda phase centers.

2.6.4 Signal Processing Risks

2.6.4.1 *Signal Processing Risks 1*: I-data and Q-data Not Collected

Description:
There is a risk that the data from the I-channel and the Q-channel are not collected from the IQ demodulator and stored in the FPGA board.

Probability: Low
The probability that the data is not collected properly is low as the FPGA board will be programmed to receive the information.

Consequences: Minor
There is an alternate way to get the data without having to rely solely on the programming, so the consequences are not significant.

Strategy:
A voltmeter can be attached to the I-channel and the Q-channel of the demodulator to get the data manually. This measured data will then be entered into an Excel spreadsheet that is set up as a backup, which will then be used to calculate the 16 amplitudes for image formation.

Team Response:

This did not occur was the team utilized 4 AD Converters to read all for voltage readings our of the IQ demodulator to ensure that a positive reading could be interpreted.

2.7 Schedule Risks

The following section depicts how the Gantt Chart's functions affect the successfully completion of the project deliverables. This section focuses on the potential complications as they relate to the critical path (refer to Appendix A3). Each section will note the necessary mitigation strategies and define all consequences of schedule.

2.7.1 Component Ordering

The following subsection illustrates the various areas involved within the component procurement process and highlights the points at which the project plan can deviate from expected.

2.7.1.1 Vendor Approval/Registration

Description:
Accessing funds through the FAMU Foundation requires that a purchase order must be placed with an approved vendor in order to procure the necessary components. Most of the vendors listed in the budget assessment are not currently registered vendors with FAMU, this amounts to additional lead time when acquiring components. The risks associated with this include a vendor not being able to be registers, by either not supplying a W-9 form and accepting purchase orders; or extending the delivery time and by extension extending the time to begin testing.

Probability: Low
The team has contacted the vendors listed in the budget assessment and they are willing to supply W-9 forms and accept purchase orders. The only reason that the vendors would not be registered would be by denial by FAMU, which has been established as a low probability of occurrence.

Consequence: Severe
Should a vendor be prevented from registering with FAMU the team will need to select a secondary vendor and place a separate purchasing order. This consequence was labeled as severe in that purchase orders are only placed for orders that exceed $100; as this may place the team in a situation where they would have to front the money for the part, or extraneous parts would need to be ordered to allow use of purchase ordering. Additionally, should a vendor fail to register with FAMU, the team will have to readjust their testing plan if a part lies along the critical path or the secondary option does not flow with the testing plan currently in place.

Strategy:
The team has placed the necessary information with Donna Butka for ordering so that enough time exists should a replacement vendor need be contacted. The team also in place alternative components, where possible, should the situation arise.

Team Response:
The team responded well to companies that were not able to properly form a Purchase Order with FAMU, mitigation strategies were determined for items and orders develop before March. During March the time to complete the project approached rapidly and issues concerning vendors were of greater concern. The team attempted to overnight all orders to ensure an expedited assurance of all components. Not all parts, however, could be procured within enough time by the project deadline. This includes the absorber, the repaired SPDT, an isolator that was left off of the bill of materials as this was never purchased.

2.7.1.2 Purchase Order & Delivery Lead Time

Description:
The time of delivery of an ordered component is increased by the need to place and process a purchase order through the Department of Electrical Engineering with Donna Butka. This process has an average extension of delivery by 5 business days. This fluid time extension may increase the delivery time beyond what has been planned for extending the waiting time before testing can occur.

Probability: Moderate
The probability for this occurrence was established at moderate with an understanding that the university will be open for only for a few more weeks before the winter break, this may cause an increase in the amount of business days it takes to process requests for a purchase order.

Consequence: Moderate
The consequence for an unanticipated lead time is rather moderate, as the team developed time into the project time line for many components to be ordered in late November. This time frame will allow for an additional five business days to be added unexpectedly.

Strategy:
The team has planned the testing strategy in the project time line behind the longest delivery time (FPGA) so that additional time could be accounted for should the additional business days be required to process the purchasing requests.

Team Response:
This was a constant risk as parts and components were ordered throughout the entire project. The lead times and shipping times were integrated into the schedule so that team members could know when to formally begin testing and integration.

2.7.1.3 Storage Facility

Description:
The delivered components and subassemblies will need to be stored in a secure location large enough to hold the mechanical frame and all of the electrical components, as they arrive. Space within the College of Engineering and other facilities around Innovation Park is especially limited, acquiring an available storage proves to be a challenging aspect to the completion of this product.

Probability: High
There has yet been an available space for the team to store their components and finding such a space has proven rather difficult. The probability was set as high to indicate the necessity and the difficulty in finding a secure location to store all of this equipment at the appropriate testing environment.

Consequence: Severe
Not having a secure and singular location to store all of the test equipment will have severe consequences, such as having multiple storage locations across Innovation Park which may result in the loss of parts and unequal storage conditions that may alter the performance of electrical components. In the event that a secure location is not able to be found, the team has not defined a plan that is most suitable for containing these components.

Strategy:
The team plans to contact the EE/ECE, ME, and IE departments if there is storage within the College of Engineering. The team will also contact the High Performance Materials Institute (HPMI), the Aero-Propulsion, Mechatronics, and Energy Building (AME), and the Center for Advanced Power Systems (CAPS) to determine if there is available storage. In the event that these facilities are not available, the team will contact other centers and institutes throughout Innovation Park.

Team Response:
The team reached out to many facilities and got a response from the Center for Advanced Power Systems who initially allowed testing to happen in their High Voltage Bay, but this space was transition to CAPS 130 where the team was also allowed to safely store and secure the structure and components.

2.7.1.4 Testing Facility

Description:
The need for an appropriate testing facility at the necessary environment presents another challenge. The antenna horns' production of side lobes demand the use of RADAR absorbing foam to prevent the detection of metal from outside the scene extent and the 20 antenna horns require nearly an entire room to be covered in such foam. Additionally, the 20' range of the radar requires that the testing facility also be able to accommodate enough space for at least 8 users for testing. The size of the necessary testing facility presents another challenge when determining the most appropriate facility for testing.

Probability: Moderate
The probability of finding an appropriate facility for testing is moderate for the reason that the EE/ECE department has offered to allow to test in their old portable, which is an all metal container. This may not be the most optimal, but it is a failsafe should other facilities not be able to accommodate our demands.

Consequence: Severe
Without the appropriate facility to test in then the Imager cannot be tested for its effectiveness as defined in the project scope.

Strategy:
The team has contacted the FSU Physics Department about using their Faraday Cage room, and they have contacted HPMI, CAPS, and AME as well to ask about testing availability. The fail safe will be utilizing the portable as described above.

Team Response:
The room that CAPS provided to the team eliminated the risk as this room met the minimum requirements and was a secure location.

2.8 Budget Risks

The following section illustrates the threats to the completion of the project as they relate to the $50,000.00 budget and the methods used to access these funds. The risks will be defined and expressed in means of probability and then will be mitigated by a strategy the team has put into place.

2.8.1 Purchase Order Minimum

Description:
The minimum amount needed to be spent before a purchase order can be placed is $100.00. On components that are valued less than this amount, the design team is expected to front the expense to these components and then be reimbursed by the FAMU Foundation. The stipulation of refunds is that the FAMU Foundation will only reimburse FAMU students, leaving the entire obligation in the hands of only one student.

Probability: High

There are a large number of components that are required that cost less than $100.00, so the chance that the funds will need to be fronted is significant.

Consequence: Severe
Readjusting the order scheduling around the available funds of one student may prevent many components from being ordered in the time allotted and could harm the completion of the project. This event has severe consequences because the already tight schedule can not afford to be extended beyond what it has already been allotted.

Strategy:
The team plans to order all components from one vendor in one order to ensure that the minimum $100.00 is reached with every order. The team also plans to order multiple components where necessary to ensure the a purchase order may be used.

Team Response:
The team handled this risk by ensuring that all orders from similar vendors were placed together to prevent in out of pocket cost to team members. There were cases where team members did need to front the money to the team's PM who then became responsible for distributing the FAMU reimbursement after placing the request for reimbursement.

2.9 Software Risks

2.9.1 System Timing Code Redesign

Description:
The sampling rate for the Analog to Digital Converter was not high enough to sample the original 20 ns pulses that were supposed to go be received in the receive antenna. The sampling rate for the A/D converter was one million bits per second, and the pulse that was being received was 20 nanoseconds.

Mitigation:
This problem was fixed by changing the timing so that the receive signal that goes into the A/D converter would be a pulse train instead of a single 20 nanosecond pulse. This leads to the A/D converter taking the average DC value of the pulse train, giving an accurate signal reflecting off the target.

Team Response:
This risk was acknowledged and fixed, allowing successful system demonstration.

2.9.2 Analog to Digital Conversion overflow error

Description: The Analog to Digital Conversion Code in the midterm hardware/software review had the issue where when the input voltage went to 1.66 V, it would reset from 7FF at 1.65 V and become 000 at 1.66 V and becoming 7FF at 3.30 V. Essentially, at the half way point between the voltage range for the A/D converter, it would reset.

Mitigation: The range for the instructions on the counter of what bit to act on was incorrect.

Team Response: This risk was acknowledged and fixed, allowing successful system demonstration.

2.9.3 Increase in amount of A/D converters

Description: In the original electrical design, there was a level shift circuit that was designed to allow the two analog to digital converters to sample the negative voltages generated by the I and Q channels of the IQ demodulator. When this was deemed unsatisfactory, code had to be written to use four A/D converters to convert and store I, Ibar, Q, Qbar into the FPGA and display for accuracy. Since the A/D converters had the range from 0 to 3.30 V, if a negative voltage was input then the A/D converter would just sample 0 V.

Mitigation: The same algorithm for writing the A/D conversion for two A/D converters was used.

Team Response: This risk was acknowledged and fixed, allowing successful system demonstration by displaying the different I, Ibar, Q, Qbar voltages depending on where the corner reflector was.

2.9.3.1 VGA Code Development Risk

Description. The VGA code includes code that lights up pixels on the VGA display, parses the VGA into columns of 16, and does all the signal processing calculations to show where the target is according to how signals are reflected off the target.

Mitigation: Since time and complexity of this task were a major constraint to this project, the goal of the VGA code was then implemented to show increased brightness depending on the voltage received. This would save time from writing the signal processing functions, and still allow the team to demonstrate that if an object is in the scene, it is detected.

Team Response: The VGA code was written enough to show that when the IQ demodulator received signal from the scene, it would light up pixels on the VGA display. The signal processing functions were written in an excel spreadsheet, allowing for the determination of where the object is by plugging in the voltage values received from the IQ demodulator by using push buttons on the FPGA to display the values for the I, Ibar, Q, Qbar. This solidified the teams success in a transmit receive scenario with the system, while leaving most of the VGA code written. This only left the parsing of the display and functions in the spreadsheet to be implemented in VHDL to be done for the project.

2.9.4 Signal Processing Risks

2.9.4.1 Hardware Errors

Description:

There is a risk that hardware errors interfere with the image formation as every transmit/receive combination might not be the same as there is variability in the hardware.

Probability: Moderate
The probability that the data is not collected properly is moderate as the image formation calibration isn't accounting for all the different path lengths.

Consequences: Moderate
The consequences of this risk is moderate as it is an additional error that can be obtained empirically when the hardware is measured.

Strategy:
In order to obtain the hardware errors, the hardware will be measured using a voltmeter. An RF foam chamber will be set up in order to provide more accurate measurements. The measured data will then be entered into the Excel spreadsheet that is set up as a backup, which will then be used to as calibration for image formation.

Team Response: RF foam was not procured by the end of the project. Signal processing calculations were not integrated with the programming code by end of project for image formation.

2.9.4.2 Image Not Formed

Description:
The image may not be formed properly on the VGA display.

Probability: Moderate
The probability that the image is not properly formed and displayed is moderate as there may be errors in the calibration.

Consequences: High
The consequences of this risk are high as the signal processing goal is to try to obtain a one-dimensional image.

Strategy:
In order to obtain the one-dimensional energy, the Excel spreadsheet containing the signal processing and image calibration information would need to be verified in order to make sure that the data entered is all correct and makes sense. The next thing to do would be to verify that the signal is actually being transmitted and received in order to be processed. Then the image processing program would need to be looked over and debugged so as to verify that it is performing its function.

Team Response:
Signal processing calculations were not integrated with the programming code by end of project for image formation.

3 Design of Major Components

3.1 Transmit Signal Chain

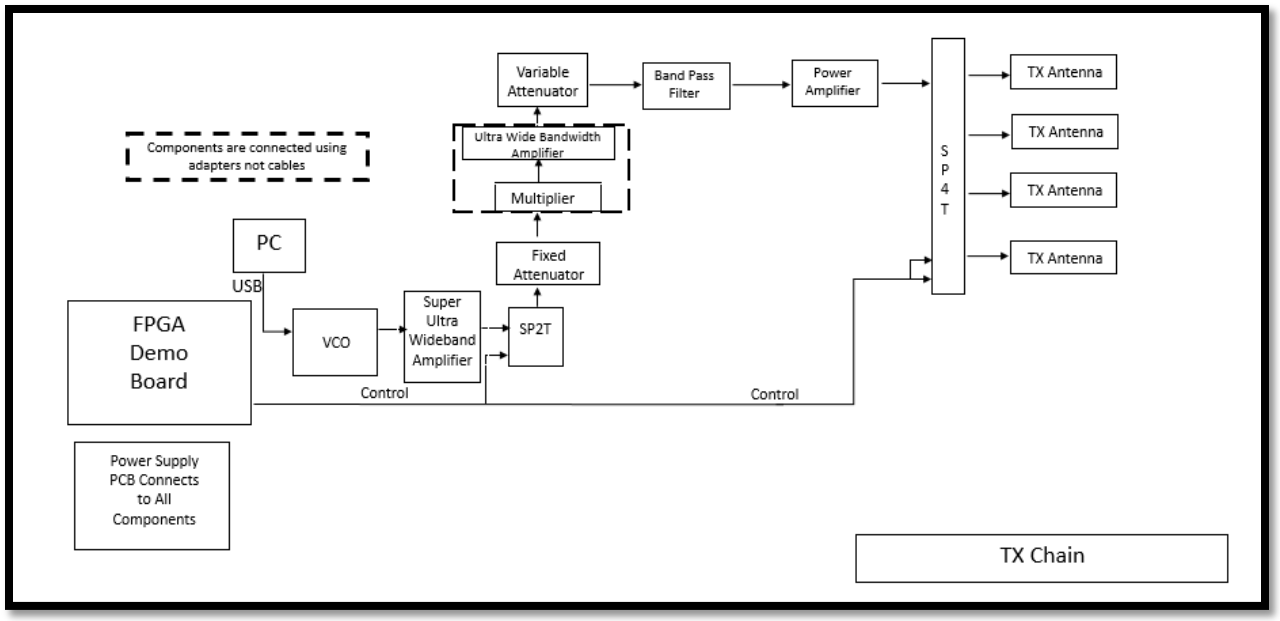


Figure 4: Transmit Signal Chain

The transmit signal chain is responsible for generating the RF signal that will be transmitted into the scene extent. The method by which the signal is generated is the VCO. The model chosen for this design generates a signal of -4 dBm at a frequency within the range of 4.38 GHz and 5.1 GHz. The next component in the transmit chain is the Super Ultra Wideband Amplifier. This amplifier was chosen because of its gain (26 dB) as well as its operating frequency range (700 MHz–18 GHz). The P1db compression point of this amplifier is 24 dBm however the output power of this design is 21.88 dBm. The cable that connects the VCO and the super ultra wideband amplifier is 3 inches long. It has a loss of 0.12 dB. This was based on the loss conversion factor of 0.47 dB/ft. This conversion factor applies to all cables in the electrical system that transmit the RF signal. Table 3 shows the places in the chain where there are cables. The next component is the SPDT; the purpose this component is to switch the system between transmit and receive mode. This model is capable of outputting a signal power of up to 27 dBm before the output begins to compress. This component was designed to output 19.76 dBm due to the loss of 2 dB inherent to this model. The next component in this design is a fixed value attenuator. This attenuator has a loss of 10 dB. The frequency multiplier is needed in this chain to increase the frequency of the system to 10 GHz. The loss associated with this component is 12.5 dB; the output of this component is designed to be -3.06 dBm. The next component is the ultra-wide bandwidth amplifier which has a gain of 12 dB. The designed output of this amplifier is 8.94 dBm, this takes into account the P1dB compression point of 10 dBm. The next component is the variable attenuator. The loss chosen for this component is 13 dB. This was attenuation level was chosen to limit the input power to the power amplifier that follows. The band pass filter is the next component after the variable attenuator. Its purpose is to center the frequency of the signal to 10.5 GHz. This component has a loss of 3 dB and a P1db compression point of 30 dBm. With the loss in mind the output of this component is -7.3 dBm. The power

amplifier follows the band pass filter. It has again of 30 dB and a P1db compression point of 37 dBm. The calculated output power of this component is 22.5 dBm. The SP4T switch follows, it has an input P1db compression point of 24 dBm. The calculated output of this component is 20.38 dBm, this takes into account the loss of 2 dB that is inherent to it. The cable that connects the SP4T to the transmit antennas is 36 inches long and has a loss of 1.41 dB.

Major risks for the transmit signal chain include:

- Component failure:
  - Consequences:
    - Signal may not be the correct frequency and/or strength
    - Component damage
  - Mitigation Strategy:
    - Ensure that all components will operate within their limits specified by the data sheets (input/output voltage, current, dBm)
- VCO Software Failure:
  - Consequences:
    - The VCO will not generate a signal with the correct frequency and/or strength
  - Mitigation Strategy:
    - Ensure that the appropriate registers have the correct programming data on the VCO

Table 6: Transmit Signal Chain Characteristics

Components	Input Power (dBm)	Input Power (mW)	Gain (dB)	Output Power (dBm)	Output Power (mW)
VCO	0.000	1	0.00	-4.000	0.398
Cable (5 inches)	-4.000	0.398	-0.20	-4.196	0.381
Super Ultra Wideband Amplifier	-4.196	0.381	26.00	21.804	151.501
Cable (7 inches)	21.804	151.501	-0.27	21.530	142.233
SPDT	21.530	142.233	-2.00	19.530	89.743
Cable (3 inches)	19.530	89.743	-0.12	19.413	87.347
Fixed Attenuator	19.413	87.347	-10.00	9.413	8.735
Frequency Multiplier	9.413	8.735	-12.50	-3.088	0.491
Ultra Wide Bandwidth Amplifier	-3.088	0.491	12.00	8.913	7.785
Cable (3 inches)	8.913	7.785	-0.12	8.795	7.577
Variable Attenuator	8.795	7.577	-12.00	-3.205	0.478
Cable (3 inches)	-3.205	0.478	-0.12	-3.323	0.465
Band Pass Filter	-3.323	0.465	-3.00	-6.323	0.233
Cable (5 inches)	-6.323	0.233	-0.20	-6.518	0.223
Power Amplifier	-6.518	0.223	32.00	25.482	353.319

Fixed Attenuator	25.482	353.319	-3.00	22.482	177.079
Cable (3 inches)	22.482	177.079	-0.12	22.36	172.352
SP4T	22.364	172.352	-2.00	20.364	108.747
Cable (36 inches)	20.364	108.747	-1.41	18.954	78.599

3.2 Receive Signal Chain

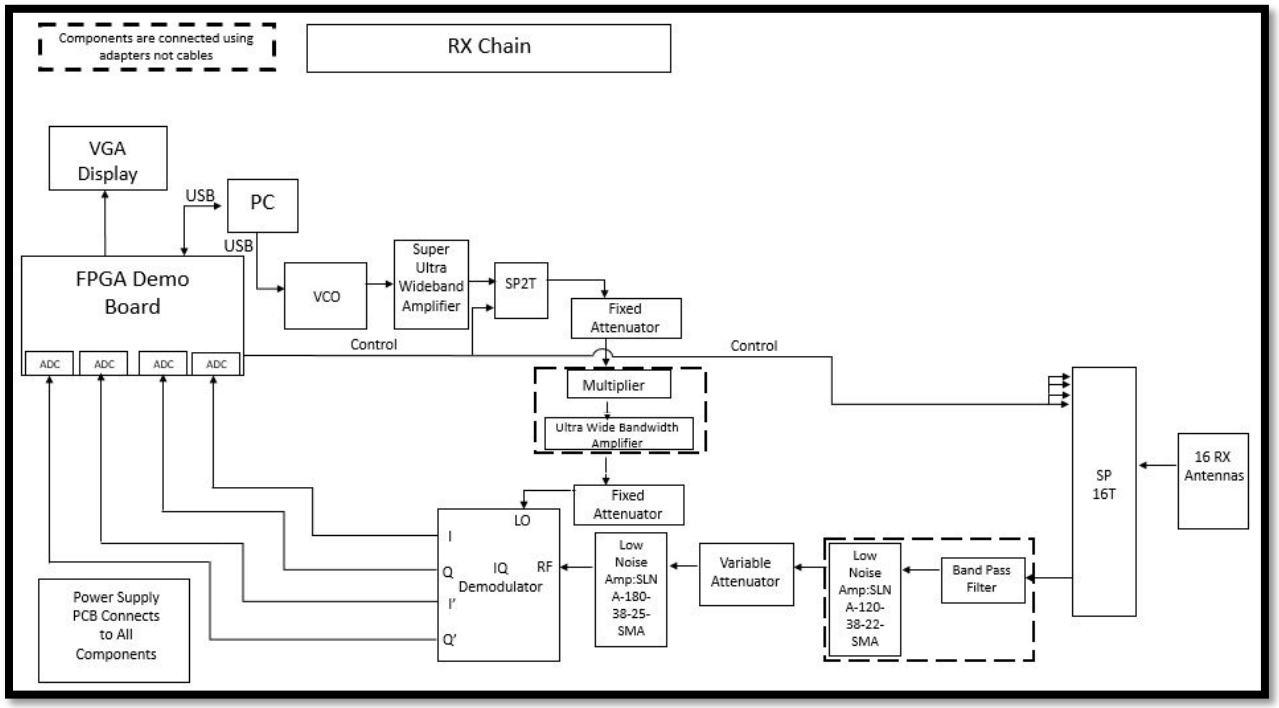


Figure 5: Receive Signal Chain

In short this chain was designed to receive the reflected signal scatterings from the target, interpret the phase and amplitude information of the signal and create imagery using signal processing. The received power seen at the cable that connects the receive antennas to the SP16T is -51.825 dBm. This was calculated using Equation 6 as shown in section 2.3.3. The SP16T switch has a calculated input of -53.235 dBm, a loss of 4.7 dB and an output of -57.935 dBm. A band pass filter follows the switch; it has a loss of 3 dB and its output is -61.085 dBm. The next component is a low noise amplifier. This component has a gain of 38 dB and outputs -23.205 dBm. Next is a variable attenuator placed to limit the input to the low noise amplifier that follows it. The attenuation loss used in the calculations is 4 dB. This creates an output of -27.205 dBm from the attenuator. The low noise amplifier that follows the variable attenuator has a gain of 38 dB and a P1db compression point of 22 dBm. The calculated input power is -27.325 dBm and the output is 10.675 dBm. The signal received then propagates to the RF channel of the IQ demodulator. The input P1db compression point is 12 dBm, the designed input to this channel is 10.555 dBm.

Major risks for the transmit signal chain include:

- Component failure:

- Consequences:
  - Signal may not be the correct frequency and/or strength
  - Component damage
- Mitigation Strategy:
  - Ensure that all components will operate within their limits specified by the data sheets (input/output voltage, current, dBm)

Table 7: Receive Signal Chain Characteristics

Component	Input Power (dBm)	Input Power (mW)	Gain (dB)	Output Power (dBm)	Output Power (mW)
RX Antenna Cable (36 inches)	-51.841	6.545E-06	-1.41	-53.251	4.731E-06
Single Pole Sixteen Throw (SP16T) Switch	-53.251	4.731E-06	-4.7	-57.951	1.603E-06
Cable (3 inches)	-57.951	1.603E-06	-0.12	-58.068	1.560E-06
Band Pass Filter	-58.068	1.560E-06	-3	-61.068	7.820E-07
LNA:SLNA-120-38-22-SMA	-61.068	7.820E-07	38	-23.068	4.934E-03
Cable (7 inches)	-23.068	4.934E-03	-0.27	-23.342	4.632E-03
Variable Attenuator (SA4077)	-23.342	4.632E-03	-14	-37.342	1.844E-04
Cable (3 inches)	-37.342	1.844E-04	-0.12	-37.460	1.795E-04
LNA:SLNA-180-38-25-SMA	-37.460	1.795E-04	38	0.540	1.132E+00
Cable (12 inches)	0.540	1.132E+00	-0.47	0.070	1.016E+00
RF (IQ Demodulator)	0.070	1.016E+00	-7	-6.930	2.028E-01

3.3 IQ Demodulator

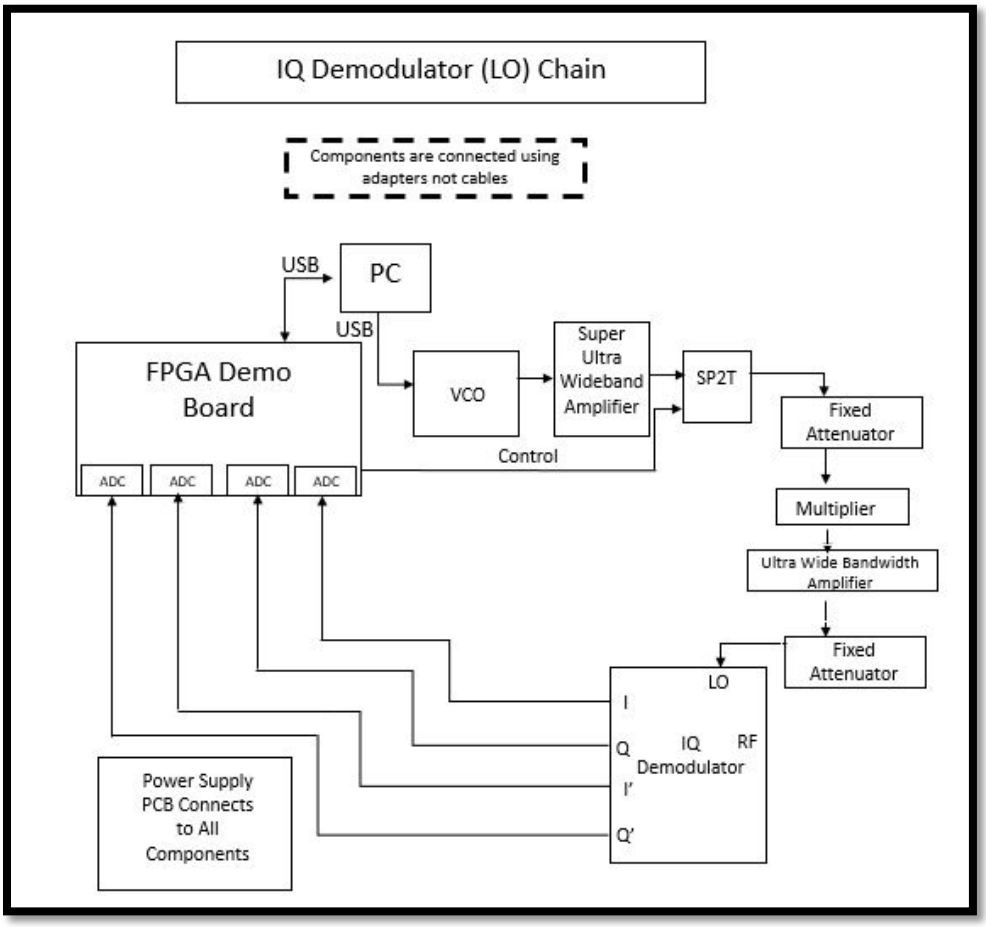


Figure 6: IQ Demodulator (LO) Chain

The IQ demodulator is important because it interprets the phase and amplitude of the received signals and outputs them as voltages. The IQ demodulator (LO) chain is the controller of the receive chain. The IQ demodulator only outputs the phase and amplitude voltages when the signal that enters the LO channel has the same frequency of the signal that enters the RF channel. The VCO, super ultra wideband amplifier, and the SPDT are considered to be in this chain because they drive the signal that enters the LO channel. The input and output power for all of the components are shown in Table 8. A key factor that went into designing this chain was that the typical strength of the signal inputted into the LO channel should be within the range of 3 to 7 dBm, preferably 5 dBm.

Major risks for the IQ Demodulator include:

- Component failure:
    - Consequences:
        - Phases and amplitudes of the RF signal do not get interpreted correctly
    - Mitigation Strategy:

- Ensure that the component will operate within its limits specified by the data sheet (input/output voltage, current, dBm)

Table 8: IQ Demodulator Signal Chain Characteristics

Components	Input Power (dBm)	Input Power (mW)	Gain (dB)	Output Power (dBm)	Output Power (mW)
VCO	0.000	1.000	0.000	-4.000	0.398
Cable (3 inches)	-4.000	0.398	-0.20	-4.196	0.381
Super Ultra Wideband Amplifier	-4.196	0.381	26.000	21.804	151.501
Cable (7 inches)	21.804	151.501	-0.27	21.530	142.233
SPDT	21.530	142.233	-2.000	19.530	89.743
Cable (3 inches)	19.530	89.743	-0.12	19.413	87.347
Fixed Attenuator	19.413	87.347	-10.000	9.413	8.735
Cable (5 inches)	9.413	8.735	-0.20	9.217	8.350
Frequency Multiplier	9.217	8.350	-12.500	-3.283	0.470
Ultra Wide Bandwidth Amplifier	-3.283	0.470	12.000	8.717	7.442
Cable (5 inches)	8.717	7.442	-0.20	8.599	7.243
Fixed Attenuator	8.599	7.243	-3.000	5.599	3.630
Cable (12 inches)	5.599	3.630	-0.47	5.129	3.258
LO IQ Demodulator	5.129	3.258	0.000	-	-

3.4 Power Supply Configuration

The power supply for the SAR system has been simplified from using multiple bulky lab power supplies to one input and 14 output voltages black box design. The black box supply requires a 19[V] input power adapter supply and regulates to output voltages of 15[V], 12[V], 5[V], -12[V], and -5[V]. Inside the black box consists of multiple drop-off voltage regulators bused off of the 19[V] power supply. Each voltage regulators then has a voltage and ground wire, twisted together to reduced electromagnetic distortion between wires, traveling through the top of the box to an either a block terminal strip. Some voltage regulators' output wires are spliced and connect to multiple block terminal inputs. The block terminals allow an input wire to connect to one side of an individual screw in terminal, and then have an additional wire connected to the other side of the terminal, which then this wire can be distributed to a component. Figure 7 is an aerial shot of the black box power supply design that illustrates how the input wires from inside the black box are connected to a terminal on each block terminal strip. The black wires are the ground wires, the red wires are the positive voltage supplies, and the white wires are the negative voltage supplies. Additionally, an on-and-off switch is located

on the side of the box, allowing easy access to supply or cutoff power to the entire SAR system. A LED light on the side of the black box confirms if power is being evenly distributed through the black box and out to each component.

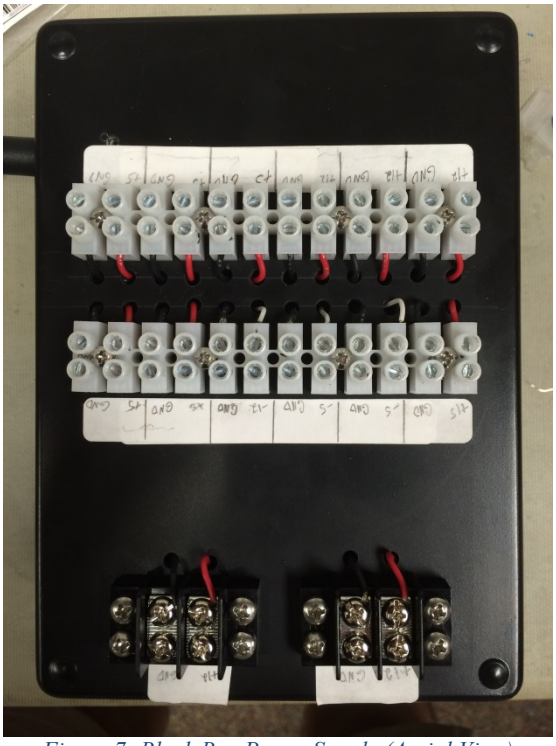


Figure 7: Black Box Power Supply (Aerial View)

The power supply board will contain the circuitry to provide power to all of the components that need power. The board itself will be powered by nine DC power supply inputs. Each of these supply inputs will provide power to the linear voltage regulators used in the design. See appendices for the data sheet as well as the schematics for all circuits and components.

Major risks for the power supply board include:

- Insufficient Power:
  - Consequences:
    - The needed output voltages and currents will not be supplied or may not be large enough to meet the needs of the components
  - Mitigation Strategy:
    - Ensure that the components will operate within its limits specified by the data sheet (input/output voltage, current)

3.4.1 Black Box Power Supply Configuration

Inside the black box consists of six positive voltage module boards and two negative voltage regulators. Three postive voltage regulators have a pi filter introduced into their circuit to prevent any cross feedback between the high gain components including both low noise

amplifiers and the power amplifier. Cross feedback can cause noise within our system and possibly distort the radio frequency signal within the system, tainting the final results. Figure 8 is a block diagram of the voltage supply design within the black box.

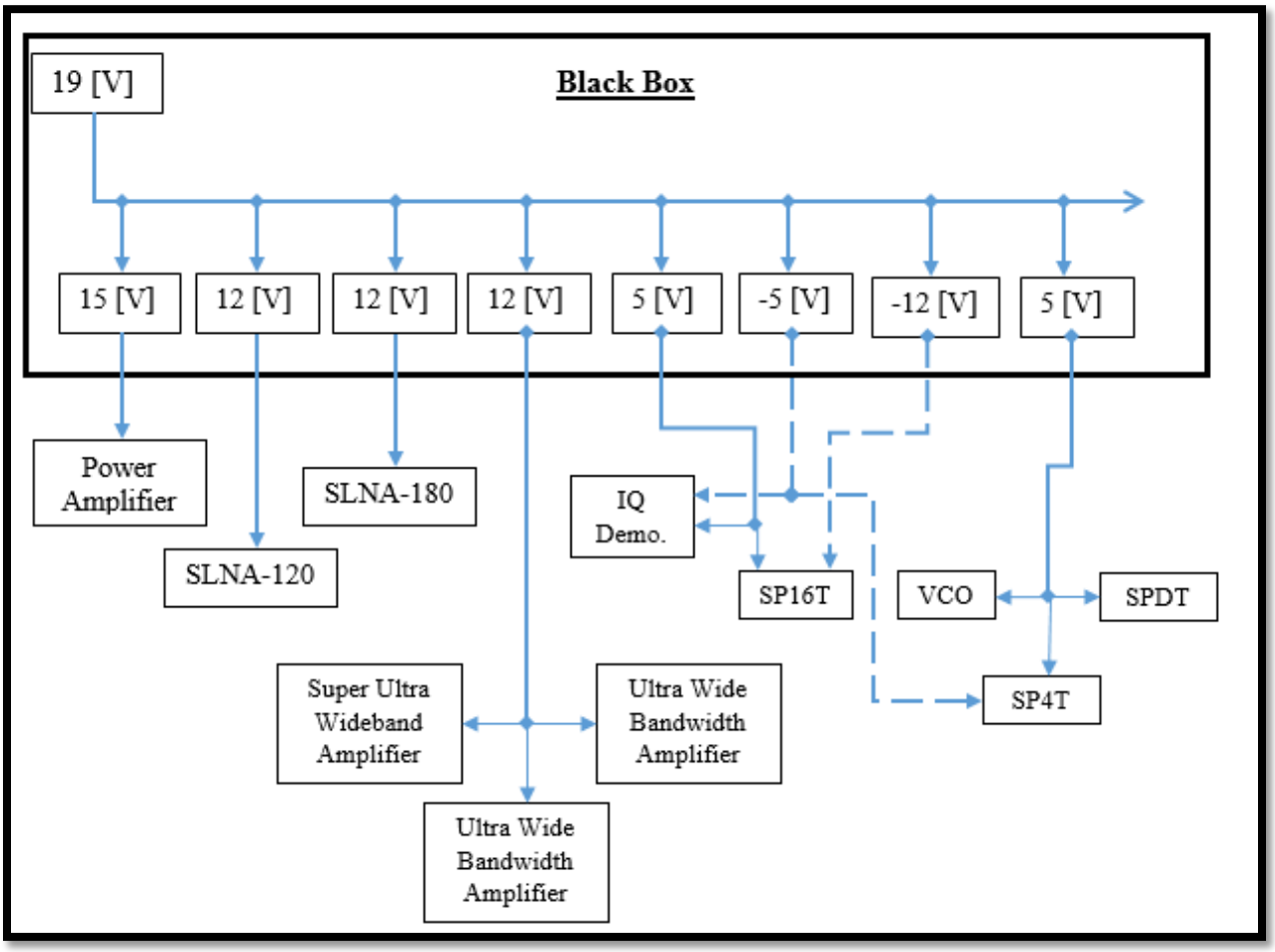


Figure 8: Black Box Power Supply Block, Flow Diagram

3.4.2 Positive Voltage Module

The positive voltage regulators are six separate power module boards consisting of Linear Tecnology's LTC4008 multi-chemistry battery charger. The LTC4008 is pulse-width modulator controller "[using] a synchronous, quasi-constant frequency, constant off-time architecture that will not generate audible noise even when using ceramic capacitors" [2]. Figure 9 is the circuit diagram to correctly employ the LTC4008. The LTC4008 charger intakes 19 [V] and based on the load resistor values connected to the *BATMON* port on the module, different voltage levels can be executed. Table 9 provides the necessary resistor pairings for the required voltages. Figure 10 is a black-and-white diagram of the power module. *VBAT* on Figure 10 is connected to a screw-in terminal outside the black box with a 22 guage wire. Like wise, a 22 guage wire is used to connected the ground (GND) port off of the power module to another screw-in terminal outside the black box.

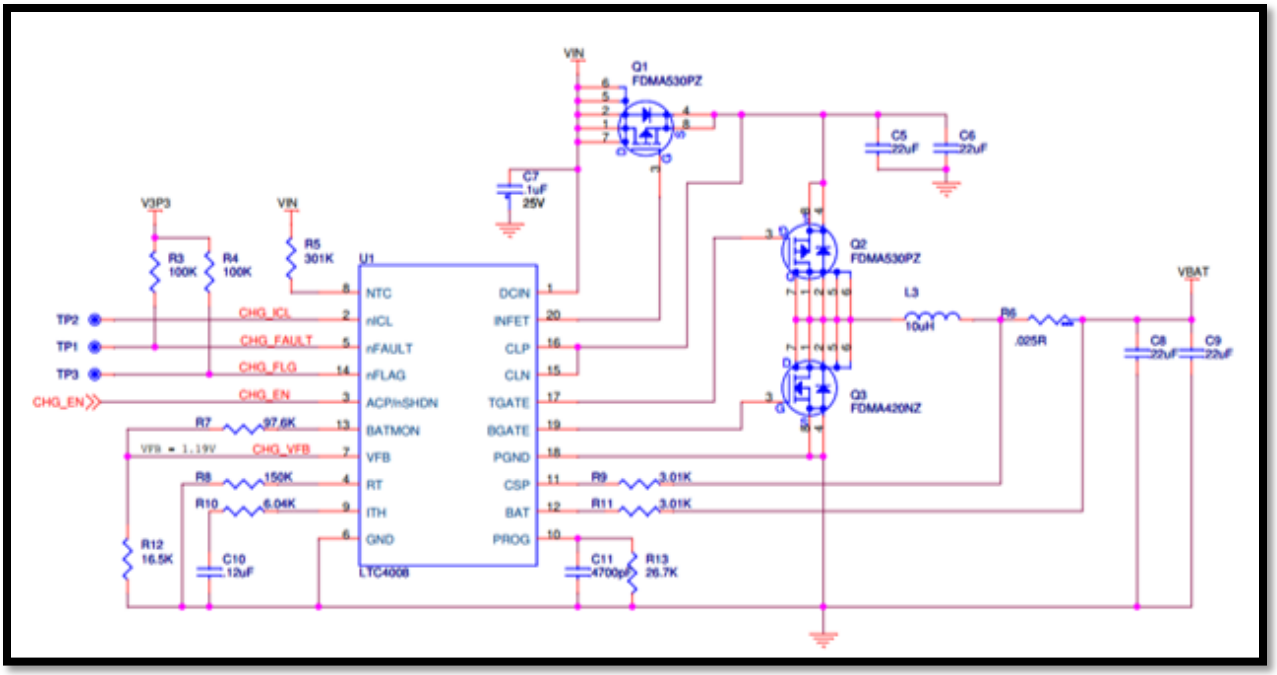


Figure 9: Circuit Diagram Layout (LTC4008)

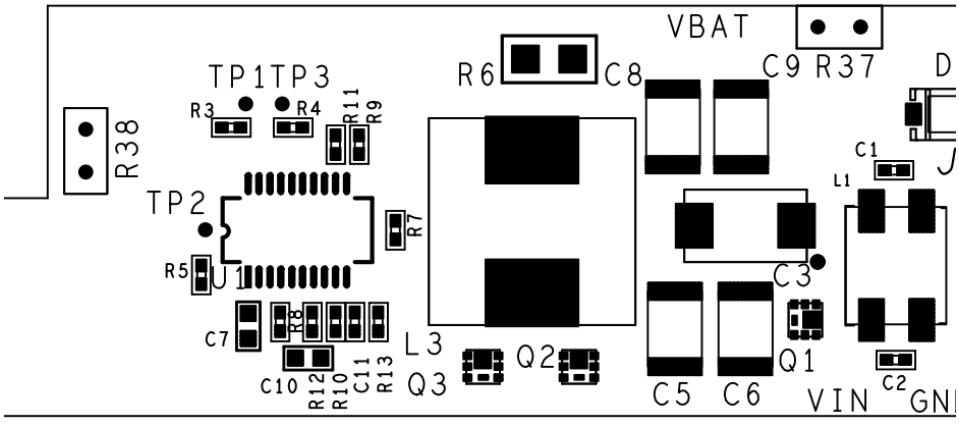


Figure 10: Positive Voltage Regulator Board Layout

Table 9: LTC4008 Resistor Values

Voltage [V]	Resistor	Resistance Value [Ω]
+5	R7	154k
	R12	47.5k
+12	R7	100k
	R12	11.0k
+15	R7	130k
	R12	11.0k

3.4.3 Negative Voltage Module

The negative voltage regulators were bought from Digikey and are Texas Instruments PTN78020AAH. However, in order to output the necessary negative voltages, additional assembly is still required. To finish creating the negative voltages, tantulum and ceramic capacitors need to be wired into the circuit and the correct resistor value needs to be inserted. The resistor sets the voltage level, Table 10 and Table 11 specifies which resistors and capacitors are required, respectively. Note, the same capacitor values are used for both negatuve regulators. Figure 11 is the circuit diagram required to create the negative voltages. Figures 12 and 13 are the finished negative voltage regulators.

Table 10: Rset Values for Negative Voltage Module

Voltage [V]	Resistor Value (R_{SET}) [Ω]
-5	2k
-12	28.8k

Table 11: Capacitor Values for Negative Voltage Modules

Capacitor	Type	Capactiance [F]	Voltage Rated
C1	Tantalum	68µ	25 [V]
C2*	Ceramic	22µ x 4	25 [V]
C3	Tantalum	68µ	25 [V]

*C2 – 4 Ceramic capaticors need be place in parallel

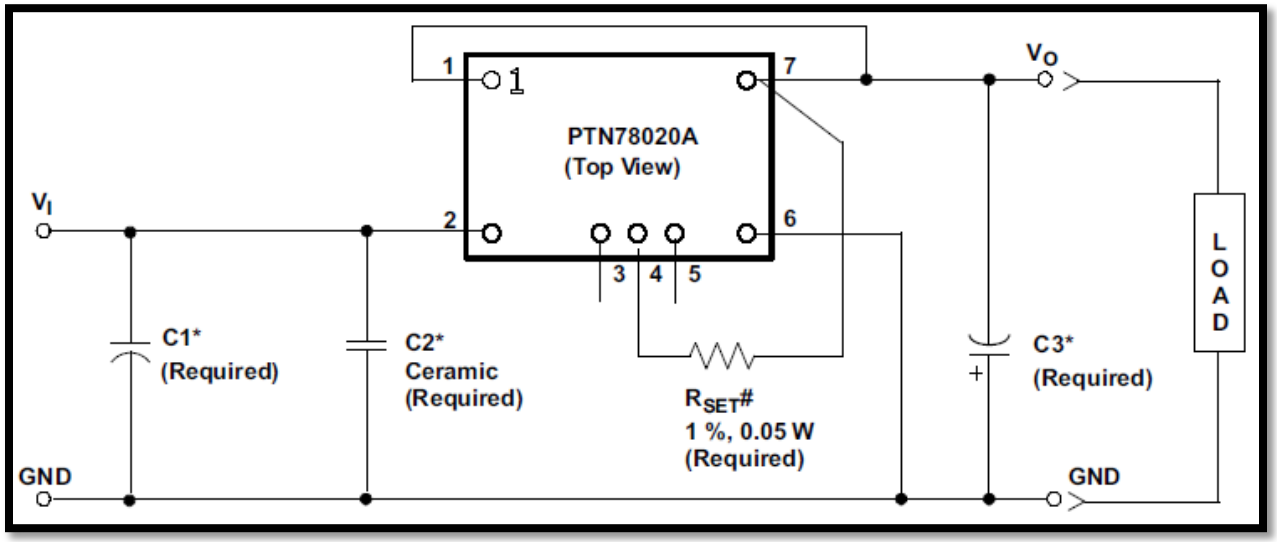


Figure 11: Negative Voltage Circuit Layout

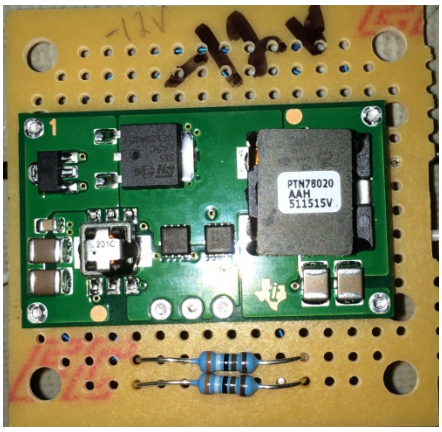


Figure 12: Negative Voltage Regulator Front side

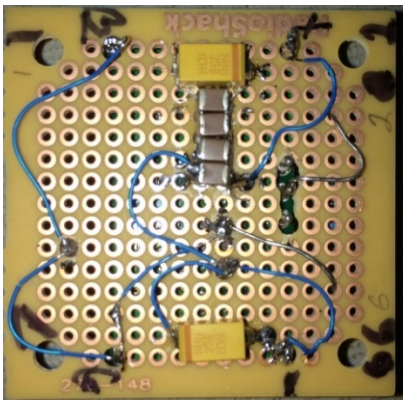


Figure 13: Negative Voltage Regulator Backside

3.4.4 Pi Filter

For the both low noise amplifiers and the power amplifiers, pi filters were installed in the circuit to prevent excessive noise from leaking into other components. A pi filter will only allow an input voltage signal equivalent to the output voltage signal pi filter to travel through to the load. All additional noise will be filtered. The construction of the pi filter is a capacitor (C1) in parallel with an inductor (L) and another capacitor (C2) in series with each other. A resistance load (RL) is then in parallel with the capacitor in series with the inductor. Figure 14 is a clear diagram of a pi filter. The performance of the filter is determined by its regulation and ripple.

Both C1 and C2 capacitors employed in the pi filters are 22[μF] ceramic from TDK Corporation, part number: C4532X5R1E226M250KA – Figure 15 is an illustration of the capacitor utilized. The inductor is a choke common mode, rated at 700[Ω] and 8[A] – Figure 15 is a visual of the choke.

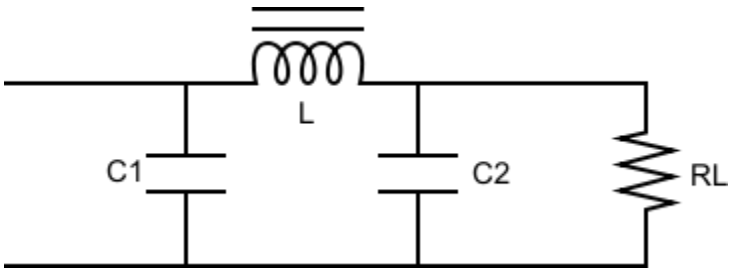


Figure 14: Pi Filter Diagram

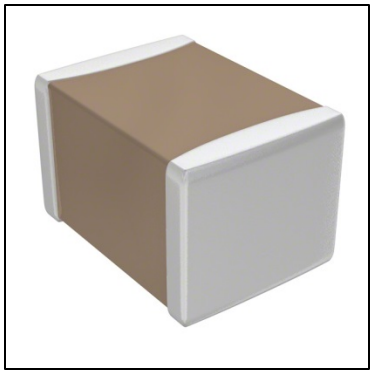


Figure 15: Ceramic Capacitor

Figure 16: Choke Common Mode

3.5 Software Design

The goal for this project (as stated in the introduction) is a radar system that uses synthetic aperture radar theory by having multiple stationary antennas to create multiple phase centers. The goal of the software design for this project was to have the system be electronically controlled by an FPGA that would transmit and receive the signals from the antennas, convert the analog input signals in the receive antennas into binary voltage values that could be stored on the FPGA, and have the FPGA calculate the phase and the amplitude of the respected signals. The results of the phase and amplitude of the calculations on the FPGA were to be displayed on the VGA display, having the display parsed into columns of 16. In non-real time, this would show via brightness how much signal the receive antenna is actually receiving. The system used a 20 nanosecond pulse to transmit to the reflecting target, and this pulse was used since the target was 20 feet away and this time would prevent crosstalk from happening. With this being said, the main tasks to the software design with detailed checklist and explanation are listed and explained in this section.

The software design aspect of this project was split into three major tasks. This was done because the software aspect of this project was most likely the most complex part of the project and completing the software in steps would ensure success. This was done to give feasible design constraints and have reasonable goals that could be achieved by the final demo of the system. Each of the three tasks will be explained thoroughly, and the status of how complete each of the tasks were will also be explained. If a part of the software design was incomplete,

there would be detailed explanation to why it was incomplete, what effects did this have on the entire demonstration and the project, and what steps would be taken to complete the software design in a timely and reasonable manner. In addition to a checklist of the completed aspects of the software design, any design changes that were made for the demonstration and a full explanation of the code used in this project is also included in this section to provide clarity for the reader. Note: To see code for the SAR Imager project, go to Appendix C.

Notable changes to the system:

Several notable changes were made in the software design for the actual demonstration of the system. The first one that was made was the values for the pulses that control the timing for the system. This was due to the Analog to Digital converter only having a sampling rate of one million samples per second. To mitigate for this issue, the timing for the system was changed so that it would take the average value of the transmitted pulses to give an average DC value for the signal reflected off the target. The timing for this would have to at least be 2 at least microseconds. This is because the range is one over two times the sampling rate for the A/D converter (aka: one million bits per second yields to a microsecond). The second notable change was the fact that there was no level shift circuit used. To mitigate for this, four analog to digital converters were used instead of two, where all the signals from the IQ demodulator (I, Ibar, Q, Qbar) were all sampled on the four analog to digital converters and stored on the FPGA.

3.5.1 System Timing

3.5.1.1 Description

The System timing includes the control of the switches for the system. This was done by using pulses from the FPGA to control the logic of the switches that control what the system is doing at a certain time. The three switches for the system are the SPDT(single pole double throw) switch, SP4T(single pole four throw) and the SP16T(single pole sixteen throw) switch. The SPDT switch controls whether the system is in transmit or receive mode. The SP4T switch controls which transmit antenna is transmitting signal. The SP16T switch controls which receive antenna is receiving signal.

3.5.1.2 Explanation

For the SPDT switch, a logic 1 was considered to be on and logic 0 was considered to be off according to the data sheet for the switch. This yielded transmit mode to be considered logic 1 and receive mode to be considered logic 0. Since it was just a 1 bit signal controlling the switch, the output type std_logic was used. The pulse actually getting transmitted to the system had the same timing as the SPDT switch, which was 20 nanoseconds. For the SP4T switch, a logic 0 was considered to be on and logic 1 was considered to be off according to the data sheet for the switch. Since four bits were used to control the SP4T switch, the output type std_logic_vector(3 DOWNTO 0) was used. For the SP16T switch, a logic 0 was considered to be on and logic 1 was considered to be off according to the data sheet for the switch. Since sixteen bits were used to control the SP4T switch, the output type std_logic_vector(15 DOWNTO 0) was used. Slider switches on the FPGA were used to control all the combinations of transmit antennas and receive

antennas, with one slider switch combination working for one transmit receive combination respectively for all transmit receive combinations. Table 12 below shows the different combinations for transmit receive by changing the slider switches on the FPGA.

Table 12 Logic Table for Switch Combination

Transmit Antenna	sw5	sw4	sw3	sw2	sw1	sw0	Receive Antenna
	0	0	0	0	0	1	r0
	0	0	0	0	1	0	r1
	0	0	0	0	1	1	r2
	0	0	0	1	0	0	r3
	0	0	0	1	0	1	r4
	0	0	0	1	1	0	r5
	0	0	0	1	1	1	r6
t0	0	0	1	0	0	0	r7
	0	0	1	0	0	1	r7
	0	0	1	0	1	0	r6
	0	0	1	0	1	1	r5
	0	0	1	1	0	0	r4
	0	0	1	1	0	1	r3
	0	0	1	1	1	0	r2
	0	0	1	1	1	1	r1
t1	0	1	0	0	0	0	r0
	0	1	0	0	0	1	r8
	0	1	0	0	1	0	r9
	0	1	0	0	1	1	r10
	0	1	0	1	0	0	r11
	0	1	0	1	0	1	r12r
	0	1	0	1	1	0	r13
	0	1	0	1	1	1	r14
t2	0	1	1	0	0	0	r15
	0	1	1	0	0	1	r15
	0	1	1	0	1	0	r14
	0	1	1	0	1	1	r13
	0	1	1	1	0	0	r12
	0	1	1	1	0	1	r11
	0	1	1	1	1	0	r10
t3	0	1	1	1	1	1	r9

	1	0	0	0	0	0	r8

3.5.1.3 Status

This code was completed and tested via an oscilloscope and finalized by testing the system in CAPS. When tested on an oscilloscope, the code was outputting the correct logic for each combination of slider switches. On the actual system, the test for controlling the system timing via the FPGA were successful. For the actual testing, the FPGA could control the SPDT switch, SP4T switch, SP16T switch, and output a pulse via using different combinations of slider switches. The VHDCI connector was used to output the 20 ns pulse to control the SPDT switch, since the pmod outputs did not allow a sharp enough rise time for that fast of a pulse. For the actual demo, the signal generator was used to control the SPDT switch since the VHDCI connector was burnt. For next year, a new connector would need to be bought to connect to the FPGA. From the results that the FPGA could control the system timing shows that this task of the code was complete.

3.5.1.4 Future steps to be taken

None. This portion of the software design was complete and does not need further work. However, if the system was to be upgraded into real time, a simple counter would just have to be added to change the emitting of pulses to the switches controlling the SPDT, SP4T, and SP16T switches.

3.5.1.5 Results relative to project success

The FPGA was able to control the system timing for the system demonstration.

3.5.2 Analog to Digital Conversion Code

3.5.2.1 Description

The Analog to Digital Conversion Code takes an analog voltage from a range of 0 to 3.3 volts and outputs a digital 12 bit binary combination of the input analog voltage. This is the portion of the code that allows the FPGA to read the signals that are reflected off of the corner reflector and store them onto the FPGA. This essentially allows the completion of the transmit receive aspect for the system. The signals that the A/D code reads are all from the IQ demodulator and respectively are I, Ibar, Q, Qbar. For this code, two Pmod A/D converters were used, and each Pmod A/D converter had two A/D converters. This allowed all four signals from the IQ demodulator to be read on the FPGA, with one Pmod A/D converter converting I,Ibar and the other Pmod A/D converter converting Q, Qbar. Note that negatives voltages go to zero since the range for the Pmod A/D converters are 0 to 3.3 volts. The actual values for the converted 12 bit binary combination were displayed on the 7 segment display as hex values to check for accuracy.

They were scaled to be so that an input of 0 volts would be read as 000 in hex, and and 3.30 volts would be read as FFF in hex. The conversion formula for the scaling can be seen below:

$$\frac{V}{3.30} * 4095 = X$$

Where V=Input voltageinto A/D converter

X= decimal Value of the hex number displayed on 7 segment display

Solving for V to check the value of input voltage from the voltage displayed on the 7 segment display is shown below:

$$V = \frac{3.30 * X}{4095}$$

3.5.2.2 Explanation

For this code, two different states were used to give the FPGA the ability to distinguish when to be reading input data. These two states were idle and read. When the state was idle, the signal CS (which matches the schematic in the data sheet) was given a value of 0, which basically shows that the A/D converter was not reading data (the input analog voltage). When the state was read, CS was given a value of 1, which shows that the A/D converter was reading in data, and a counter was used to check how many bits were left out of 12 bits and what bit the counter was on. This allowed for the correct parsing of data when an analog voltage was input. Note that both A/D converters were used on each Pmod A/D converter, so in total four A/D converters were used to read I, Ibar, Q, and Qbar. Pushbuttons were used to display each of the four voltages from the IQ demodulator.

3.5.2.3 Status

This code was completed and tested via input voltages from a DC power supply and finalized by testing the system in CAPS. The tests for reading input voltages from a DC power supply were successful, and extremely accurate. This was shown when the 7 segment display displayed 7FF for a 1.65 voltage input, FFF for a 3.30 voltage input, and 000 for a 0 voltage input. When testing the system in CAPS, the FPGA was able to read the I, Ibar, Q, Qbar voltages from the IQ demodulator and displayed on the 7 segment display using the pushbuttons on the FPGA. This showed that this coding task was completed, and needs no more further work.

3.5.2.4 Future steps to be taken

Future steps to be taken: None. This portion of the software design was complete and does not need further work. Even if the system was to be upgraded into real time, the code for the Analog to Digital conversion is reliant on the clock of the FPGA and counters that are already much faster than the system timing needed for real time. This shows that even if the system was upgraded to real time, the Analog to Digital Conversion code would not have to be changed.

3.5.2.5 Results relative to project success

Results relative to project success: FPGA was able to convert analog voltage signals that reflected off the corner reflector to digital 12 bit binary combinations in the system demonstration. The digital voltage values were read off the 7 segment display, thus providing proof that the transmit receive aspect of the project was complete.

3.5.3 VGA Code

3.5.3.1 Description

The VGA code would do the proper illumination of the pixels for the VGA display, along with the correct parsing of the columns to illuminate the pixels into columns of 16. This code also includes all of the calculations for the signal processing and calculations with the different received voltages that are stored onto the FPGA. The VGA will overall perform the Fast Fourier transform of the incoming energy, allowing the metal object to be detected by the pixels illuminated on the VGA display. To summarize, the VGA code signal processing will perform the basis functions for 16 angles by taking the sine of the 16 angles in equal increments. The VGA code will then break down the basis functions into real and imaginary parts, and get the stored data from the IQ demodulator and have the IQ data times the real and imaginary components of the basis functions. This will give the amplitude corresponding to each of the corresponding 16 angles. If this result were to be graphed, this would give a sinc function, and the peak of this sinc function is what would determine where the energy is coming from thus lighting up the VGA display corresponding to that region. Since RF absorbing foam was not procured for this project, ideal detection of an object in this project was not doable. In an ideal setting with no cross talk, an object would able to be detected. In essence, the signal processing calculations that are on the excel spreadsheet need to be implemented in VHDL, and the sinc function that is the result of the complex multiplication is the result of the Fast Fourier transform of the input signals.

3.5.3.2 Explanation

There are several steps for completion of this code. For the illumination of pixels on the VGA display, the VGA display had the horizontal and vertical counter given values that would allow for pixels to be illuminated on a 640x480 display. The FPGA has designated ports for the output of color from the VGA port, so these designated ports were used and output as logic ‘1’ when the clock was high and this was dependent on a counter that the value was changed when the input voltage from the A/D converters was changed. For the lookup table, the values for sine and cosine for the angles was chosen based on iterated values from the voltage ranged of 0 to 3.3 volts and the angles used in the scene for signal processing. This was done from a sample look up table found online, and this same lookup table is given on the team website as code for the project. The basis functions results and the complex multiplication of IQ and the results from the

basis functions could be done the following three ways. The first way and most likely way to do this would be to do a conversion to the 12 bit numbers to make it a signed number by either having the first bit being 1 or 0. Doing multiplication in binary of the signed numbers would allow the signal processing functions to be written by only losing a bit of accuracy. This is fine as losing one bit of accuracy for the data taken for this system is definitely still accurate enough due to the small amount of data points taken for this project. If thousands of data points were taken, then more bits of accuracy would have to be added and possibly having the data stored from the A/D converter changed to a higher bit range. This is unnecessary for this project, so just losing one bit of accuracy for signed binary multiplication will be fine. Another way to do this would be to use fix floating point in VHDL by including the ufixed library and then doing the multiplication and then scaling and/or converting back to the 12 bit binary combination used earlier. The third way would be to use floating point in VHDL by including a package that can be downloaded online. By far, the most likely way to do this and thus complete the project is the first option. Complex multiplication will thus be easy by just taking the binary results from each of the calculations previously done.

3.5.3.3 Status

The completion for this code was broken down into 6 parts. They are the following:

1. Pixel illumination of the VGA display
2. Having the VGA display detect an object if it is in the scene by lighting up if a signal is reflected.
3. Proper look up table for sine and cosine functions
4. Parsing the illumination of pixels on the VGA display
5. Write and break down basis functions from spreadsheet into real and imaginary components
6. Complex multiplication of IQ data and the results from the basis functions.

Pixel illumination of the VGA display, having the VGA display detect an object if the signal is reflected from the corner reflector, and the proper look up table for sine and cosine values was completed. The only parts that need to be completed for next year to complete the project are to parse the illumination of pixels on the VGA display, write and break down basis functions into real and imaginary components, and complex multiplication of the IQ data and the results of the basis functions.

3.5.3.4 Future steps to be taken

The only things that need to be done in order to ensure completion of this portion of code for the project are to implement the functions on the signal processing excel spreadsheet, and to parse the illumination of pixels on the VGA display. After this, the entire part of coding for the Imager is complete and would need no further work.

3.5.3.5 Results relative to project success

Results relative to project success: FPGA was able to output pixels to VGA display, noted in Figure 17, whenever something was reflecting off the corner reflector. The brightness of the pixels were relative to how high the input voltage from the IQ demodulator was, being very bright when the input voltage was close to 3.3 V and very dim when close to 0 volts. Although this could not pin point where the target was on the scene, the FPGA could successfully output pixels on the VGA display corresponding in brightness to how much input voltage was received from the reflected from the target.

For Figure 17 below, the input voltage was 0 V, thus showing the VGA display blank.

Figure 17 VGA Display 1

For the image below, the input voltage was 1.65 V, thus showing the VGA display halfway in brightness lit up.

Figure 18 VGA Display 2

For the image below, the input voltage was 3.30 V, thus showing the VGA display lit up completely in brightness.

Figure 19 VGA Display 3

3.6 Signal Processing Design

If the target was really close to the array of antennas, there would be a huge difference in the path length between the center of the array and the phase center that's off to the side. However, when going 20 feet away from the array, then the difference is manageable, so a target would be set up at boresite 20 feet away at the center of the array, which would be called a calibration target. And then each phase center and the I and Q voltages would be measured, which would then become the calibration factor. This calibration factor represents the error out in free space from the horn to the target. So the calibration at boresite was done in order to determine what the calibration factor would be when the target is at the center of the array of horns. The calculation of error at the maximum angle was done in order to determine how the calibration holds up when the scatter energy is brought in at different angles.

The range from the antennas to the target is 20 feet; however, for the calibration, the measurements will be done in inches, hence the range is 240 inches. The antenna separation, in lambda, is 6λ. One lambda at a frequency of 10 GHz is equal to 1.18 inches.

3.6.1 Boresite Calibration

As explained in the signal processing section, there are two transmit horns and eight receive horns, and sixteen phase centers from each transmit and receive antenna pair to the scene are created. In the following Figure 20, A is the first transmit horn and A_1 through A_8 are the receive horns, which in this case each one of them is pairing with transmit horn A. B at the bottom is the second transmit horn, and B_1 through B_8 going from bottom to top are pairing with transmit horn B.

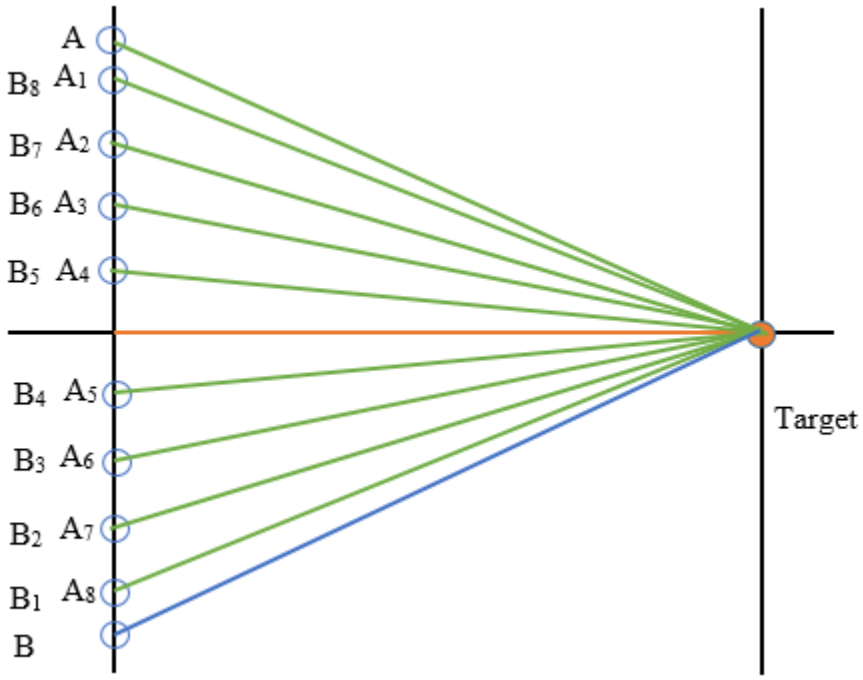


Figure 20. Transmit and Receive Horns with Target at Boresite

In Table 13, the distance relative to the center of the array is calculated in lambda. The distance for A_4, as well as for A_5, is calculated by dividing the antenna separation of 6λ by 2, as the center is halfway between antennas A_4 and A_5, which results in 3λ. Then the distance for A_3, as well as for A_6, is calculated by adding the result of A_4 to the antenna separation of 6λ, and the result is 9λ. These calculations continue in this trend for horns A_1, A_2, A_7, and A_8. For the transmit horn A, the distance relative to the center of the array is found by adding the result of A_1, which is 21λ to half of the antenna separation for a result of 24λ. The same process is applied to the transmit horn B along with the receive horns B_1 through B_8.

In order to calculate the distance relative to the center of the array in inches, the distances in lambda were simply multiplied by 1.18 inches, which is what one lambda is equal to. To find the distance to range when the target is not moved off at any angle, in which case θ = 0°, the Pythagorean Theorem is used as shown in Figure 1. If a is equal to the distance relative to the center of the array and r is the distance from the center to the target, then the relation for each horn would be $distance = \sqrt{a^2 + r^2}$. Then for horns A_1 through A_8, the sum of the transmit/receive path of each antenna was calculated by adding the calculated distance of horn A

to each of these receive horns. The same was done for transmit horn B and receive horns B_1 through B_8. This is essentially the boresite calibration.

Table 13. Boresite Calibration

BORESITE CALIBRATION				
	f = Distance Relative to Center of Array (λ)	**a = Distance Relative to Center of Array (inches)**	**Distance to Range from Each Antenna (θ=0°) (inches)**	**Sum of Tx and Rx Path of Each Antenna (inches)**
A	24	28.34645669	241.67	
A1	21	24.80314961	241.28	482.95
A2	15	17.71653543	240.65	482.32
A3	9	10.62992126	240.24	481.90
A4	3	3.543307087	240.03	481.69
A5	3	3.543307087	240.03	481.69
A6	9	10.62992126	240.24	481.90
A7	15	17.71653543	240.65	482.32
A8	21	24.80314961	241.28	482.95
B8	21	24.80314961	241.28	482.95
B7	15	17.71653543	240.65	482.32
B6	9	10.62992126	240.24	481.90
B5	3	3.543307087	240.03	481.69
B4	3	3.543307087	240.03	481.69
B3	9	10.62992126	240.24	481.90
B2	15	17.71653543	240.65	482.32
B1	21	24.80314961	241.28	482.95
B	24	28.34645669	241.67	

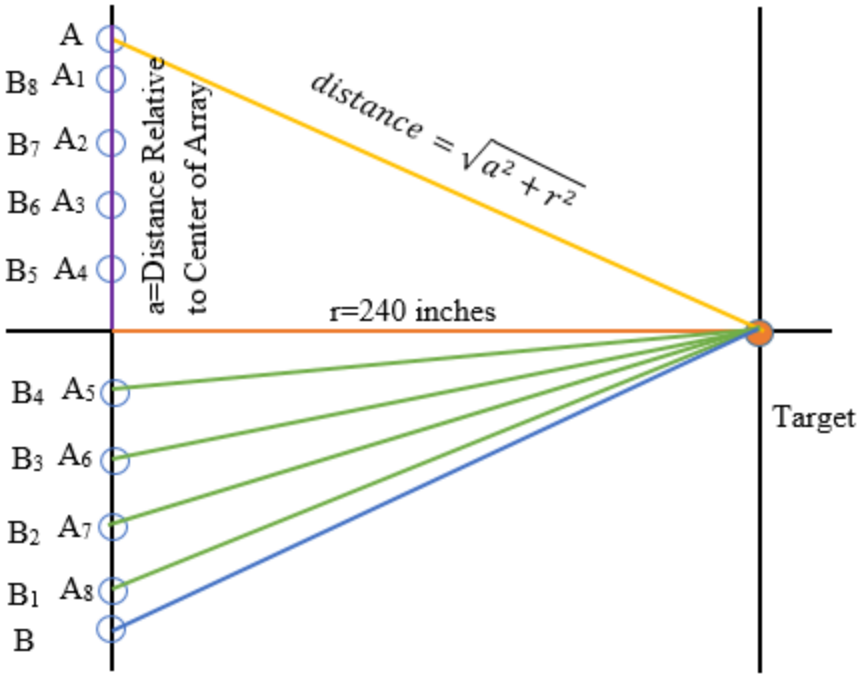


Figure 21. Calculation of Path from Antenna to Target

In Figure 22, the sums of the transmit and receive paths to each antenna were plotted out as sixteen points. As observed in the previous table, the results of each of the antennas A_1 through A_8 are the same as of each of the corresponding antennas B_1 through B_8, which is reflected in the plot below.

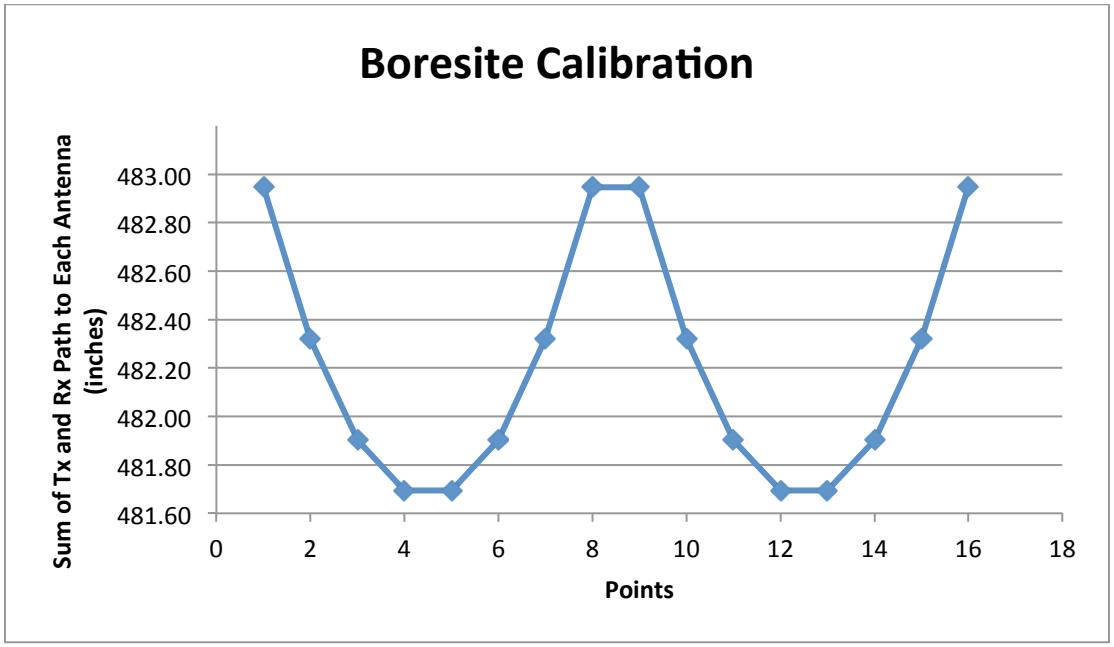


Figure 22. Sum of Tx and Rx Path to Each Antenna for Boresite Calibration

3.6.2 Calculation of Error at Maximum Angle

After calculating the boresite calibration, it is necessary to calculate the error with the target at maximum angle, which is five degrees in this case. When the target is rotated five degrees, the vertical line that the horns are on are also rotated the same angle as shown in Figure 23. The same relationship with the rotated line is present as there was previously with the boresite calibration. The distance between each phase center is the hypotenuse of a right triangle.

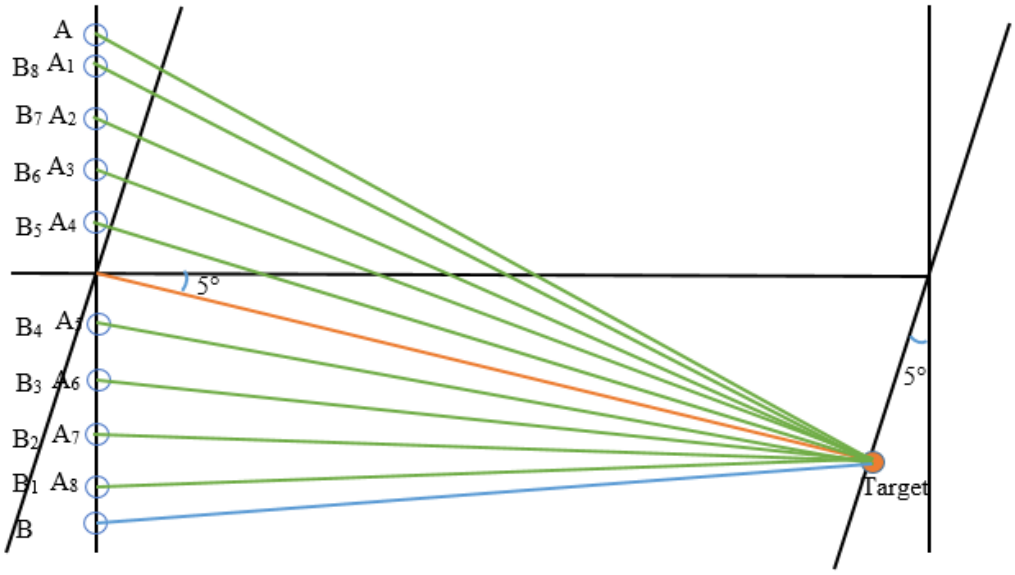


Figure 23. Transmit and Receive Horns with Target Off-Center 5°

The phase centers are being formed from the middle of the transmit horn to the middle of a receive horn, and a line is drawn about halfway in between. This is the reference point for the processing. When it goes to the far field having a transmit and receive field, it is equivalent to having one antenna that does transmit and receive at a point halfway in between. So these sixteen points in phase are taken and then when going off at an angle, there would be a target that's not at boresite and even at far field. If it is shifted and rotated at an angle θ, then the distance to each of the phase centers increases by d*sin(θ).

With the target at boresite, there's no phase difference as d*sin(θ) would be zero since θ is zero so there wouldn't be any difference in the distance. But as the target is rotated, a progressively increasing distance is picked up as it goes from each phase center. That's what the processing is looking for, the phase line coming in with different slope. That is what the scatter energy is being decomposed into, how it comes in at different angles and causes different phase slopes from phase center to phase center.

In the following Table 18, the far field phase centers are calculated by taking the average of the transmit antenna and the receive antenna being calculated. For example for A_1, the far field phase center is calculated in the following manner: $\frac{f_A+f_{A1}}{2} = \frac{24\lambda+21\lambda}{2} = 22.5$. To calculate the far field phase centers in inches as shown in the third column, the values of each far field phase centers is multiplied by 1.18 inches, which is equal to one lambda.

In the fourth column, which is labeled as 2*d*sin(θ) (inches), d*sin(θ) was multiplied by two since it's two-way as with the transmit and receive, it goes out and back, which means it picks up twice the distance. Now the transmit and receive are the same lengths at far field. When that fourth column is plotted, it is a slope line as shown in Figure 24. If θ is equal to zero, it would go to zero, and the path length to all the phase centers would be the same. If θ is increased to 1, it would get bigger. That's the ideal response, so if there is a target at far field, that's how it would respond as.

Table 14 Phase Center Theta Calculation

	e=Far Field Phase Centers (lambda)	**d=Far Field Phase Centers (inches)**	**2*d*sin(θ) (inches)**
A1	22.5	26.57480315	-4.17
A2	19.5	23.03149606	-3.61
A3	16.5	19.48818898	-3.06
A4	13.5	15.94488189	-2.50
A5	10.5	12.4015748	-1.95
A6	7.5	8.858267717	-1.39
A7	4.5	5.31496063	-0.83
A8	1.5	1.771653543	-0.28
B8	1.5	1.771653543	0.28
B7	4.5	5.31496063	0.83
B6	7.5	8.858267717	1.39
B5	10.5	12.4015748	1.95
B4	13.5	15.94488189	2.50
B3	16.5	19.48818898	3.06
B2	19.5	23.03149606	3.61
B1	22.5	26.57480315	4.17

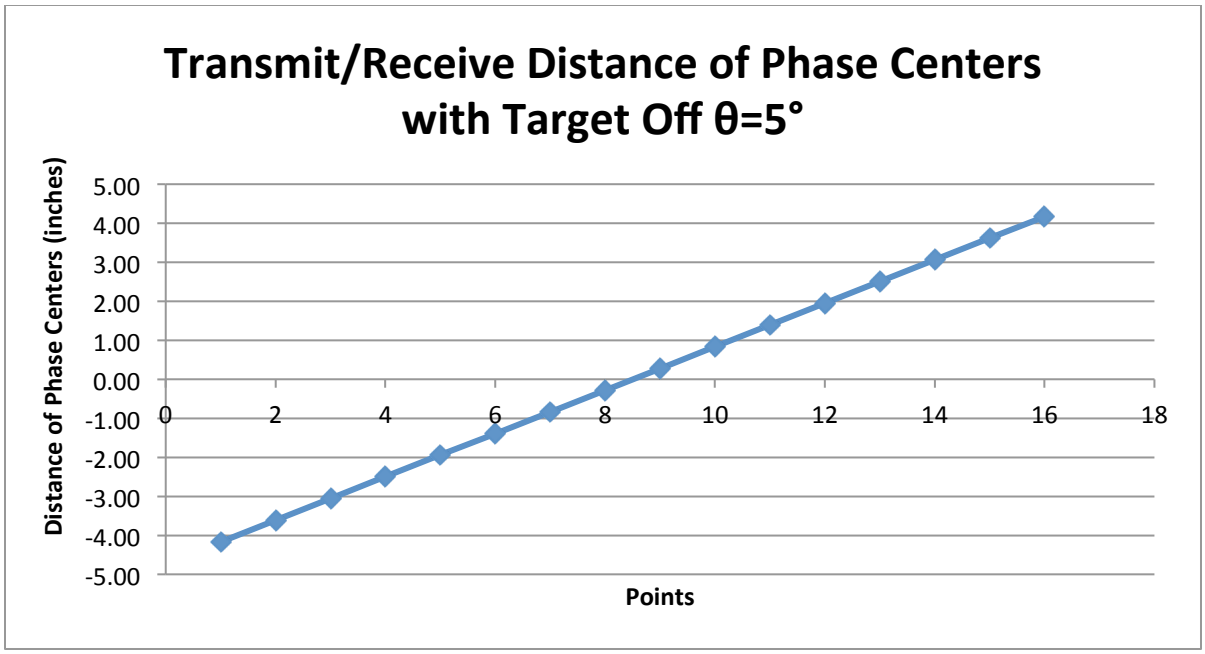


Figure 24. Transmit and Receive Distances of Phase Centers with Target Rotated to θ=5°

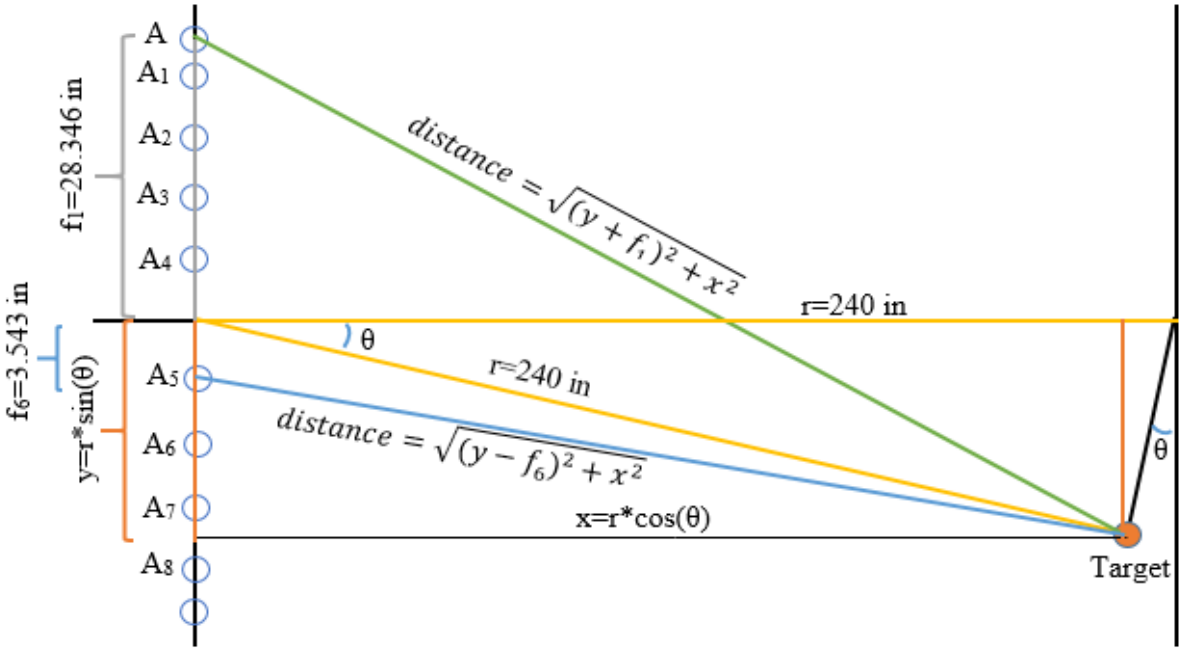


Figure 25. Geometry of Antennas with Target Rotated Off at 5°

Figure 25 above shows the transmit horn as well as the receive horns on the vertical line with the target off-center at five degrees. In this case, the distance relative to the center of the array is denoted as f, in which it is shown that it is 24λ for transmit horn A. Since the target is rotated to θ = 5°, it needs to be accounted for here. The distance to the target is still equal to 240 inches, which is denoted by r, and a right triangle can be formed. The relation is such that from the center of the array down to where the target is located, it is equal to 240 inches times the sine

of the angle θ, and this is denoted as y and is equal to 18.83 inches. The base is denoted as x and it is equal to the distance of the range of 240 inches times the cosine of the angle θ, and the result is 239.26 inches. In order to find the total distance from the horn to the target, the Pythagorean Theorem can be used again for the transmit horn A and the receive horns A_1 through A_4 as follows: $distance\ to\ target = \sqrt{(y+f)^2 + x^2}$.

However, that same relation cannot be used for the receive horns A_5 through A_8 as shown also in Figure 25. For these horns, since they are below the center of the array, the distances relative to the center of the array have to be subtracted from y, which is the following: $distance\ to\ target = \sqrt{(y-f)^2 + x^2}$.

The calculations for the distance to point on the radius of the range, which are the path lengths, are shown below in Table 15. The same process of calculating the sums of the transmit and receive paths to each antenna from the boresite calibration is applied in this case as well. The path length for transmit antenna A is added to the respective path lengths for receive antennas A_1 through A_8, and it is likewise done for transmit antenna B and the receive antennas B_1 through B_8.

For the Resultant column in the table, the sums of the path lengths with the target off five degrees were subtracted from the sums of the path lengths at boresite. For example, for receive antenna A_1, the sum of the path length for boresite calibration is equal to 482.95 inches and the sum of the path length with the target off five degrees is equal to 487.07 inches. The subtraction result is equal to -4.13 inches.

The resultant values are converted from inches to degrees by first converting them to lambda values and multiplying it by 360°. All the distances get converted to phase because a radar can essentially be considered a phase machine, which is why the distance differences were realized. In the error column in inches, the results of the resultant in inches are subtracted from the results of the 2*d*sin(θ) calculated previously in Table 14 above.

Table 15. Calculating Error at Max Angle 4.5°

CALCULATE ERROR AT MAX ANGLE						
	Distance to Point on Radius of Range (inches)	**Sum of Tx and Rx Path to Each Antenna (inches)**	**Resultant (inches)**	**Resultant (deg)**	**Error (inches)**	**Error (deg)**
A	243.87					
A1	243.21	487.07	-4.13	-1257.819076	-0.04	-13.218
A2	242.04	485.90	-3.58	-1091.478135	-0.03	-10.088
A3	241.07	484.93	-3.03	-923.6783062	-0.03	-8.4158
A4	240.30	484.17	-2.48	-754.8362734	-0.03	-7.7861
A5	239.75	483.61	-1.92	-585.3829798	-0.03	-7.7678
A6	239.40	483.27	-1.36	-415.7582631	-0.03	-7.9209

A7	239.26	483.13	-0.81	-246.4052117	-0.03	-7.8023
A8	239.33	483.20	-0.26	-77.76440994	-0.02	-6.9714
B8	243.21	482.66	0.29	88.65160372	-0.01	-3.9158
B7	242.04	481.48	0.84	254.9925449	0.00	-0.7851
B6	241.07	480.52	1.39	422.7923735	0.00	0.88674
B5	240.30	479.75	1.94	591.6344063	0.00	1.51636
B4	239.75	479.20	2.50	761.0876999	0.01	1.53471
B3	239.40	478.85	3.05	930.7124166	0.00	1.38164
B2	239.26	478.71	3.61	1100.065468	0.00	1.50024
B1	239.33	478.78	4.16	1268.70627	0.01	2.33108
B	239.45					

In Figure 26 shown below, the values of the sums of the transmit and receive paths to each antenna are plotted out, and it's taking on the shape of a slope with a hump in the middle, which is desirable. When the processing is being done and the target is across at an angle, it would reflect back a phase slope to each one of the horns that's more severe as it's off at an angle. The slope of that response to each horn when the distance is converted to phase will used to determine the location in the angle space. The ideal result is to have a linear slope. When the target is placed off five degrees, then a response of a linear slope is desired and it would be known if there's a scatter there.

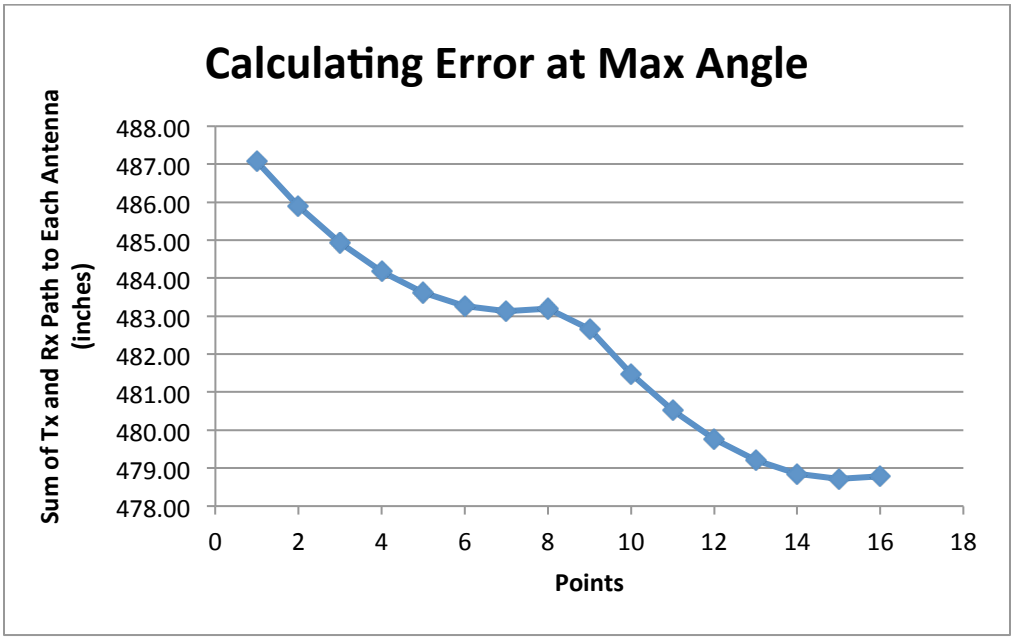


Figure 26. Sum of Tx and Rx Path to Each Antenna for Error Calculation

Figure 27 below shows the resultant, in inches, plotted out and it ends up being a line that is increasing from left to right, which means that calibration is holding. So when the target is off an angle and the different path length differences are calculated and then the original calibration

for the errors at boresite is subtracted, a linear response is obtained, which is the desired response. The next thing to do is to compare that to the d*sin(θ) reference.

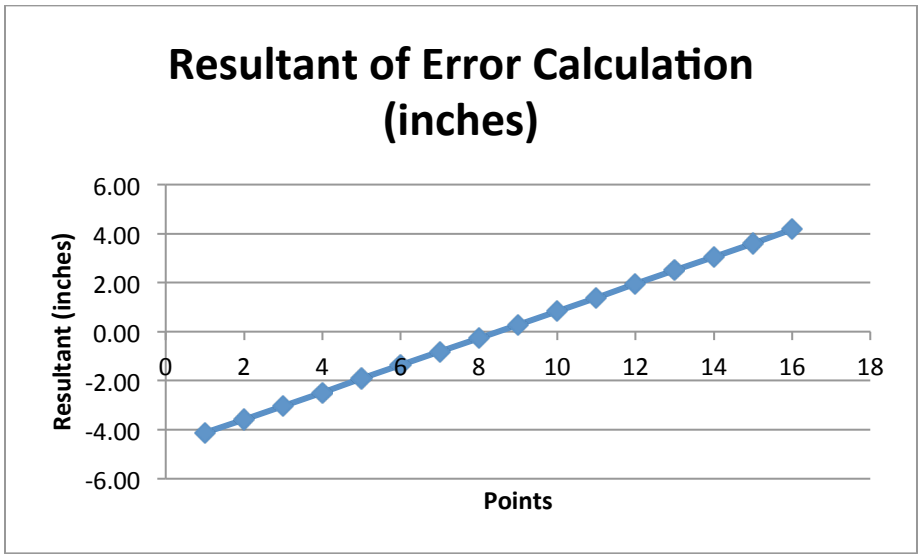


Figure 27. Error Calculation Resultant

In Figure 28 below, the results for the error calculations in degrees are plotted out. This ends up being the phase error that occurs. If everything were ideal, for example if the range was set to far field at 24,000 inches instead of 240 inches, the shape would stay the same but the error would go down to a very small value and that final difference is negligible. At 240 inches, there are ripples, which are the errors. If a perfect scatter at 5° is obtained, then a linear slope would not be obtained as though it was in far field, and instead there be errors obtained.

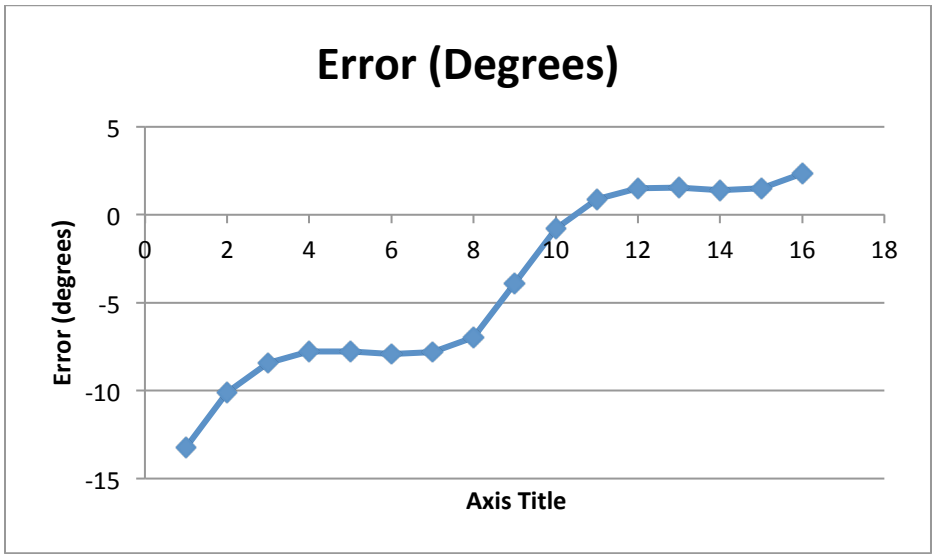


Figure 28. Error for Max Angle

4 Test Plans

4.1 System and Integration Test Plan

The entire system includes the electrical system, the antenna structure, and the signal processing. In goal of testing the system as a whole is to detect the metal trihedral within the scene extent. Based on the calculations in the IQ demodulator description in the system requirements section when the trihedral is in the center of the 40in x 40in scene extent with the I and Q channels can be a maximum of 100mV. As the trihedral moves within the scene extent (as long as the distance from the structure stays 20 feet) the signal reflections will come from different receive antennas which result in a different angles of reflections. This causes the I and Q channel voltages to change. In a controlled environment with RF absorbing foam, when there is no metal in the scene extent there should be no reflections thus the I and Q voltages should be 0mV. This is because the radar cross section will be 0 which leads to a zero result for the received power of the radar range equation.

4.2 Electrical Components Test

There are two types of electrical components: the RF components and the power supply. The plan for testing the RF components involved using a spectrum analyzer (peak power function) to verify the input and output power in the RF components matched the power levels in the design. There are three subsystems that contain RF components: the transmit chain, receive chain, and LO chain of the IQ demodulator. As for the power supply the method of testing the outputs involved using a voltmeter to measure the voltage generated from each power supply output.

4.2.1 Transmit Path Components

Input and output power levels for each transmit chain components are listed in the table below, as well as the frequency of the signals. In addition, there is a test result form for the VCO shown below. See appendix for the entire set of test forms. There were two series of tests that were conducted on the transmit signal chain. The first set where the RF signal detector was used and the second set where the spectrum analyzer was used. The spectrum analyzer was not used to measure the output of each component because this was accomplished by using the RF detector. The spectrum analyzer was used to measure the output of the VCO and the SP4T switch. This was done after the power levels for each RF component were verified using the RF detector.

Table 16: Transmit Path Components Power Levels

Component	Input Power		Output Power		Frequency
	[dBm]	*[mW]*	*[dBm]*	*[mW]*	*[GHz]*
Voltage Controlled Oscillator (VCO)	0.000	1	-4.000	0.398	5
Super Ultra Wideband Amplifier	-4.196	0.381	21.804	151.501	5
Single Pole Double Throw (SPDT) Switch	21.530	142.233	19.530	89.743	5

Fixed Attenuator (10dB)	19.413	87.347	9.413	8.735	5
Frequency Multiplier	9.413	8.735	-3.088	0.491	10
Ultra Wide Bandwidth Amplifier	-3.088	0.491	8.913	7.785	10
Variable Attenuator	8.795	7.577	-3.205	0.478	10
Band Pass Filter	-3.323	0.465	-6.323	0.233	10
Power Amplifier	-6.518	0.223	25.482	353.319	10
Fixed Attenuator (3dB)	25.482	353.319	22.482	177.079	10
Single Pole Four Throw (SP4T) Switch	22.364	172.352	20.364	108.747	10

Scheduled Test Reporting Form

Test Item: Voltage Controlled Oscillator (VCO) – Spectrum Analyzer
Tester Name: Joshua Cushion
Test Date: 3/21/2015
Test Time: 12:30 PM
Test Location: A314
Test Objective: To ensure that the VCO generates an output signal with the correct power and frequency.

Requirements:

- 1- HMC820LP6CE VCO board and USB interface board
- 1- DC power supply
- 1- Spectrum Analyzer (>10.5GHz Capability)
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- Various attenuation pads

Procedure:

1. Mount the VCO board at connector J3 onto the USB board at J2. The SEN pin on J3 should be connected to pin 11 of J2.
2. Set the DC power supply to +5.5Vdc
3. Connect the USB interface board and the PC using the USB cable
4. Copy serial number FTVD4CZ8A into blank serial number space and click open interface
5. Select the HMC820LP6CE from the PLL with Integrated RF VCOs dropdown box.
6. Connect the output of the VCO to the input of the 38dB attenuator pads.
7. Connect the output of the pads to the input of the spectrum analyzer.
8. Connect the cables from the power supply to the terminals on the VCO board
    a. TP3: +5.5Vdc
    b. TP4: GND
9. Enable the power supply
10. In the window of the GUI, set the frequency of the VCO to 500 MHz.
11. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
38	-41.96	-3.96	0.402	4.631	-4	0.398	5

FAILED

Comments: VCO does not generate a high enough frequency such that the signal once multiplied by the frequency multiplier, will be within the pass band of the band pass filter. This component will be replaced by the RF signal generator.

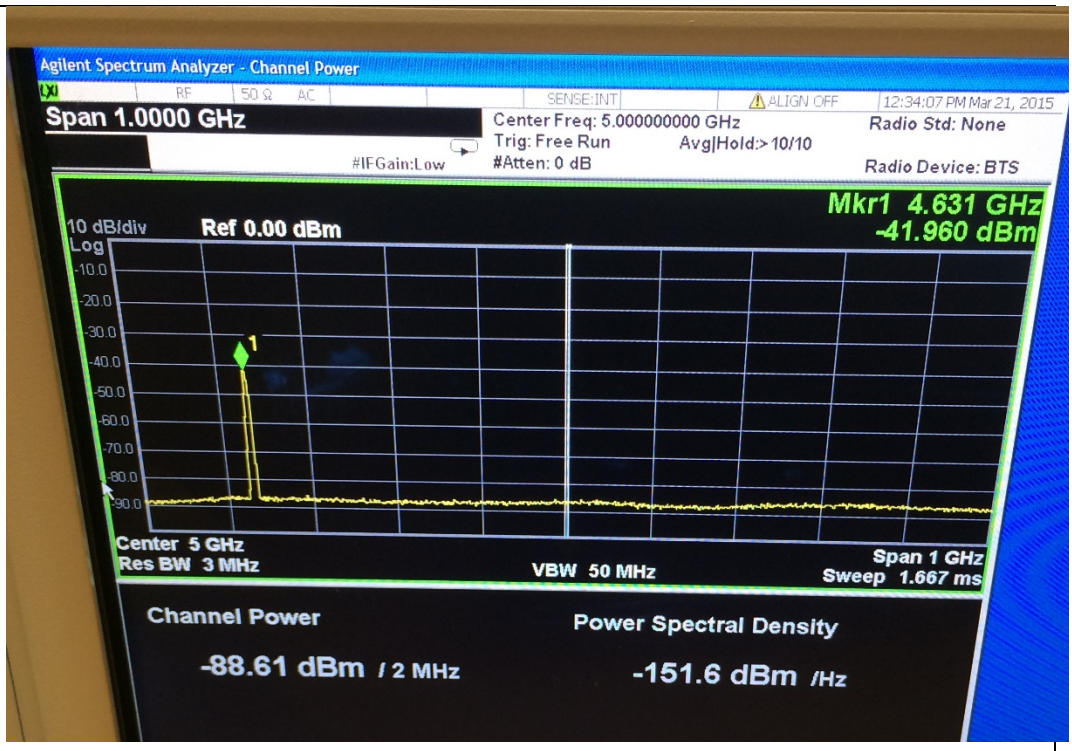


Figure 29: Output of VCO (spectrum analyzer)

4.2.2 Receive Path Components

Input and output power levels for each receive chain components:

Table 17: Receive Path Components Power Levels

Component	Input Power		Output Power		Frequency
	[dBm]	*[mW]*	*[dBm]*	*[mW]*	*[GHz]*
Single Pole Sixteen Throw (SP16T) Switch	-53.251	4.731E-06	-57.951	1.603E-06	10
Band Pass Filter	-58.068	1.560E-06	-61.068	7.820E-07	10
Low Noise Amplifier (LNA-SLNA-120-38-22-SMA)	-61.068	7.820E-07	-23.068	4.934E-03	10
Variable Attenuator (SA4077)	-23.342	4.632E-03	-37.342	1.844E-04	10
Low Noise Amplifier (LNA-SLNA-180-38-25-SMA)	-37.460	1.795E-04	0.540	1.132E+00	10
Radio Frequency (RF) IQ Demodulator	0.070	1.016E+00	-6.930	2.028E-01	10

Scheduled Test Reporting Form

Test Item: Receive Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the peak power output from the first low noise amplifier (SLNA-120-38-22-SMA) in the receive chain.

Requirements:

- Assembled Receive Chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (20 dB) – needed if RF signal generator cannot generate an output signal with and amplitude of -50 dBm

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
LNA:SLNA-120-38-22-SMA	12	250	-	-
Single Pole 16 Throw Switch	5	550(max)	-12	200(max)
1- 0V (SP16T VCTL)	0	-	-	-

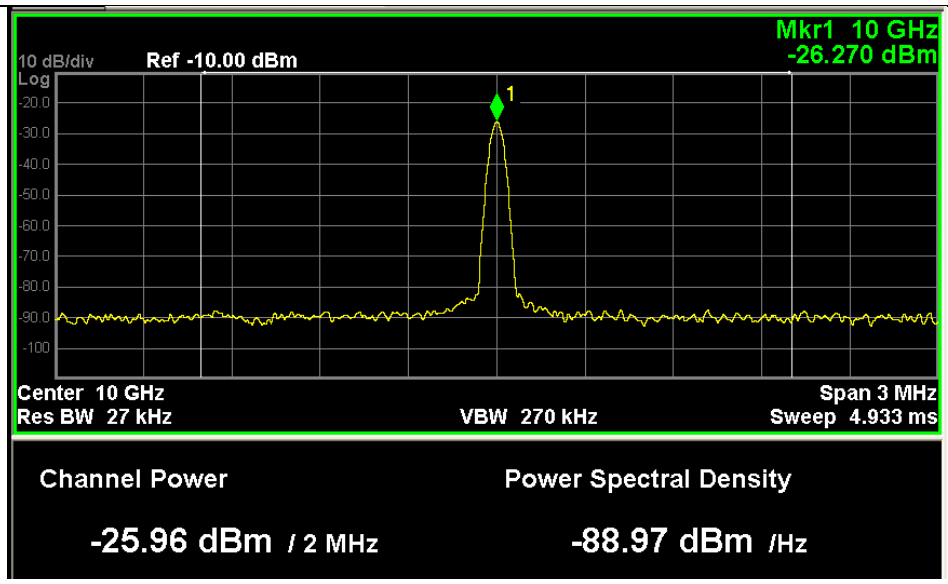
Table 1: Power Supply Requirements

Procedure:

1. Connect the output of the RF signal generator to the input of the 20 dB attenuator pads.
2. Connect the output of the 20 dB pads to the input of the spectrum analyzer using a short RF cable.
3. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
4. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -51 dBm and frequency of 10 GHz.
5. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the SP16T switch at the desired channel.
6. The COM port of the SP16T switch should be connected to the band pass filter.
7. The BPF should be connected to the input of the low noise amplifier.
8. Connect the RF Out connector on the LNA to the input of the analyzer.
9. Set one of the CTL voltage supplies to 0V and connect it to the SP16T control pin that corresponds to the correct channel connected to the RF signal generator. The positive terminal to the CTL pin and the ground terminal to the GND pin.
10. Enable the power supplies in the following order:
    a. -12V
    b. +5V
    c. +12V
    d. +0V(VCTL)
11. Record the peak power and frequency shown on the spectrum analyzer.
12. Disable the power supplies in this order:
    a. +0V(VCTL)
    b. +12V
    c. +5V
    d. -12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
3	-26.270	-23.270	0.00471	10	-23.068	4.934E-3	10



Comments:
PASSED
The attenuation was due to the loss in the cable connected to the spectrum analyzer.

4.2.3 LO IQ Demodulator Path Components

Input and output power levels for each receive chain components:

Table 18: LO IQ Demodulator Path Components Power Levels

Component	Input Power		Output Power		Frequency
	[dBm]	*[mW]*	*[dBm]*	*[mW]*	*[GHz]*
Voltage Controlled Oscillator (VCO)	0.000	1.000	-4.000	0.398	5
Super Ultra Wideband Amplifier	-4.196	0.381	21.804	151.501	5
Single Pole Double Throw (SPDT) Switch	21.530	142.233	19.530	89.743	5
Fixed Attenuator	19.413	87.347	9.413	8.735	5
Frequency Multiplier	9.217	8.350	-3.283	0.470	10
Ultra Wide Bandwidth Amplifier	-3.283	0.470	8.717	7.442	10
Fixed Attenuator	8.599	7.243	5.599	3.630	10
LO (IQ Demodulator)	5.129	3.258	-	-	10
Scheduled Test Reporting Form					

Test Item: LO IQ Demodulator Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the transmit signal from the going into the LO port of the IQ demodulator is at the designed peak power of approximately 5.559dBm.
Requirements:

- Assembled LO IQ demodulator chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 1- Pulse generator
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (39 dB total)

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-

Table 1: Power Supply Requirements

Procedure:

1. Connect the output of the RF signal generator to the input of the spectrum analyzer using a short RF cable.
2. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
3. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -4 dBm and frequency of 5 GHz.
4. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the super ultra wide bandwidth amplifier.
5. Connect the RF Out connector on the 3dB pad (connected to the ultrawide bandwidth amplifier) to the input of the attenuator pads using the short RF cable.
6. Connect the output of the pads to the input of the analyzer.
7. Set one of the CTL voltage supplies to 0V and connect it to the SPDT. The positive terminal to the CTL pin and the ground terminal to the GND pin.
8. Enable the power supplies in the following order:
    a. +12V
    b. +5V
    c. +12V (ultra wide bandwidth amp)
9. Record the peak power and frequency shown on the spectrum analyzer.
10. Disable the power supplies in this order:
    a. +12V (ultra wide bandwidth amp)

b. +5V
c. +12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
42	-37.262	4.738	2.977	10	5.599	3.258	10

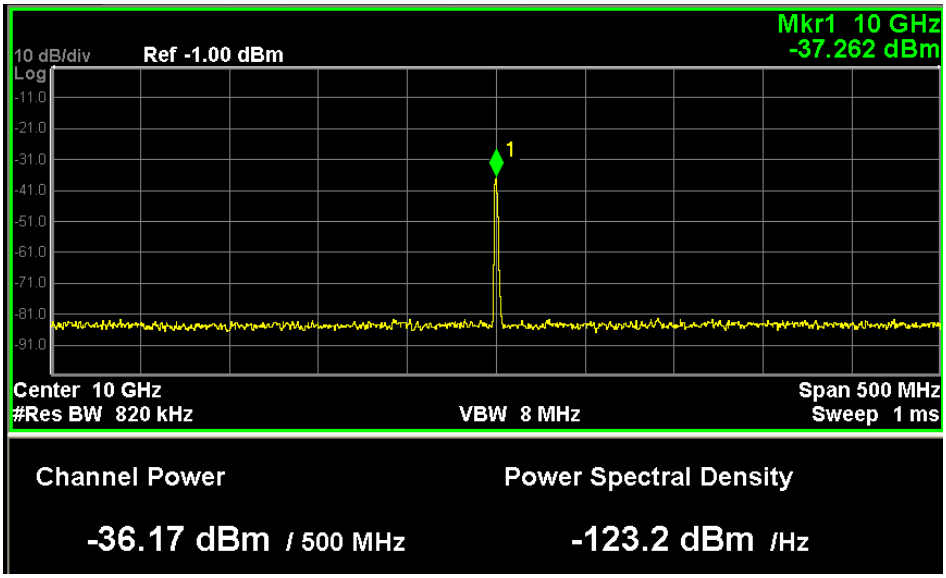


Figure 30: Peak power measured

Comments:
PASSED
39 dB loss for attenuation pads, 3 dB for the RF cable connected at the output of the 3dB pad coming from the ultra-wide bandwidth amplifier to the spectrum analyzer.

4.2.4 Power Supply Board

Table 12 shows the voltage and current input requirements for each component. In order to ensure that the power supply board would provide the correct voltages, each output was measured using a voltmeter. As for the current, the components would not turn on if the there was insufficient current being supplied to the component.

Table 19: Component Power Supply Requirements

QTY	Part Name	V+(Vdc)	I+ (mAdc)	V-	I-(mAdc)

				(Vdc)	
1	VCO	3.3	45	-	-
1	SPDT Switch	5	1.4	-	-
1	SP4T Switch	5	160	-5	50
1	SP16T Switch	5	550(max)	-12	200(max)
1	IQ Demodulator	5	110	-5	-
1	Super Ultra Wideband Amplifier	12	400(max)	-	-
2	Ultra Wide Bandwidth Amplifier	12	62	-	-
1	Low Noise Amplifier SLNA-120-38-22-SMA	12	250	-	-
1	Low Noise Amplifier SLNA-180-38-25-SMA	12	280	-	-
1	Power Amplifier	15	900	-	-

5 Mechanical Design and Analysis

5.1 Overview of the Design

The goal of the project was to create a functioning, two-dimensional, static Synthetic Aperture Radar (SAR) and have it detect metal in a scene extent of 30x30 inches. A typical SAR is active, utilizing the movement of one antenna to simulate multiple receive antennas after transmitting a signal, generating multiple phase centers. A phase center is the midpoint between transmit and receive antennas. Based on the time the signal takes to return and the phase center the reflected signal collides with will determine the phase of the signal. From the signal's phase, the location and formation of the object can be established with advanced signal processing. The radar system for this project is static, meaning immovable and relies on the moment of the object. To construct a static SAR imager, twenty horns antennas will be aligned together, similar to the layout of a phased array system. Ten antenna horns will be aligned in the vertical axis of the structure and ten antenna horns will be aligned in the horizontal axis of the antenna horn structure. At the end of each horn array, there will be a transmit antenna. Then, one of the end horn antennas will transmit a signal and have the neighboring horn antennas switch on and off to create the multiple phase centers, similar to an active SAR. If multiple radar components are configured correctly and the signal processing is efficient, the static SAR design for this project will be able to determine where an object with a high radar cross section is located on a screen, based on two-dimensional imaging.

5.2 Overview of Antenna Structure

The horn antenna structure will consist of both steel and aluminum based metals for the convenience of machinability and cost. The structure will be made in separate sections, components, to bolt together. This is the most efficient plan attack because the structures width and height is 5.5 ft. x 5.5 ft. respectively. The design has four separate quadrants, material of steel, which will be connected together using a c-channel divider to allow enough space in between quadrants for each horn antennas to be placed. Below in Figure 31 shows the 3-D rendering for how the horn antennas are held together by two quadrant panels and how the connector/divider holds the two quadrant panels. Figure 32 shows the improvising made to adjust to fabrication error.

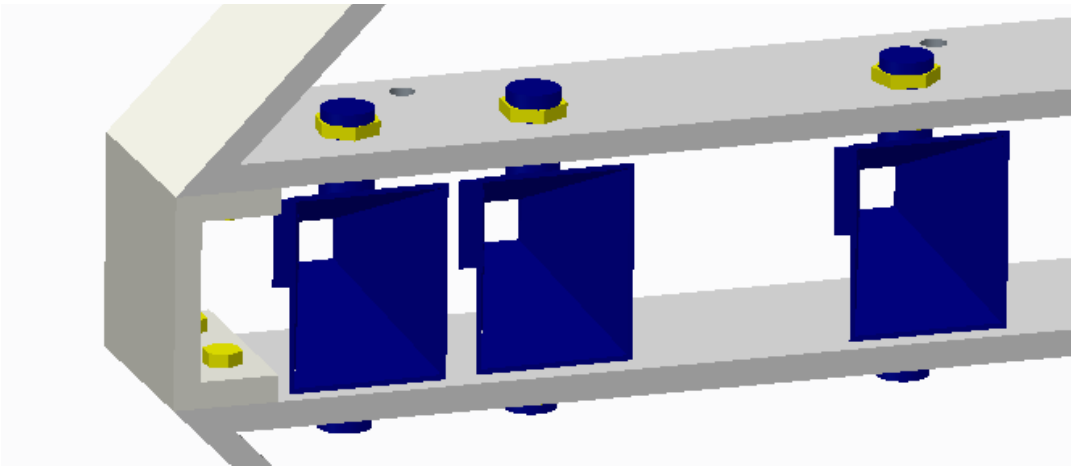


Figure 31: 3-D Model Showing Horn Placement on Structure

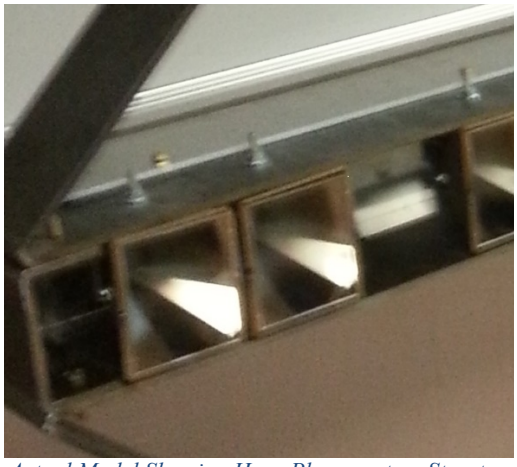


Figure 32: Actual Model Showing Horn Placement on Structure

Due to the improper fabrication from our manufacturing source, the horns are not flush with the front of the structure. To improvise, the horn antenna was offset past the horn cover, so no interference could come from the steel metal and disrupt the signal. Four horn covers were bolted onto the back of the structure to cover the horns and the wires running to the horns. Figure 33, displays the horn covers which are displayed in yellow. The covers will also add extra support for the structure. Also, Figure 34 shows the full design of the horn structure without the stand and component box.

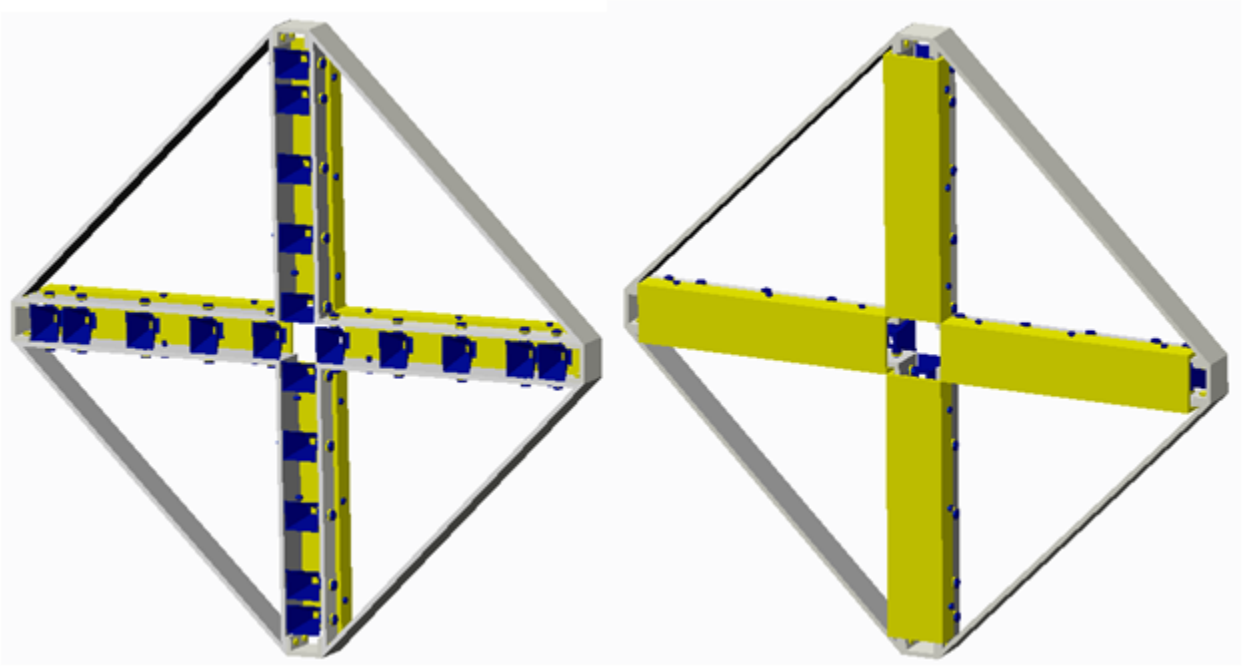


Figure 33: 3-D Model of the Horn Antenna Structure without Stand and Component Box

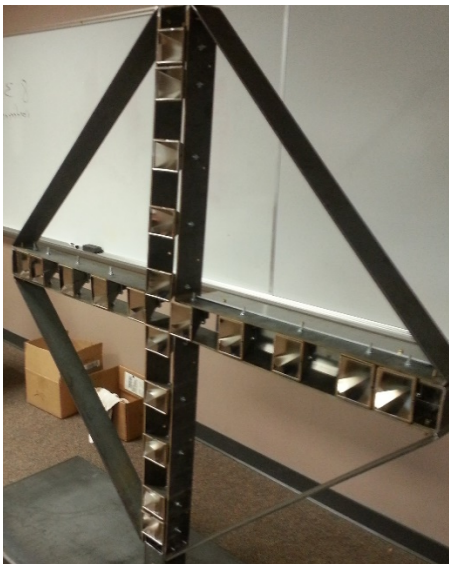


Figure 34: Actual Model of the Horn Antenna Structure without Component Box

After much rendering to produce a design concept, the structure came to life with the fabrication of steel to produce the quadrant panels, c-channel connector, and the structure stand. This provided much support to the structures weight. Steel is approximately $2.5\frac{g}{cm^3}$ denser than aluminum which will provide for a more sturdy structure when it comes to stress analysis. More detail of the stress analysis will be provided later in the report.

5.3 Antenna Structure Design

From the Mechanical aspect, the design of the antenna structure has been modified. Also, there have been additions to the structure. After the structure came back from Metal Fabrications the structure did not come together smoothly. The horn holders, stand to structure c-connector, and component box had to be customized. Two additional support poles had to be added to the structure also. The trihedral was also constructed differently than had been anticipated.

5.3.1 Refined Structure

In the following section, explanations of the modified structure will be presented. Each modification is so the structure can come together and for better support. The new modifications have been calculated and adjusted accordingly to fit our parameters.

5.3.1.1 Horn Holders

The c clamp holder from the fabrication shop fit over the horn antenna, but when the waveguide adapter were to be bolted on, the horn holders interfered. Below in Figure 35 shows the cut horn holder allowing the waveguide adapter to be bolted properly.

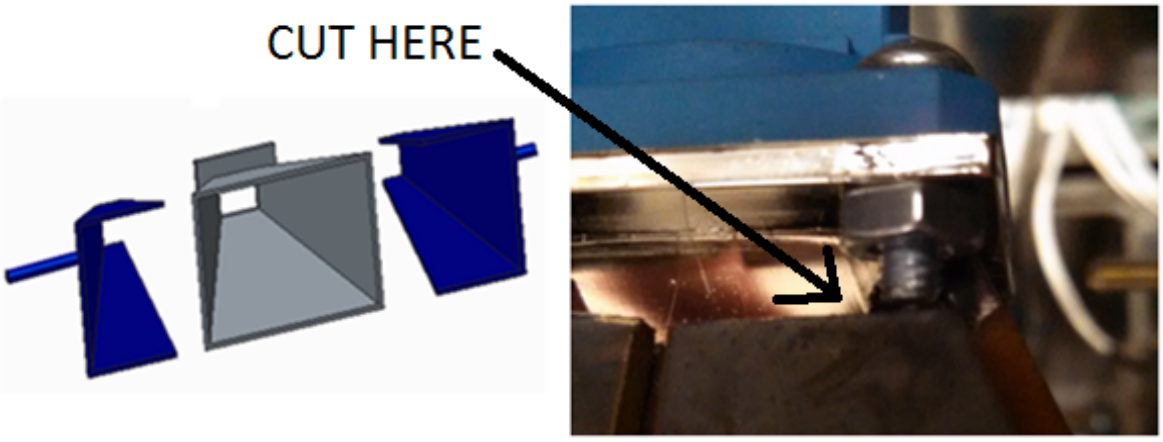


Figure 35: Horn Holder Adjustment

5.3.1.2 Stand to Structure C-Connector

The ME team did account for nuts and the head of bolts to be flush with the wall surface of the connector, however, the fabrication shop added an extra piece of metal inside the connector to have the structure more stable when connected to the stand. The fabrication shop did not leave enough space to have a nut or head of bolt flush with the wall surface. Figure 36 shows the cut made to allow proper assembly.

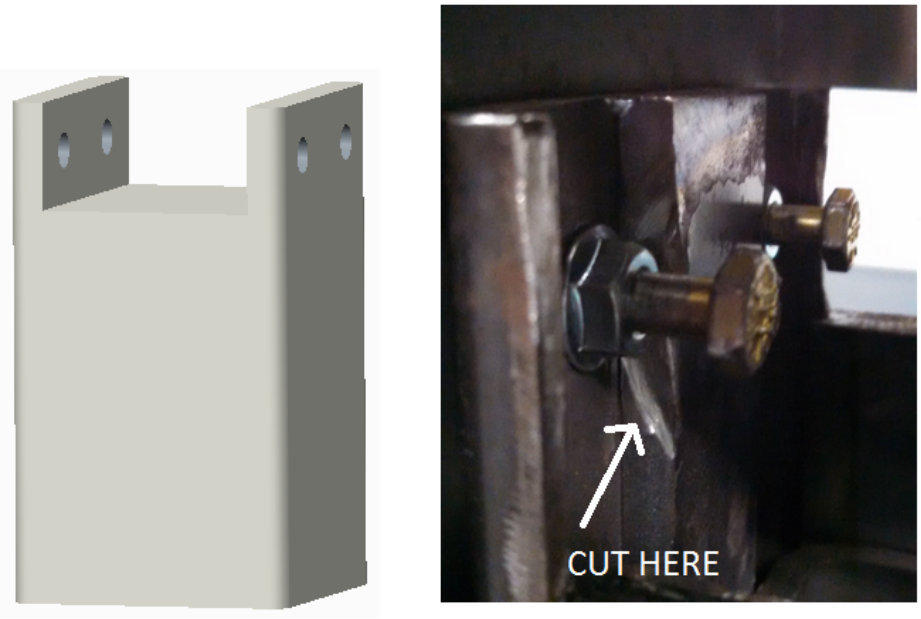


Figure 36: Stand to Structure C-Connector Adjustment

5.3.1.3 Component Box

The component box to hold the electrical components had to be cut because of poor fabrication of the horn covers which go on the back of the quadrant panels. Below in Figure 37 shows the component box cut to allow proper assembly.

Figure 37: Electrical Component Box Adjustment

5.3.1.4 Support Poles

After the entire structure was assembled, the structure would slightly sway from side to side. Two support posts were created to account for this effect. Figure 38 shows the support posts.

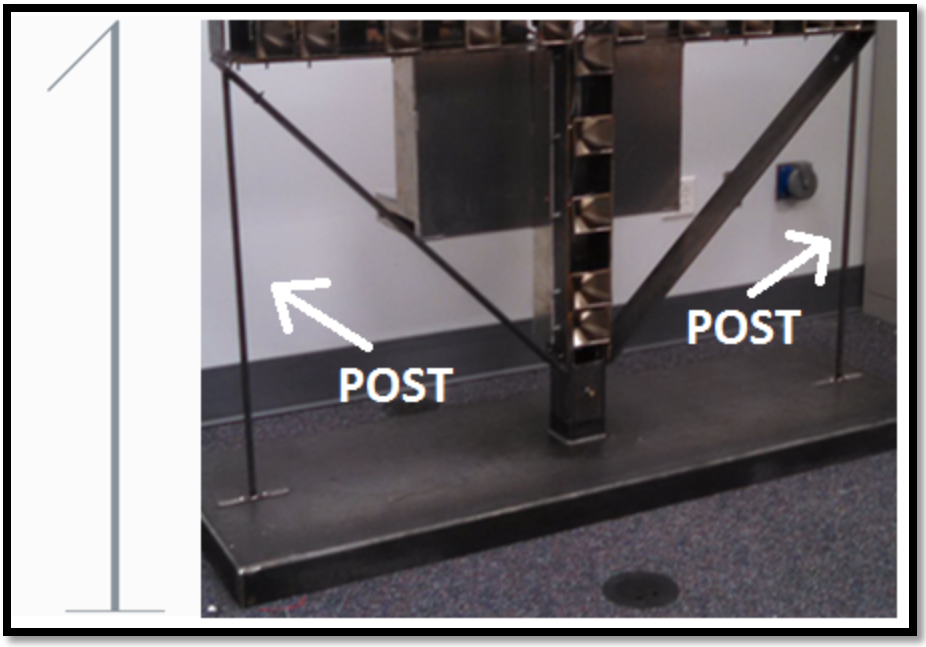


Figure 38: Support Post Addition

5.3.1.5 Trihedral

The Trihedral, commonly known as a metal corner reflector, was to be fabricated with three equilateral triangle planes. The initial material chosen was aluminum. These planes are joined together to form a triangular pocket to receive and reflect waves, this is reflected in Figure 39. Instead, a 2 inch PVC post was cut approximately 45 inches long for the pole. The trihedral was made by cutting the corner of a tin box. This was glued to the top of the post. To keep the post upright an 8.5 by 11 inch acrylic sheet was attached to the bottom side of the post. This can be seen in Figure 27 below.

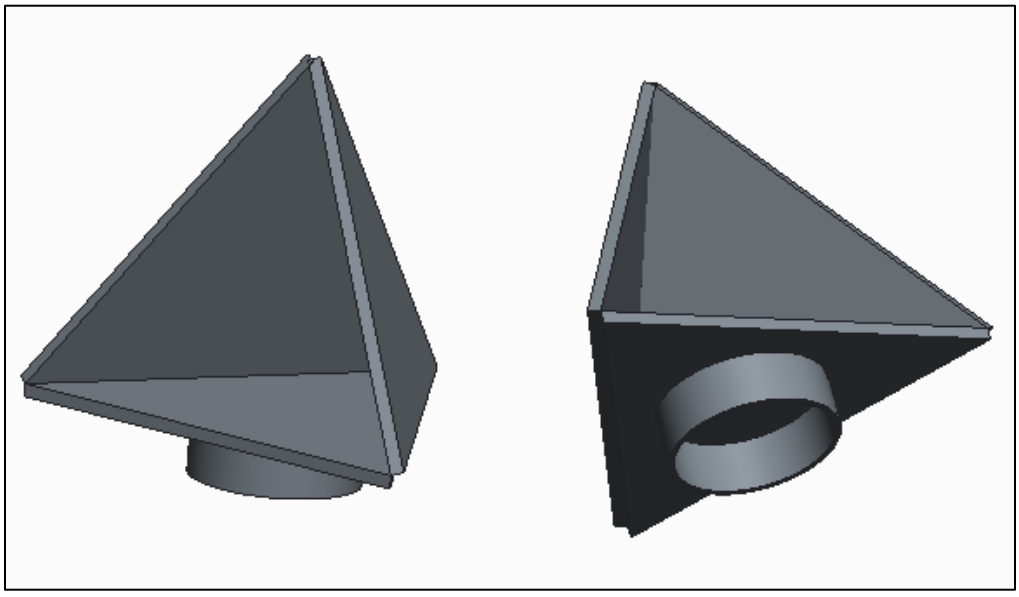


Figure 39: Trihedral assembly used to calibrate radio waves

5.3.2 Horn Alignment

The goal from the sponsor was to have adjustability of the horn on the structure. After the structure was assembled the sponsor requested to align the 20 antenna horns with a laser pointed inside of a 1 ft diameter circle at 20 ft away from the front of the horns. Before the horn could be aligned a method to hold the laser in the center of a horn antenna had to be invented. A horn antenna was used by cutting the waveguide adapter plate off the back of the horn antenna. 2 clear fishing strings were cut and placed across the front of the horn antenna to find the center. This was also done on the side which the waveguide adapter plate was cut. By using sticky putty a laser pointer could be placed in between the 2 x fishing string to have the laser line up perfectly. Below in Figure 40 shows the custome horn alignment tool.

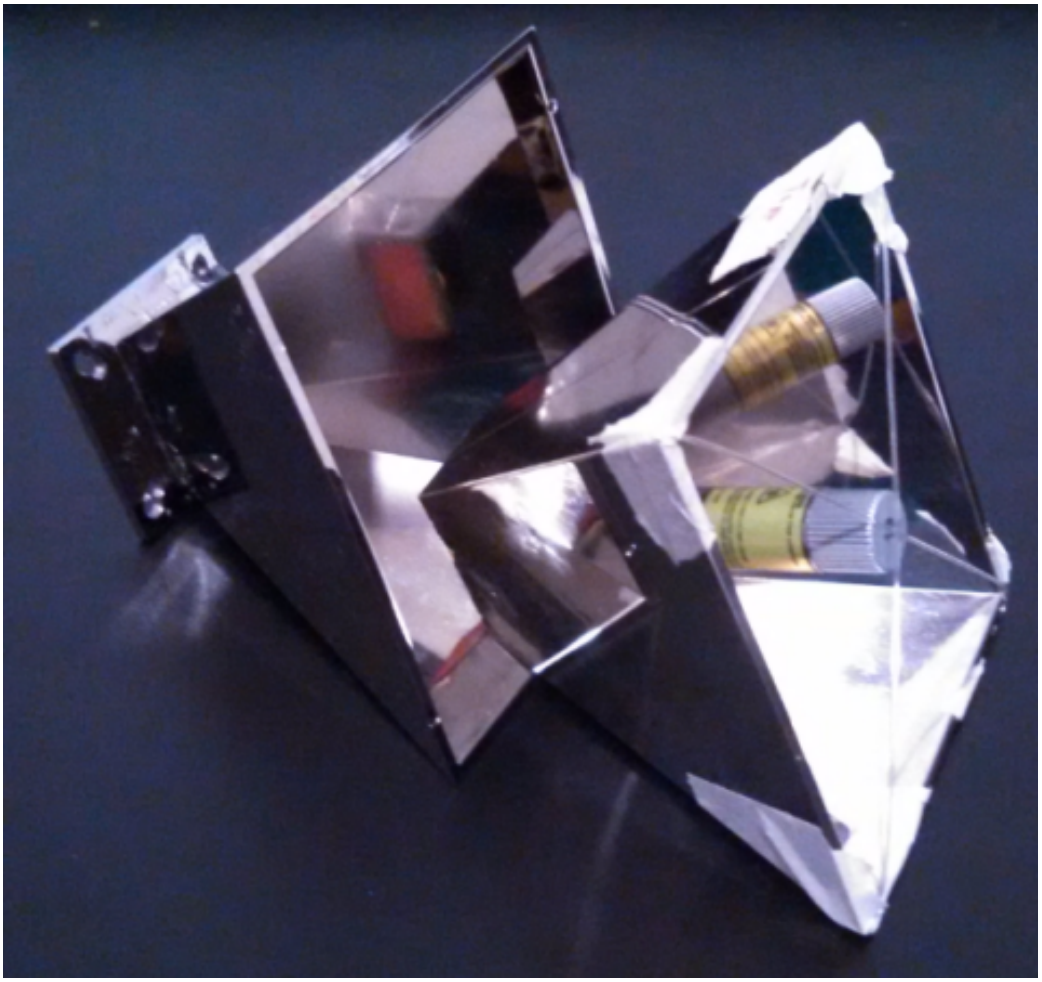


Figure 40: Horn Alignment Tool

5.4 Stress Analysis

Before each component of the structure is analyzed, it is essential that a visual of the whole structure is displayed for reference. Figure 41 is a reference visual for each component listed in the stress analysis section. Following the reference is Table 20 showing the actual weight of each component.

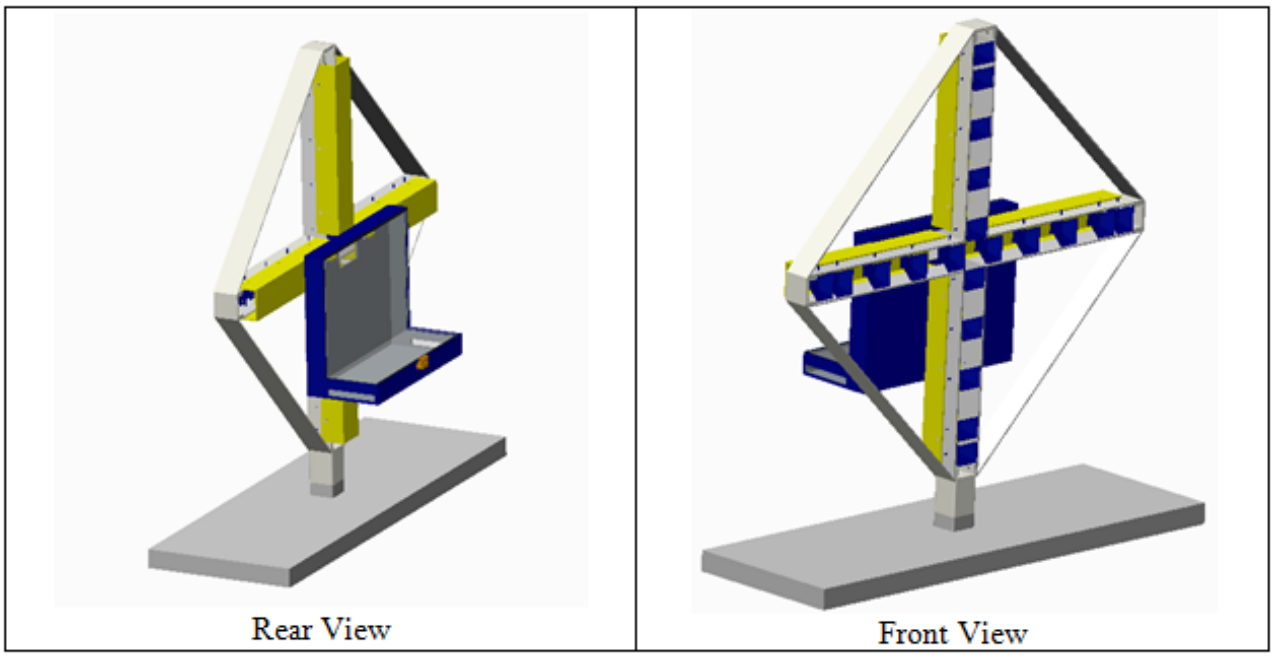


Figure 41: Synthetic Aperture Radar Structure

Table 20: Weight Distribution for Each Component of the SAR Imager Structure

Component	Material	Weight	units
Component Box	Aluminum	33.3	lb.
Quadrant Panel	Steel	24.8	lb.
Quadrant Connector	Steel	3.5	lb.
Quadrant Connector to Stand	Steel	11.8	lb.
Vertical Horn Cover (Top and bottom)	Aluminum	7.9	lb.
Horizontal Horn Cover(Left)	Aluminum	8.0	lb.
Horizontal Horn Cover (Right)	Aluminum	8.0	lb.
Structure Stand	Steel	120.5	lb.
Total		217.8	lb.

5.4.1 Components

5.4.1.1 Aluminum Horn Cover (Left & Right)

Figure 42 displays the stress analysis through displacement. There are two horn covers supplying support for the component box. This was done with two slot inserts cutting the weight of the component box in half. Both slot inserts will be holding approximately a maximum of 20 lbs. The visual in the figure is an over exaggerated depiction of the displacement at the maximum weight. The maximum displacement of deformation at maximum load is 8.8×10^{-6} in. This displacement has no effect on the material, proving the Aluminum 6061 is a valid choice for our structure.

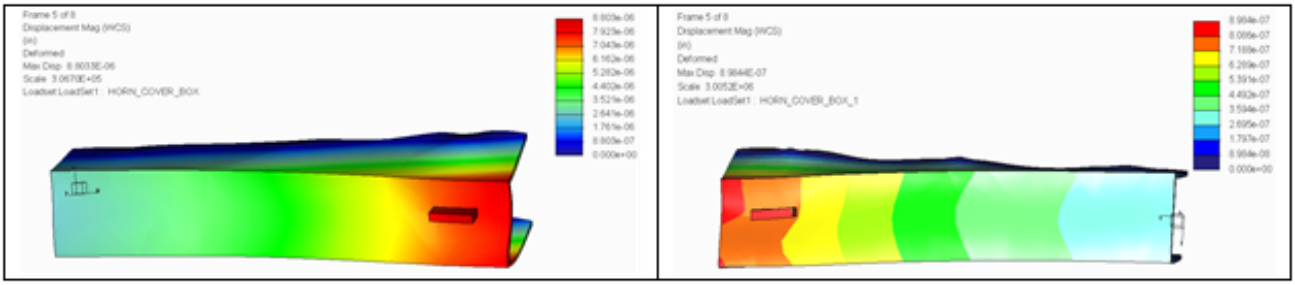


Figure 42: Horn cover for both left and right horizontal horn alignment.

5.4.1.2 Steel Quadrant Panel (Quadrant 1 & 2)

The stress analysis associated with Figure 43 is the quadrant panel for Quadrant 1 and 2. These are the two quadrants located above the centerline of the structure. The displacement in the figure is for Quadrant 1, but because the weight distribution is symmetrical to one another, the displacement will be the same for both quadrants. The maximum deformation displacement on these quadrant panels will be 5.8 x 10^{-5} in at maximum load. The largest load quadrant panel one and two will be holding is approximately 27.5 lbs. As said before, both quadrants will evenly distribute the weight of approximately 56 lbs.

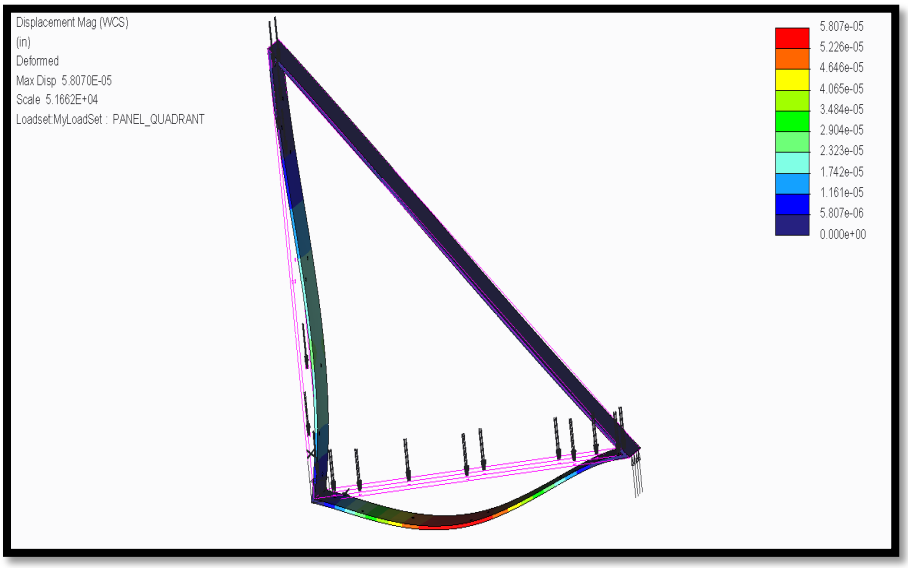


Figure 43: Stress Analysis of Quadrant 1 and 2 Quadrant Panels.

5.4.1.3 Steel Quadrant Panel (Quadrant 3 & 4)

Quadrant Panel 3 and 4 are located below the centerline of the structure. These panels will support the weight of the component box and the two quadrant panels above them. The load is now pulling down on the quadrant panel, rather than pushing down. The horn cover is bolted to the bottom of the quadrant panel creating a pulling force on the panel. In this case, the maximum displacement is 3.0 x 10^{-7} in. This displacement is recorded at the maximum load. Figure 44 has specific details to display the displacement of the material. The Panel will not be deformed from the applied load expected.

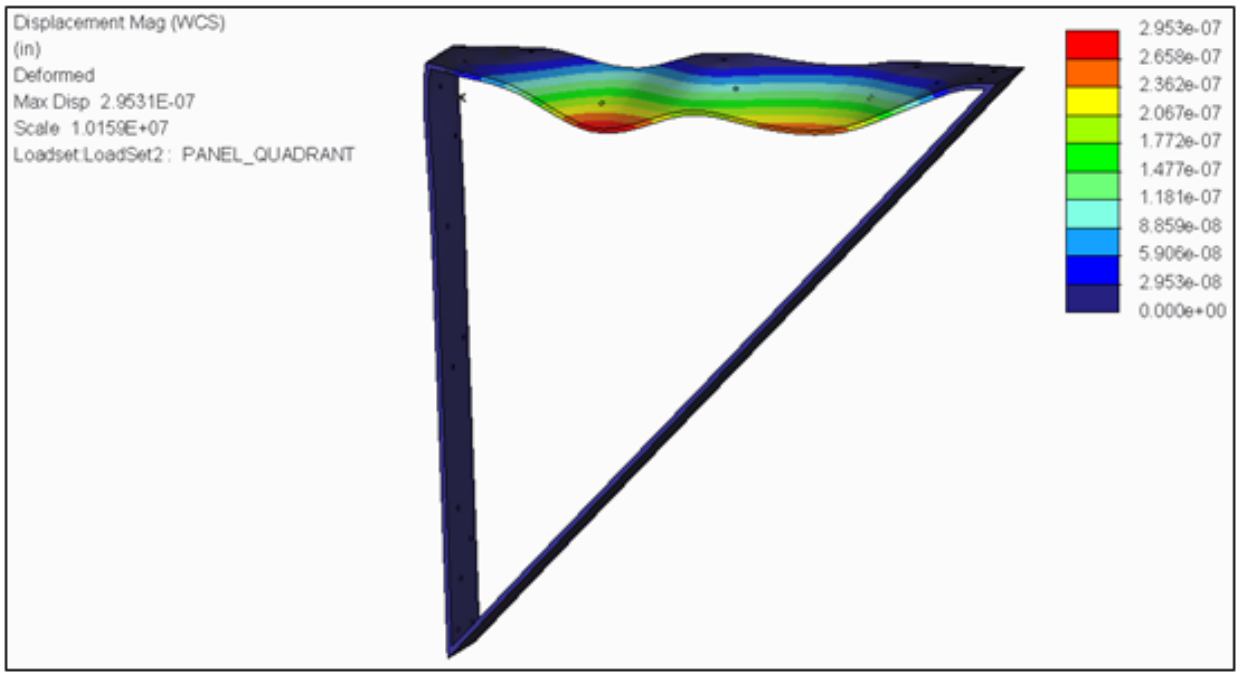


Figure 44: Stress Analysis of Both Quadrant 3 and 4 Quadrant Panels.

5.4.1.4 Steel Connector Channel (Structure to Stand)

The connector channel, Figure 45, is the female component to the structure stand. This component will hold the weight of the whole structure including the four quadrant panels and component box. The connector component was made of thick metal that will support the weight of the entire structure. After stress analysis, the maximum displacement is 6.9 x 10^{-8} in. The maximum load of the structure is roughly 75 lbs. This custom component was designed specifically to withstand the weight of the structure.

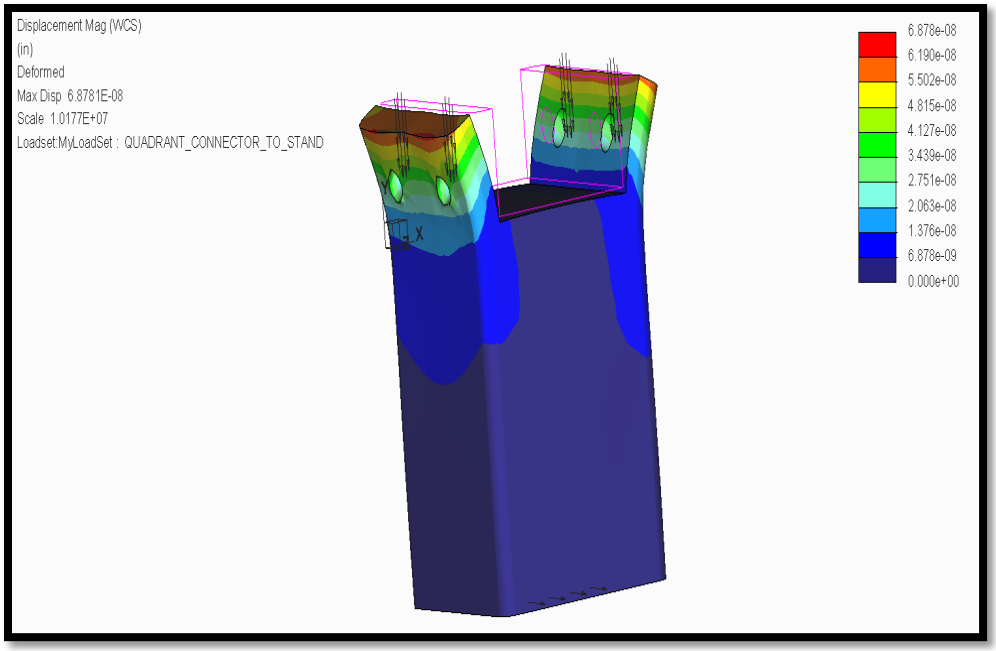


Figure 45: Stress Analysis of C-channel Connecting Structure to Structure Stand.

5.4.1.5 Steel Structure Stand

The structure stand below is again shown at an exaggerated state. Due to the moment the structure causes on the stand, the male component to the connector channel will receive a bending force. From analysis, shown in Figure 46, the maximum displacement is 3.0 x 10^{-8} in. This will cause negligible deflection in the component. The Structure stand itself will withstand the weight of the structure as well. The maximum displacement at the male components is zero inches. The modification of the stand deems suitable to hold the structure.

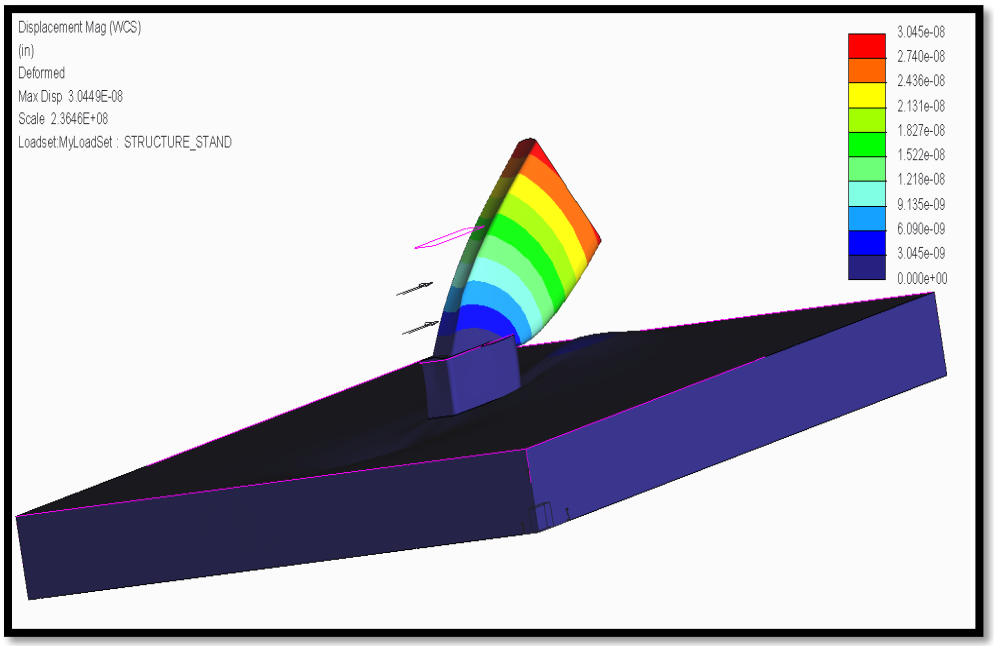


Figure 46: Stress Analysis on Structure Stand Holding the Entire Structure.

5.5 Heat Dissipation Analysis

5.5.1 Electrical Component Placement

The Electrical components was placed inside the components box which was attached to the antenna structure. The components was placed onto an L-shaped sheet of aluminum metal. The FPGA, Power Supply, and Level Shift Circuit was placed on the horizontal while the remaining components was placed on the vertical of the L-shape sheet. A simple 3D model of the old component layout can be seen in Figure 47 below along with the cables excluding the USB, VGA, Power, and switch to horn cables/wires. The figure also includes dimensions of the L-shape sheet. A few components had to be adjusted for convenience of location which can be seen in picture in 5.6 Results section.

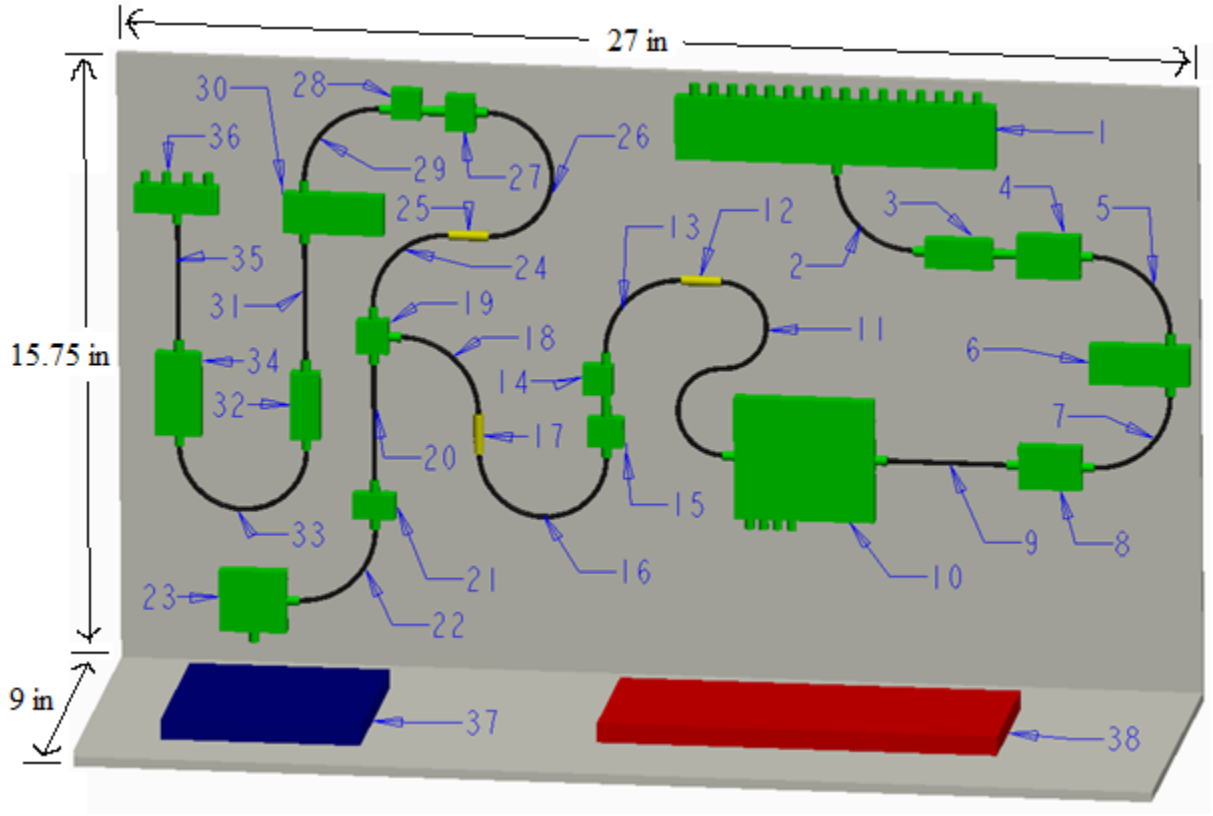


Figure 47: Electrical Components on L-shaped Sheet.

The following list corresponds with the numbers in Figure 25 above.

1 - SP16T Switch
2 - 3 Inch 90 Degree Bend Cable
3 - Band Pass Filter
4 - Low Noise Amplifier
5 - 3 Inch 90 Degree Bend Cable
6 - Variable Attenuator
7 - 3 Inch 90 Degree Bend Cable
8 - Low Noise Amplifier
9 - 3 Inch Cable
10 - IQ Demodulator
20 - 3 Inch Cable
21 – Super Ultra Wide Band Amplifier
22 - 3 Inch 90 Degree Bend Cable
23 - VCO
24 - 3 Inch 90 Degree Bend Cable
25 - Fixed Attenuator
26 - 5 Inch 180 Degree Bend Cable
27 - Multiplier
28 - Ultra Wide Band Amplifier
29 - 3 Inch 90 Degree Bend Cable

11 - 7 Inch S Bend Cable
12 - Fixed Attenuator
13 - 3 Inch 90 Degree Bend Cable
14 - Ultra Wide Band Amplifier
15 - Multiplier
16 - 5 Inch 180 Degree Bend Cable
17 - Fixed Attenuator
18 - 3 Inch 90 Degree Bend Cable
19 - SP2T Switch
30 - Variable Attenuator
31 - 3 Inch Cable
32 - Band Pass Filter
33 - 5 Inch 180 Degree Bend Cable
34 - Power Amplifier
35 - 3 Inch Cable
36 - SP4T Switch
37 - FPGA
38 – Power Supply/Level Shift Circuit

5.5.2 Heat Transfer from Electrical Components

For calculating the heat transfer of the components the box will be treated as a completely closed electrical component box. The first step in finding the temperature rise inside the box was to determine the inside surface area of the box which was calculated to be 12.76 ft^2. The power going into the box was found by totaling the power supplied to each component which was calculated to be 34.8 W. Dividing the total power by the total surface area gives the heat flux inside the box which was calculated to be 2.7 W/ft2. By using the graph in Figure 48 below the temperature rise inside the box was determined to be approximately 13.5 ± 2.8 °C. The error was found by taking 25% of the calculated temperature rise which was suggested from a PENTAIR data sheet [3].

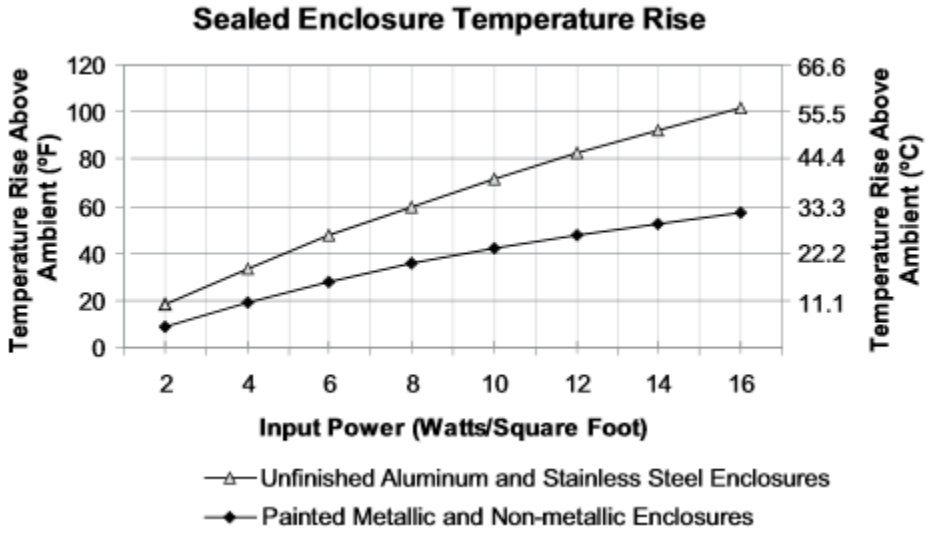


Figure 48: Sealed Enclosure Temperature Rise.

The above calculation was for an average temperature inside the box. The super ultra-wide band, ultra-wide band, low noise, and power amplifier dissipate the most heat inside the box creating hotter spots. Below in Table 21 shows the heat transfer of each electrical component.

Table 21: Heat Transfer of Each Electrical Component

Component	Area (ft2)	Voltage (V)	Current (A)	Dissipated Power (W)	Heat Transfer (W/ft2)
VCO	0.174	3.300	0.045	0.149	0.855
FPGA	0.278	3.300	0.200	0.660	2.376
SPDT	0.005	5.000	0.001	0.007	1.400
SP4T	0.010	5.000	0.160	0.800	78.367
SP16T	0.089	5.000	0.550	2.750	30.938
IQ DEMOD	0.075	5.000	0.110	0.550	7.300
SUPER ULTRA WBA	0.005	12.000	0.400	4.800	897.662
ULTRA WBA	0.005	12.000	0.400	4.800	1031.642
LOW NOISE AMP	0.012	12.000	0.320	3.840	321.488
POWER AMP	0.017	15.000	1.100	16.500	981.818
Total	X	X	X	34.856	3353.846

From Table 14 above the amplifiers dissipate the most heat. A heat sink was ordered with the super ultra-wide band amplifier to ensure proper cooling. The ultra-wide band, low noise, and power amplifiers were kept cool with thermal compound.

5.6 Results

5.6.1 Finished Structure

Once the adjustments were made to the structural components assembly went smooth for the entire structure. Below in Figure 49 show the final structure.

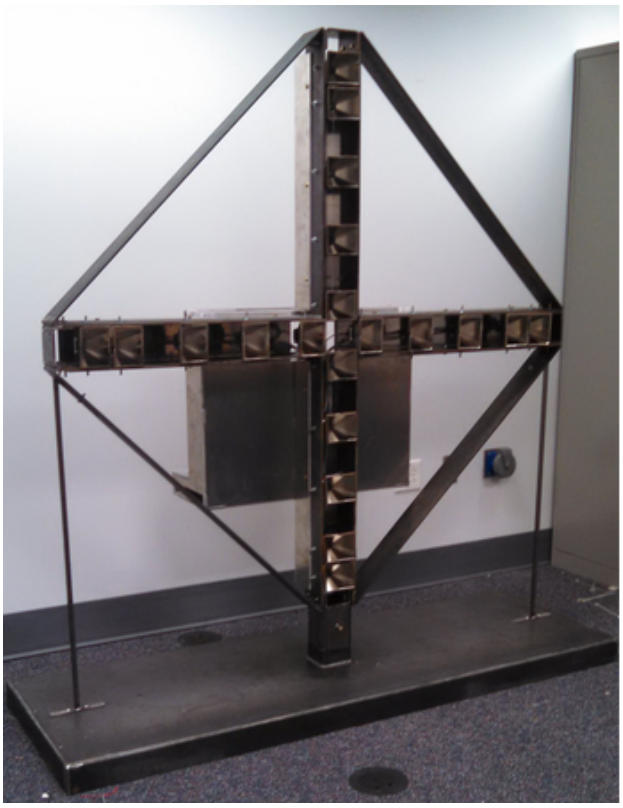


Figure 49: Finished Structure

5.6.2 Component Placement

The component placement had to be adjusted so the SP4T switch could be centralized on the component sheet. This made it easier for connecting the cables which ran to the transmit horn antennas. Below in Figure 50 shows the final component layout including the wires for powering and grounding.

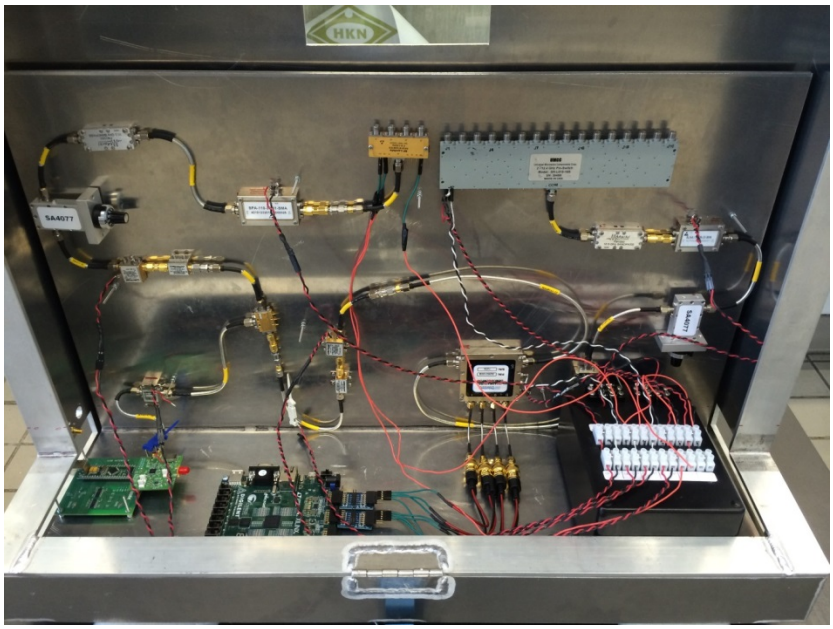


Figure 50: Finalized Component Placement

6 Schedule

6.1 Conceptual Design Review Fall 2014 Schedule

This section outlines the initial tentative schedule for the project that was originally created in November 2014. Most of the details of this initial schedule are for dates prior to December 15, 2014. Line items after that date are general descriptions of the tasks that needed to be done in general for the project without knowledge of the future Milestones the ECE, ME, and IE departments would require for completion. Several changes were made to the schedule including design changes, procurement delays pushing testing schedules back, re-scoping the project tasks, as well as input from the Northrop Grumman sponsor for task unforeseen.

There is a large gap in the schedule from December 2014 to January 8, 2015 due to the Winter Break and the school closing during that time. The schedule table highlights the tasks better than the Gantt chart view because the chart would be very comprehensive and hard to read. Instead the tasks list associated with the Gantt chart has been attached below. To see the Gantt Charts for both schedules refer to Appendix E.

Table 22: Previous Schedule from Conceptual Design Milestone #3

Task Name	Duration	Start	Finish	Resource Names
Prepare Milestone #3 - System-Level Design	**23 days**	**Wed 10/22/14**	**Fri 11/21/14**	
Frequency Justification	**6 days**	**Wed 10/22/14**	**Wed 10/29/14**	**Matthew Cammuse**
Antenna Design Concept	**8 days**	**Wed 10/22/14**	**Fri 10/31/14**	**Matthew Cammuse**
Aperture Simulation	8 days	Wed 10/22/14	Fri 10/31/14	Matthew Cammuse
Component Trade-Offs	8 days	Wed 10/22/14	Fri 10/31/14	Matthew Cammuse
Technical Trades	**5 days**	**Mon 10/27/14**	**Fri 10/31/14**	**ALL**
Identify Trades	2 days	Mon 10/27/14	Tue 10/28/14	ALL
Perform Trade-Off Analysis	3 days	Mon 10/27/14	Wed 10/29/14	ALL
Assess Project Risks & Issues	**2 days**	**Mon 10/27/14**	**Tue 10/28/14**	**Jasmine Vanderhorst, Benjamin Mock**
Outline Milestone #3 Report	2 days	Mon 10/27/14	Tue 10/28/14	ALL
Team Meeting - Status Update	**0 days**	**Tue 10/28/14**	**Tue 10/28/14**	**Jasmine Vanderhorst**
FPGA Programming Plan & Concept	**16 days**	**Wed 10/22/14**	**Wed 11/12/14**	**Patrick Delallana**
Signal Processing Code	16 days	Wed 10/22/14	Wed 11/12/14	Julia Kim, Patrick Delallana
Component Trade-offs	6 days	Wed 10/22/14	Wed 10/29/14	Patrick Delallana
Develop Contingency Plan	6 days	Wed 10/22/14	Wed 10/29/14	Patrick Delallana

Analog-To-Digital Converter Code	8 days	Wed 10/29/14	Fri 11/7/14	Patrick Delallana
Discrete Controls	8 days	Wed 10/29/14	Fri 11/7/14	Patrick Delallana
VGA Code	11 days	Wed 10/29/14	Wed 11/12/14	Patrick Delallana
Assess Project Risks & Issues	**2 days**	**Mon 11/3/14**	**Tue 11/4/14**	**Jasmine Vanderhorst, Benjamin Mock**
25% Completion of Milestone 3 Report	5 days	Tue 10/28/14	Mon 11/3/14	ALL
Team Meeting - Status Update	**0 days**	**Tue 11/4/14**	**Tue 11/4/14**	**Jasmine Vanderhorst**
Simulation: Timing/Synchronization	**8 days**	**Wed 10/22/14**	**Fri 10/31/14**	**Patrick Delallana**
Determine Components	5 days	Wed 10/22/14	Tue 10/28/14	Joshua Cushion
Determine Component Timing	3 days	Tue 10/28/14	Thu 10/30/14	Patrick Delallana
Generate Timing Diagram	2 days	Thu 10/30/14	Fri 10/31/14	Patrick Delallana
Finalize Component Budget	3 days	Wed 10/29/14	Fri 10/31/14	Benjamin Mock
Radar Range Equations	**6 days**	**Mon 11/3/14**	**Mon 11/10/14**	**Joshua Cushion**
Signal Calculation	6 days	Mon 11/3/14	Mon 11/10/14	Matthew Cammuse
Noise Calculation	6 days	Mon 11/3/14	Mon 11/10/14	Joshua Cushion
Transmit Path Concept	**6 days**	**Mon 11/3/14**	**Mon 11/10/14**	**Joshua Cushion**
Component Trade-Offs	4 days	Mon 11/3/14	Thu 11/6/14	Joshua Cushion
Perform Analysis	6 days	Mon 11/3/14	Mon 11/10/14	Joshua Cushion
Receive Path Concept	**6 days**	**Mon 11/3/14**	**Mon 11/10/14**	**Joshua Cushion**
Component Trade-Offs	4 days	Mon 11/3/14	Thu 11/6/14	Joshua Cushion
Perform Analysis	6 days	Mon 11/3/14	Mon 11/10/14	Joshua Cushion
Cabling Design Concept	**3 days**	**Thu 11/6/14**	**Mon 11/10/14**	**Patrick Delallana**
Component - Cable Type Selection	3 days	Thu 11/6/14	Mon 11/10/14	Patrick Delallana
Generate Interface Control Document (ICD)	**3 days**	**Mon 11/10/14**	**Wed 11/12/14**	**Patrick Delallana**
"From-To" Diagram - component parameters	3 days	Mon 11/10/14	Wed 11/12/14	Joshua Cushion, Patrick Delallana
Conceptual Mechanical Design	**8 days**	**Mon 11/3/14**	**Wed 11/12/14**	**Malcolm Harmon, Mark Poindexter**
Vendor - Part Ordering	6 days	Mon 11/3/14	Mon 11/10/14	Malcolm Harmon
Mechanical - Part	6 days	Mon 11/3/14	Mon 11/10/14	Mark Poindexter

Fabrication/Procure				
Material Trade Offs	3 days	Thu 11/6/14	Mon 11/10/14	Mark Poindexter
Material Stress/Strain, Deflection	3 days	Mon 11/10/14	Wed 11/12/14	Malcolm Harmon
Component Layout-Integrated Design	1 day	Wed 11/12/14	Wed 11/12/14	Malcolm Harmon
Assess Project Risks & Issues	2 days	Mon 11/10/14	Tue 11/11/14	Benjamin Mock, Jasmine Vanderhorst
50% Completion of Milestone #3 Report	6 days	Mon 11/3/14	Mon 11/10/14	ALL
Finalize Mechanical Design	**6 days**	**Thu 11/6/14**	**Thu 11/13/14**	**Malcolm Harmon, Mark Poindexter**
Create 2 Trihedral	2 days	Thu 11/6/14	Fri 11/7/14	Mark Poindexter
Create Antenna Frame	3 days	Mon 11/10/14	Wed 11/12/14	Mark Poindexter
Create Frame Wall Mount	3 days	Mon 11/10/14	Wed 11/12/14	Malcolm Harmon
Create Frame Ground Mount	3 days	Mon 11/10/14	Wed 11/12/14	Malcolm Harmon
Create Radar Absorbing Foam Frame	1 day	Wed 11/12/14	Wed 11/12/14	Malcolm Harmon
Detailed Description of Designs	**4 days**	**Mon 11/10/14**	**Thu 11/13/14**	**Mark Poindexter**
Description	3 days	Mon 11/10/14	Wed 11/12/14	Mark Poindexter
Purpose	3 days	Mon 11/10/14	Wed 11/12/14	Mark Poindexter
Trade-Offs	3 days	Tue 11/11/14	Thu 11/13/14	Malcolm Harmon
Power Budget Concept	**6 days**	**Thu 11/6/14**	**Thu 11/13/14**	**Julia Kim**
Voltage Requirements	3 days	Thu 11/6/14	Mon 11/10/14	Julia Kim
Wire and Current Capacity	3 days	Thu 11/6/14	Mon 11/10/14	Julia Kim
PCB Level Shifter	4 days	Mon 11/10/14	Thu 11/13/14	Julia Kim
Testing Concept	**4 days**	**Mon 11/10/14**	**Thu 11/13/14**	**Julia Kim**
Signal Processing Test	4 days	Mon 11/10/14	Thu 11/13/14	Julia Kim, Patrick Delallana
Subassembly Testing Concept	**4 days**	**Mon 11/10/14**	**Thu 11/13/14**	**Julia Kim, Matthew Cammuse**
Transmit Path	2 days	Mon 11/10/14	Tue 11/11/14	Julia Kim, Joshua Cushion
Receive Path	2 days	Mon 11/10/14	Tue 11/11/14	Joshua Cushion, Julia Kim
Full Transmit/Receive Path	2 days	Wed 11/12/14	Thu 11/13/14	Joshua Cushion, Julia Kim
System Calibration Concept	**4 days**	**Mon 11/10/14**	**Thu 11/13/14**	**Julia Kim, Matthew Cammuse**

Signal Processing Calibration	4 days	Mon 11/10/14	Thu 11/13/14	Julia Kim
Cabling Calibration - Physical Characteristics	4 days	Mon 11/10/14	Thu 11/13/14	Matthew Cammuse
Team Meeting - Status Update	**0 days**	**Tue 11/11/14**	**Tue 11/11/14**	**Jasmine Vanderhorst**
100% Completion of Milestone #3 Report	5 days	Mon 11/10/14	Fri 11/14/14	ALL
Team Meeting - Presentation Prep	**0 days**	**Tue 11/18/14**	**Tue 11/18/14**	**Jasmine Vanderhorst**
Milestone #3 System-Level Design Final Presentation Due	**0 days**	**Fri 11/21/14**	**Fri 11/21/14**	**ALL**
Procure Storage Facility	**15 days**	**Mon 11/17/14**	**Fri 12/5/14**	**Benjamin Mock**
Verify Vendor Authorization with University	**15 days**	**Mon 11/17/14**	**Fri 12/5/14**	**Benjamin Mock**
Component Ordering (50 parts)	**15 days**	**Tue 11/18/14**	**Mon 12/8/14**	**Benjamin Mock**
FPGA Board (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
VCO (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Power Amplifier (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Wideband Amplifier (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Antenna Horns (20 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Low Noise Amplifier (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Frequency Multiplier (2 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SPDT Switch (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SP4T Switch (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SP16T Switch (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Variable Attenuator (3 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Fixed Attenuators (12 units total)	**15 days**	**Tue 11/18/14**	**Mon 12/8/14**	**Benjamin Mock**
SA18H-07 (3 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SA18H-08 (3 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SA18H-09 (3 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
SA18H-10 (3 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
IQ Demodulator (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Analog-To-Digital Converter (2 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Band Pass Filter (2 units)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock
Isolator (1 unit)	15 days	Tue 11/18/14	Mon 12/8/14	Benjamin Mock

Thanksgiving Break	**3 days**	**Thu 11/27/14**	**Sun 11/30/14**	**ALL**
Christmas break	**17 days**	**Mon 12/15/14**	**Tue 1/6/15**	**ALL**
Spring: First Week of Class	**8 days**	**Wed 1/7/15**	**Fri 1/16/15**	**ALL**
System Assembly	**18 days**	**Wed 1/7/15**	**Fri 1/30/15**	**ALL**
Team Meetings - Spring Deliverables & Milestones	6 days	Thu 1/8/15	Thu 1/15/15	ALL
Verify All Components in Secure Storage	5 days	Mon 1/12/15	Fri 1/16/15	ALL
Connect FPGA Board, CPU, and Display	5 days	Mon 1/19/15	Fri 1/23/15	ALL
Construct Electrical Circuit	7 days	Mon 1/19/15	Tue 1/27/15	ALL
Attach Power Supply	3 days	Tue 1/27/15	Thu 1/29/15	ALL
Attach To Structural Supports	2 days	Thu 1/29/15	Fri 1/30/15	ALL
System Testing	**15 days**	**Mon 2/9/15**	**Fri 2/27/15**	**ALL**
Test FPGA Programs	5 days	Mon 2/9/15	Fri 2/13/15	ALL
Test Power Supply	5 days	Mon 2/9/15	Fri 2/13/15	ALL
Test Circuit Components	5 days	Mon 2/9/15	Fri 2/13/15	ALL
Analyze Connectivity	5 days	Mon 2/9/15	Fri 2/13/15	ALL
Record and Analyze Tests	11 days	Fri 2/13/15	Fri 2/27/15	ALL
Result Evaluation	**35 days**	**Mon 3/2/15**	**Fri 4/17/15**	**ALL**
Document Project Progress	5 days	Mon 3/2/15	Fri 3/6/15	ALL
Finalize Project	15 days	Mon 3/9/15	Fri 3/27/15	ALL
Finalize Report	11 days	Sat 3/28/15	Fri 4/10/15	ALL
Present Project Results	5 days	Mon 4/13/15	Fri 4/17/15	ALL
Final Exam Week	**5 days**	**Mon 4/27/15**	**Fri 5/1/15**	**ALL**
End of Year: Graduation	**0 days**	**Sat 5/2/15**	**Sat 5/2/15**	**ALL**

6.2 Spring 2015 Final Project Schedule

This section highlights all the updates that have been made to the tentative schedule this semester for the team. A comparison between these two schedules details where the discrepancies exist and what caused the major changes in the schedule. This section will also highlight the major milestones achieved throughout the duration of the project.

Table 23: Final Project Schedule - Spring 2015

Task Name	Duration	Start	Finish	Resource Names
Begin Spring Semester	0 days	Wed 1/7/15	Wed 1/7/15	**All**

Internal Team Meeting: 5pm	0 days	Mon 1/12/15	Mon 1/12/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/14/15	Wed 1/14/15	**Pete Stenger, All**
FPGA Programming	9 days	Thu 1/8/15	Tue 1/20/15	**Patrick De La llana**
Timing Diagrams	8 days	Thu 1/8/15	Mon 1/19/15	**Patrick De La llana**
Waveguide Adapter Selection	10 days	Mon 1/12/15	Fri 1/23/15	**Matthew Cammuse**
Obtain Testing & Storage Facility	15 days	Mon 1/12/15	Fri 1/30/15	**Benjamin Mock, Jasmine Vanderhorst**
Meet with CAPS Safety Coordinator: Michael Coleman	4 days	Mon 1/12/15	Thu 1/15/15	**Benjamin Mock, Jasmine Vanderhorst**
Complete Online Safety Training	7 days	Thu 1/15/15	Fri 1/23/15	**All**
Attend EHS Safety Class	1 day	Fri 1/30/15	Fri 1/30/15	**All**
Identify Problem Items	18 days	Mon 1/12/15	Wed 2/4/15	**Benjamin Mock**
Radar Absorbing Foam	11 days	Mon 1/12/15	Mon 1/26/15	**Matthew Cammuse**
DC Power Supplies	8 days	Mon 1/26/15	Wed 2/4/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 1/19/15	Mon 1/19/15	**Jasmine Vanderhorst**
Frame Design	13 days	Mon 1/19/15	Wed 2/4/15	**Malcolm Harmon, Mark Poindexter**
Stress Analysis	10 days	Mon 1/19/15	Fri 1/30/15	**Malcolm Harmon**
Material Justifications	10 days	Mon 1/19/15	Fri 1/30/15	**Malcolm Harmon**
Component Layout Schematic	5 days	Wed 1/28/15	Tue 2/3/15	**Mark Poindexter**
Obtain Preliminary Frame Welding Price Quote	3 days	Mon 2/2/15	Wed 2/4/15	**Mark Poindexter**
Component Ordering	13 days	Mon 1/19/15	Wed 2/4/15	**Benjamin Mock**
Update Budget	6 days	Mon 1/19/15	Mon 1/26/15	**Benjamin Mock**
Identify Component Risks	7 days	Mon 1/26/15	Tue 2/3/15	**Benjamin Mock**
Level Shift Circuit Design	12 days	Tue 1/20/15	Wed 2/4/15	**Joshua Cushion**
Programming Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La llana**
Discrete Code Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La llana**
7-Segment Display Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La llana**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/21/15	Wed 1/21/15	**Pete Stenger, All**
Ongoing Progress: Signal Processing	6 days	Wed 1/21/15	Wed 1/28/15	**Julia Kim**
Power Supply Design	4 days	Mon 1/26/15	Thu 1/29/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 1/26/15	Mon 1/26/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/28/15	Wed 1/28/15	**Pete Stenger, All**
Ongoing Progress: Signal Processing	6 days	Wed 1/28/15	Wed 2/4/15	**Julia Kim**
Develop Testing Plans	7 days	Wed 1/28/15	Thu 2/5/15	**Matthew Cammuse**
Individual Component Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	**Matthew Cammuse**
Subassembly Testing Strategy	7 days	Wed 1/28/15	Thu 2/5/15	**Matthew Cammuse**
System Integration Strategy	7 days	Wed 1/28/15	Thu 2/5/15	**Matthew Cammuse**

Gather Appropriate Safety Signage	6 days	Fri 1/30/15	Fri 2/6/15	**Benjamin Mock**
Anechoic Foam Layout	11 days	Fri 1/30/15	Fri 2/13/15	**Matthew Cammuse**
Shipping Arrangements	11 days	Fri 1/30/15	Fri 2/13/15	**Benjamin Mock**
RF Lambda Vendor Parts	6 days	Fri 1/30/15	Fri 2/6/15	**Benjamin Mock**
Marki: Bandpass Filter	6 days	Fri 1/30/15	Fri 2/6/15	**Benjamin Mock**
Fairview Vendor Parts	7 days	Fri 1/30/15	Mon 2/9/15	**Benjamin Mock**
Digikey Vendor Parts	9 days	Fri 1/30/15	Wed 2/11/15	**Benjamin Mock**
Minicircuits Vendor Parts	11 days	Fri 1/30/15	Fri 2/13/15	**Benjamin Mock**
Team Meeting & Preparation for VP of Northrop Grumman	1 day	Mon 2/9/15	Mon 2/9/15	**All**
Internal Team Meeting: 5pm	0 days	Mon 2/2/15	Mon 2/2/15	**Jasmine Vanderhorst**
Calibration Plan: Hardware & Software Compatibility	3 days	Mon 2/2/15	Wed 2/4/15	**Joshua Cushion**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/4/15	Wed 2/4/15	**Pete Stenger, All**
Team Members Submit Report Sections	0 days	Wed 2/4/15	Wed 2/4/15	**All**
Milestone 4 Report Due	0 days	Thu 2/5/15	Thu 2/5/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 2/4/15	Wed 2/11/15	**Julia Kim**
Data Storing Software for FPGA to PCU	12 days	Thu 2/5/15	Fri 2/20/15	**Matthew Cammuse, Patrick De La llana**
Finalize Frame Design	3 days	Tue 2/10/15	Thu 2/12/15	**Malcolm Harmon, Mark Poindexter**
GO/NO-GO Design Stopping Point	2 days	Tue 2/10/15	Wed 2/11/15	**Mark Poindexter, Malcolm Harmon, Pete Stenger**
Submit Final Design Welding Vendors	2 days	Wed 2/11/15	Thu 2/12/15	**Malcolm Harmon, Mark Poindexter, Pete Stenger**
Prepare Presentation	4 days	Mon 2/9/15	Thu 2/12/15	**Jasmine Vanderhorst**
Milestone 4: Detailed Design Review & Test Plan Presentation	5 days	Mon 2/9/15	Fri 2/13/15	**All**
Northrop Grumman VP Visit and Project Update	2 days	Tue 2/10/15	Wed 2/11/15	**Pete Stenger, All**
Programming & Testing	44 days	Mon 2/9/15	Thu 4/9/15	**Patrick De La llana**
Analog To Digital Conversion Code	11 days	Mon 2/9/15	Mon 2/23/15	**Patrick De La llana**
FPGA Code Simulation and Testing	15 days	Mon 2/16/15	Fri 3/6/15	**Patrick De La llana**
Subassembly Testing	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion, Matthew Cammuse**
Transmit Signal and Modulator LO Chain	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion, Matthew Cammuse**
Power Supply Board	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion, Matthew Cammuse**
Data Gathering, Analysis, and Reporting	35 days	Fri 2/20/15	Thu 4/9/15	**Julia Kim**

Miscellaneous Task	35 days	Fri 2/20/15	Thu 4/9/15	**Julia Kim**
Receive Signal Chain	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion, Matthew Cammuse**
Build Component Box and Attach to Frame	5 days	Mon 2/23/15	Fri 2/27/15	**Mark Poindexter**
Scheduled to Receive Completed Antenna Frame	0 days	Fri 3/6/15	Fri 3/6/15	**Malcolm Harmon**
Actual Structure Received	0 days	Fri 3/20/15	Fri 3/20/15	**Malcolm Harmon, Mark Poindexter**
Transmit and Modulator LO Chain Component Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Matthew Cammuse, Joshua Cushion**
Programming Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Patrick De La llana**
Ongoing Progress: Signal Processing	6 days	Wed 2/11/15	Wed 2/18/15	**Julia Kim**
Build Power Supply Board	3 days	Mon 2/16/15	Wed 2/18/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 2/16/15	Mon 2/16/15	**Jasmine Vanderhorst**
Ongoing Progress: Signal Processing	6 days	Wed 2/18/15	Wed 2/25/15	**Julia Kim**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/18/15	Wed 2/18/15	**All**
Software Demonstration	5 days	Mon 2/23/15	Fri 2/27/15	**Patrick De La llana**
Discrete Code Switch Display	2 days	Mon 2/23/15	Tue 2/24/15	**Patrick De La llana**
A-to-D Conversion Display	2 days	Tue 2/24/15	Wed 2/25/15	**Patrick De La llana**
Tentative: VGA Imaging Display	2 days	Thu 2/26/15	Fri 2/27/15	**Patrick De La llana**
Internal Team Meeting: 5pm	0 days	Mon 2/23/15	Mon 2/23/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/25/15	Wed 2/25/15	**All**
Milestone 5: Midterm Hardware/Software Reviews	5 days	Mon 2/23/15	Fri 2/27/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 2/25/15	Wed 3/4/15	**Julia Kim**
VGA Coding	29 days	Mon 3/2/15	Thu 4/9/15	**Patrick De La llana**
Ongoing Progress: Signal Processing	11 days	Wed 3/4/15	Wed 3/18/15	**Julia Kim**
Spring Break: No School	5 days	Mon 3/9/15	Fri 3/13/15	**All**
Internal Team Meeting: 5pm	0 days	Mon 3/16/15	Mon 3/16/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/18/15	Wed 3/18/15	**All**
DC Wire Harness	**13 days**	**Mon 3/16/15**	**Wed 4/1/15**	**Matthew Cammuse**
Design DC Wire Harness	8 days	Mon 3/16/15	Wed 3/25/15	**Matthew Cammuse**
Wire Design Support for Pre-Fab	8 days	Mon 3/16/15	Wed 3/25/15	**Julia Kim**
Build DC Wire Harness	6 days	Wed 3/25/15	Wed 4/1/15	**Malcolm Harmon, Mark Poindexter, Matthew Cammuse**
Received Fixed Structure From Metal Fabrications	**0 days**	**Mon 3/23/15**	**Mon 3/23/15**	**Malcolm Harmon, Mark Poindexter**
Internal Team Meeting: 5pm	0 days	Mon 3/23/15	Mon 3/23/15	**Jasmine Vanderhorst**

Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 3/25/15	Wed 3/25/15	**All**
Software Integration	29 days	Mon 3/2/15	Thu 4/9/15	**Patrick De La llana**
Integrate all codes with FPGA Board	22 days	Mon 3/2/15	Tue 3/31/15	**Patrick De La llana**
Troubleshooting	7 days	Wed 4/1/15	Thu 4/9/15	**Joshua Cushion, Julia Kim, Matthew Cammuse, Patrick De La llana**
Visit From Northrop Grumman Sponsor: Pete Stenger	3 days	Wed 4/1/15	Fri 4/3/15	**All**
Ongoing Progress: Signal Processing	6 days	Wed 3/18/15	Wed 3/25/15	**Julia Kim**
Hardware Integration	19 days	Mon 3/16/15	Thu 4/9/15	**Joshua Cushion, Julia Kim, Mark Poindexter, Matthew Cammuse, Patrick De La llana**
Soldering Components	15 days	Mon 3/16/15	Fri 4/3/15	**Matthew Cammuse, Patrick De La llana**
Install and Fasteners and Components	15 days	Mon 3/16/15	Fri 4/3/15	**Malcolm Harmon, Mark Poindexter**
Sync Hardware with Code	6 days	Wed 4/1/15	Wed 4/8/15	**Patrick De La llana, Joshua Cushion**
Troubleshooting	6 days	Wed 4/1/15	Wed 4/8/15	**Julia Kim, Matthew Cammuse**
Cabling	6 days	Thu 4/2/15	Thu 4/9/15	**Mark Poindexter**
Power Connection	4 days	Mon 4/6/15	Thu 4/9/15	**Matthew Cammuse, Julia Kim**
System Testing	3 days	Mon 4/6/15	Wed 4/8/15	**All**
Finalize Signal Processing	6 days	Wed 4/1/15	Wed 4/8/15	**Julia Kim**
Design Project Poster	5 days	Wed 4/1/15	Tue 4/7/15	**Jasmine Vanderhorst**
ECE Senior Design Demonstration	0 days	Wed 4/8/15	Wed 4/8/15	**All**
ECE Senior Design Fair	0 days	Thu 4/9/15	Thu 4/9/15	**All**
User Manual and Guide	9 days	Mon 4/6/15	Thu 4/16/15	**Mark Poindexter, Malcolm Harmon**
Electronic Procedural Guide	9 days	Mon 4/6/15	Thu 4/16/15	**Joshua Cushion**
Project Turnover & Lessons Learned	8 days	Mon 4/6/15	Wed 4/15/15	**Jasmine Vanderhorst, Benjamin Mock**
Milestone 7: Final Project Report	0 days	Fri 4/17/15	Fri 4/17/15	**All**
Prepare Presentation	4 days	Mon 4/13/15	Thu 4/16/15	**Jasmine Vanderhorst**
Milestone 7: Final Project Presentation	2 days	Tue 4/14/15	Thu 4/16/15	**All**

6.2.1 Initial versus Actual Schedule Major Changes

Compared to the initial schedule outlined previously, the Spring 2015 schedule has changed drastically. There was a shift in the schedule by about two months. Testing was supposed to start around late January to early February 2015, but did not actually begin until late February and lasted throughout March and April 2015. This shift is attributed to design and

specification requirement changes like material selection, size requirements, and additional components required, as well as learning of miscellaneous unknown parts needed for the project. To provide an example, the initial design called for a level shift circuit and two analog to digital converters but was later changed to have no level shift circuit and four analog to digital converters. Also, there was a delay in obtaining the VCO due to longer lead times but once the VCO arrived it did not meet the specifications for the passband Bandpass filter, it was too low. Once this issue was realized testing was on hold until the RF signal generator could be obtained from a rental company on 3/16. The mechanical structure was initially supposed to be completed in the Fall 2014 semester, but several design improvements were made via the sponsor's request and was not finalized until February 2015.

The mechanical structure was originally quoted at approximately $12,000 causing the mechanical engineers to reevaluate the vendor and scout other contracts for the job. The process of quoting the structure took longer time than expected which pushed the schedule. The goal date at this point was to have the structure completely welded and ready for use by 2/27 from a local fabrication shop called Metal Fabricators. They accepted the job, provided a quote, and the team received a promised finish date of 3/6. However, when the deadline approached, the shop had created our design but had made an error saying it needed to be reworked. This did not push the schedule too far out of date because the universities were closed from 3/9 to 3/13. To the team's disappointment, the structure was not only not ready for pick up on 3/16, but the quadrant panels were not to the design specifications and there were several issues with what Metal Fabricators deemed a final product. This incorrectly fabricated structure had to be reworked and this caused the schedule to shift past the critical path of other tasks needing to be complete. It was not until 3/20 that the structure was turned over to the team, and even at that point, still needed custom work to be done by the team's mechanical engineers to fix the issues. Ultimately, the structure was delayed from 2/27 to 3/20 for a total of 3 weeks. Having the structure assembled was needed to align the horns, attach the component box, and integrate the entire system and run test from 20 feet away. This 3 week delay pushed all of these task past their originally scheduled dates.

Another delay and change in the schedule came from a rare and expensive part that had an 11-13 week lead time between the manufacturer and the FAMU Foundation. The SP16T switch was not received until 3/27 even though it was ordered in mid-December 2014. The team's final demonstration for the project was slated for 4/8 so this component delivery delay put a strain on the testing and troubleshooting plans because the SP16T switch was needed to test the 16 receive channels.

Lastly, the FPGA board should have been ordered as soon as possible. The order was placed in October 2014 but the component was not actually received until January 2015. The primary issue was the complexity of the tasks, like signal processing and the logic behind the electronic components and then converting this information into a functioning VHDL Code. The VHDL code was needed for multiple tasks such as, complex multiplications for the I and Q data for the IQ Demodulator and signal processing concepts such as fast Fourier transforms to get the frequency composition of the signals. Due to the complexity of programming and the extensive research and practice that went into learning VHDL, simultaneously while working on the research aspect of SAR Theory, timing was an issue from the start. Had the FPGA board been ordered sooner, more time practicing and learning its functionality would have benefited the

team tremendously. This issue caused a lack in ability to test subsystems and the integrated system early and was pushed until late in the Spring Semester.

6.2.2 Project Milestones

Despite the many issues with theory complexity, subcontracted structural work, procurement issues, and design changes, there were several milestones successfully completed throughout the duration of the project, including completing a successful final demonstration of the entire system on the projected date of 4/8.

6.2.2.1 Fall 2014 Completed tasks:

1. Designed RF electrical system including:
    a. signal power levels
    b. component noise figures
    c. component noise temperatures

Dates Performed: Fall Semester 2014

2. Antenna design and analysis

Dates Performed: Fall Semester 2014

3. Mechanical structure design and analysis

Dates Performed: Fall Semester 2014

4. Performed component analysis and selected RF components capable of implementing the design.

Dates Performed: Fall Semester 2014

5. Procured components and test equipment.

Dates Performed: November 2014 – March 2015

6. Tested and verified signal power levels at output of each RF component in signal transmit chain using an RF detector.

Dates Performed: 2/17 – 3/6

Note: Used an RF detector because signal analyzer was not received until 3/16.

6.2.2.2 Spring 2015 Milestones:

1. Test and verify the following for the signal power levels and pulse quality for each of the following signal chains using the signal analyzer and high frequency signal generator:
    a. Transmit – completed 3/23
    b. LO IQ demodulator – completed 3/23
    c. Receive – completed 3/27

    Note: Signal analyzer and high frequency signal generator were not received until 3/16.

2. Integrate the FPGA with the RF components and test the software to control the timing of the switches:

a. SPDT and SP4T

Completion date: 3/25

b. SP16T (delivery date 3/27)

Completion date: 3/29

3. Verify that the analog to digital converters sample and convert the received RF pulses.

Completion date: 3/27

4. Verify that the IQ demodulator can successfully:
    a. Output the correct voltages for both the phase and amplitude (I and Q channels) of the received RF signal.

Expected completion date: 3/31

5. Assemble mechanical structure

Completion date: 4/1

Note: Scheduled Northrop Grumman sponsor visit 4/1 – 4/3

6. Verify FPGA code using I/O for the following functions:
    a. A/D conversion of IQ demodulator outputs: (I,I',Q,Q')

Completion date: 4/1

7. Transmit an RF pulse with the correct amplitude (power) and frequency from a single antenna, verify the signal power at 20 feet using field strength meter.

Completion date: 4/2

8. Verify that a single antenna on the receive chain can detect a returned pulse from the transmit chain.

Completion date: 4/2

9. Integrate electrical system:
    c. 4 transmit antennas
    d. 16 receive antennas
    e. Component box
        i. RF components
        ii. FPGA
        iii. Power supply wiring, connectors, etc.

Completion date: 4/3

10. Test and calibrate entire SAR system including:
    a. 4 transmit antennas
    b. 16 receive antennas
    c. Signal processing
        i. Generate scene extent data using excel program

Completion dates: 4/3-4/9

11. Final Hardware demonstration of the Transmit, Receive, and IQ Demodulator LO chains along with power system, and programming complete.

Completion date: 4/9

7 Final Budget and Justification

7.1 Initial Budget Estimate

Northrop Grumman granted the FAMU-FSU College of Engineering $50,000.00 to sponsor the project through the Department of Electrical and Computer Engineering. The team developed a living budget that could accommodate any necessary changes to the schedule or scope without running the risk of depleting the allotted allocation. The initial projection is noted in Figure 51 as a pie chart. The Electrical Components comprised 51% of the entire budget while a Remainder of 37% existed for necessary changes. The remaining $19,000.00 was more than sufficient to satisfy the safety buffer of $12,000.00 that the team originally decided upon at the beginning of this project. Table 24 indicates the layout of expense for the SAR Imager as was initially laid out.

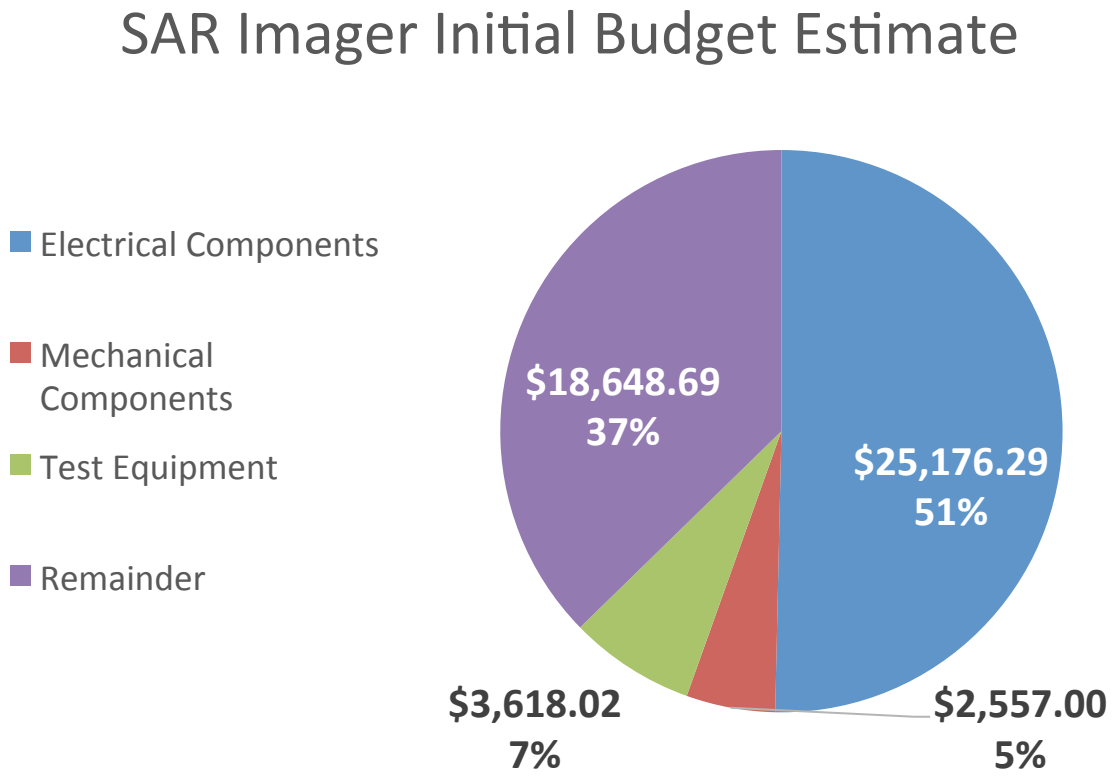


Figure 51 SAR Imager Initial Budget Allocation

Table 24 SAR Imager Initial Expense Report

Component	Product Number	Quantity	Unit Price	Total Price
Power Amplifier	SPA-110-30-01-SMA	1	1930.72	1930.72
Low Noise Amplifier	SLNA-120-38-22-SMA	1	1361.4	1361.4
Variable Attenuator	SA4077	3	580.84	1742.53
Fixed Attenuator	SA18H-07	3	44.55	133.65
Fixed Attenuator	SA18H-08	3	44.55	133.65
Fixed Attenuator	SA18H-08	3	44.55	133.65
Fixed Attenuator	SA18H-09	3	44.55	133.65
Fixed Attenuator	SA18H-10	3	44.55	133.65
Fixed Attenuator	SA18H-03	3	44.55	133.65
Band Pass Filter	SA18H-06	3	240	480
FPGA Board	Nexys 3	2	189	378
ADC	410-064P-KIT	2	37	74
Pmod Test Point Header	410-135P	3	16	48
Antenna Horns	MA86551	25	22.5	562.5
VCO Kit	126489-HMC820LP6CE	1	327.98	327.98
SPDT	HMC-C058	1	2482.01	2482.01
SP4T	RFSPaTA0812G	1	1725	1725
SP16T	UMC SR-L010-16S	1	4009	4009
Wideband Amplifier	ZVA-183-S+	1	895	895
Waveguide Adapters	90-422	22	175	3740
50 Ohm Loads (Male)	ST1819	15	16.66	249.9
50 Ohm Loads (Female)	ST1825F	5	22.64	113.2
SMA Connector M-M	ACX1240-ND	5	6.13	30.65
SMA Connector F-M	ACX1246-ND	5	7.07	35.35
SMA Connector F-F	ACX1242-ND	5	5.23	26.15
SMA-BNC Adap. M-M	501-1341-ND	5	12.67	63.35
SMA-BNC Adap. M-F	501-1141-ND	5	10.51	52.55
SMA-BNC Adap. F-M	501-1140-ND	5	10.51	52.55
SMA-BNC Adap. F-F	501-1338-ND	5	9.99	49.95
48” RF Cables	SCA49141-48	3	6.13	44.1
36” RF Cables	SCA49141-36	25	7.07	339
12” RF Cables	SCA49141-12	3	5.23	37.8
7” RF Cables	SCA49141-07	5	12.67	63
5” RF Cables	SCA49141-05	10	10.51	126
3” RF Cables	SCA49141-03	10	10.51	126

Ultra Wideband Amplifier	ZX60-14012L+	3	179.95	539.85
Frequency Amplifier	ZX90-2-50-S+	2	41.95	83.9
Low Noise Amplifier	SLNA-180-38-25-SMA	1	1205	1205
Anechoic Absorber		25	50	1250
Mechanical Frame	N/A	1	12678	2557
Field Strength Meter		1	129.95	129.95
RF Detector	A409	1	500	500
Signal Generator	AT-N5183B	1	1302.02	1302.02
Signal Analyzer	AT-N9030A	1	1816	1816
			Total Cost	31351.31
			Savings	18648.69

7.2 Actual Budget Allocation

Figure 52 below indicates the budget utilization in a pie chart for the total sponsored amount of $50,000.00. The project $12,000.00 of unspent resource was eventually allocated to cover the cost of additional spare components and miscellaneous mechanical frame hardware. Also, the cost for rental equipment doubled from the initial projection as the rental contract needed to be extended a month for proper demonstration. The cost for the structure and its components remained relatively static, but instances where items from Home Depot or Fastenal were needed inflated the price noted between Figures 48 and 49.

Table 25 below indicates the final bill of materials and budget as allocated through the FAMU Foundation. This table indicates and does not discriminate between ordered spare electrical components, but noticing the increased quantity of parts between Table 23 and Table 24 should highlight the final adjustments made. Spare parts were initially integrated into the ordering plan for the team but discretion was made to save the safety buffer should something occur. For example, the team considered creating an Anechoic Absorbing chamber with this, but the smallest possible chamber that could be built to meet the specifications as demanded would cost in excess of $7,000.00. This item was eventually reevaluated and restructured multiple times but eventually was never ordered so that the future team could devise a better strategy to construct a more optimal operating environment.

The remaining amount of $7,472.06 was intended for the procurement of repaired or duplicate parts in the extreme case that during final testing and integration that all components were destroyed. It is suggested to future teams that this type of allocation remain within the budget, but also to ensure that each component is operational as soon as possible to pre-allocate the funds necessary to repair or replace them. Items that should be purchased immediately following team formation include the: SP16T, SP4T, SPDT, VCO Eval Board, ADC (x3), and each Amplifier.

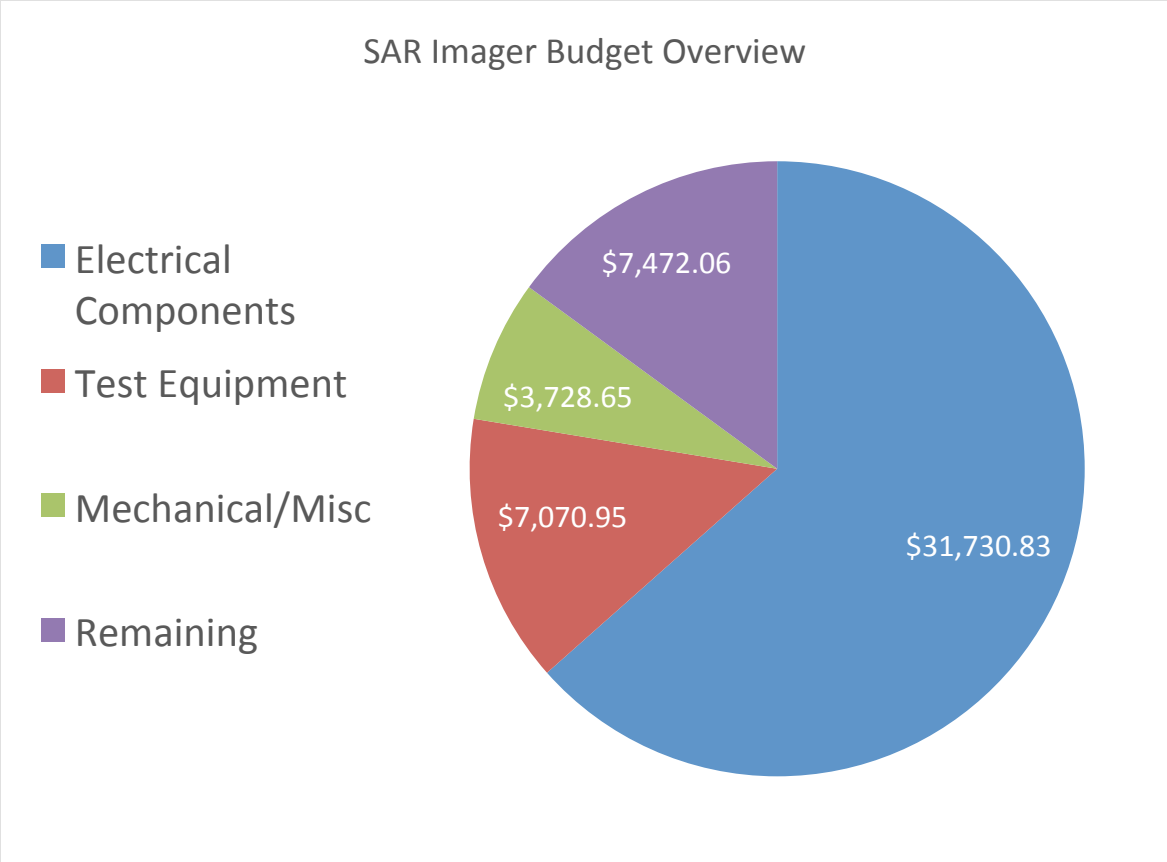


Figure 52: $50,000 Budget Allocation Summary

Table 25: Bill of Materials by Vendor

Distributor	Product	P/N	Unit Price	Quantity	Invoice
Fairview Microwave	Power Amplifier 1	SPA-110-30-01-SMA	$1,930.72	1	$ 1,930.72
	Power Amplifier 2	SPA-110-30-01-SMA	$2,145.24	1	$ 2,145.24
	Low Noise Amplifier 1	SLNA-120-38-22-SMA	$1,361.40	1	$ 1,361.40
	Low Noise Amplifier 2	SLNA-180-38-25-SMA	$1,205.00	1	$ 1,205.00
	Low Noise Amplifier 3	SLNA-120-38-22-SMA	$1,512.67	1	$ 1,512.67
	Variable Attenuator	SA4077	$580.84	3	$ 1,742.52
	Fixed Attenuator	SA18H-03	$44.55	3	$ 133.65
	Fixed Attenuator	SA18H-06	$44.55	3	$ 133.65
	Fixed Attenuator	SA18H-07	$44.55	3	$ 133.65
	Fixed Attenuator	SA18H-08	$44.55	3	$ 133.65
	Fixed Attenuator	SA18H-09	$44.55	3	$ 133.65
	Fixed Attenuator	SA18H-10	$44.55	3	$ 133.65
	50 Ohm Load (male)	ST1819	$16.66	15	$ 249.90
	50 Ohm Load (female)	ST1825F	$22.64	5	$ 113.20
	RF Cable 48"	SCA49141-48	$14.70	3	$ 44.10

	RF Cable 36"	SCA49141-36	$13.56	25	$ 339.00
	RF Cable 12"	SCA49141-12	$12.60	3	$ 37.80
	RF Cable 7"	SCA49141-07	$12.60	5	$ 63.00
	RF Cable 5"	SCA49141-05	$12.60	10	$ 126.00
	RF Cable 3"	SCA49141-03	$12.60	10	$ 126.00
Digi-Key	VCO Eval Board	129468-HMC820LP6CE	$327.98	1	$ 327.98
	VCO Eval Board	129468-HMC820LP6CE	$327.98	1	$ 327.98
	SPDT	HMC-C058	$2,482.01	1	$ 2,482.01
	SMA m-m	ACX1240-ND	$6.13	5	$ 30.65
	SMA f-m	ACX1246-ND	$7.07	5	$ 35.35
	SMA f-f	ACX1242-ND	$5.23	5	$ 26.15
	SMA - BNC m-m	501-1341-ND	$12.67	5	$ 63.35
	SMA - BNC m-f	501-1141-ND	$10.51	5	$ 52.55
	SMA - BNC f-m	501-1140-ND	$10.51	5	$ 52.55
	SMA - BNC f-f	501-1338-ND	$9.99	5	$ 49.95
	SMA - BNC m-f	501-1141-ND	$10.51	2	$ 21.02
	SMA - BNC f-m	501-1140-ND	$10.51	2	$ 21.02
	SMA - BNC f-f	501-1338-ND	$9.99	2	$ 19.98
	BNC Female Pomona Lead	501-1030-ND	$8.55	7	$ 59.85
	SMA m-m	ACX1240-ND	$6.13	4	$ 24.52
	SMA f-m	ACX1246-ND	$7.07	2	$ 14.14
	SMA f-f	ACX1242-ND	$5.23	5	$ 26.15
	SMA - BNC m-m	501-1341-ND	$12.67	3	$ 38.01
Digilent	FPGA Board	Nexys 3	$189.00	2	$ 378.00
	ADC	410-064P-KIT	$37.00	2	$ 74.00
	Pmod Test Point Header	410-135P	$16.00	3	$ 48.00
	1 Pin MTE Cable	240-005P	$4.99	5	$ 24.95
	VHDCI	164-433P	$9.49	2	$ 18.98
	Standoffs	240-020P	$1.49	5	$ 7.45
Advanced Receiver	Antenna Horns	MA86551	$22.50	25	$ 562.50
Marki Microwave	Band Pass Filter	FB-1050	$240.00	2	$ 480.00
RF Lambda	SP4T	RFSP4TA0812G	$1,725.00	1	$ 1,725.00
UMCC	SP16T	UMC SR-L010-16S	$4,009.00	1	$ 4,009.00
Minicircuits	Wideband Amplifier 1	ZVA-183-S+	$895.00	1	$ 895.00
	Wideband Amplifier 2	ZVA-183-S+	$895.00	1	$ 895.00
	Ultra Wideband	ZX60-14012L+	$179.95	3	$ 539.85

	Amplifier				
	Frequency Multiplier 1	ZX90-2-50-S+	$41.95	2	$ 83.90
	Frequency Multiplier 2	ZX90-2-50-S+	$895.00	1	$ 895.00
Metal Fabrication	Frame	N/A	$2,557.00	1	$ 2,557.00
ARRA	Waveguide Adapters	90-462	$170.00	22	$ 3,740.00
RA Mayes	Anechoic Absorber	C-RAM FAC 3.0	$47.00	15	$ 705.00
Less EMF	Field Strength Meter	EM2	$129.95	1	$ 129.95
Electro Rent	Signal Generator	KT-N5183B-520	$1,302.00	2	$ 2,604.00
	Spectrum Analyzer	KT-N9030A-513	$1,816.00	2	$ 3,632.00
Home Depot	Hex Bolt 1/4" (bag of 2)	85638	$0.61	22	$ 13.42
	Hex Nut 1/4"	96808	$0.60	28	$ 16.80
	Washers 1/4" (bag of 4)	2028	$0.98	7	$ 6.86
	Laser	40-0915	$19.97	2	$ 39.94
	Vary Zip Ties	50725	$16.99	1	$ 16.99
	Corner Brace (pack of 4)	13542	$1.97	1	$ 1.97
	3"x10ft PVC Pipe	1727	$6.22	1	$ 6.22
	Acrylic Sheet	1S08104A	$3.19	2	$ 6.39
	Aluminum Sheet Metal	56064	$10.62	1	$ 10.62
RadioShack	25 pin D Connector	276-1547	$2.49	1	$ 2.49
Polyphase Microwave	IQ Demodulator 1	AD60100B	$1,225.00	1	$ 1,225.00
	IQ Demodulator 2	AD60100B	$1,225.00	1	$ 1,225.00
Ground Shipping			$12.50	12	$ 150.00
Overnight Shipping			$35.00	4	$ 140.00
Equipment Shipping			$95.00	2	$ 190.00
		Total Budget			$ 50,000.00
		Total Spent			$ 42,527.94
		Remaining Budget			$ 7,472.06

8 Lessons Learned

8.1 General Engineering Lessons

The interdisciplinary, eight member team responsible for the development of the SAR Imager gained experience in and developed skills pertaining to the following areas:

- Task delegation and committee formation strategies for accomplishing tasks associated with long projects and ambitious goals.
- Establishing evaluation and gate review check points throughout the lifetime of a project to ensure that deliverables are being met and work is being accomplished in a timely and effective fashion.
- Settling disputes amongst team members' ideas in a professional manner.
- Communicating in a manner that is both effective and succinct in translating the ideas of each team member.
- The team learned how to value trust within each other to ensure that the project was completed successfully.
- Patience is often the better method when waiting on work to be completed while also checking up along the way to ensure that the given task is being completed via the schedule.
- Given that the team comprised eight individuals across three separate engineering departments it was a frustrating but worthwhile experience in working together to accomplish the long list of goals. (Conclusion of this section)

8.2 Electrical Engineering Lessons

The Electrical Engineering team found a greater understanding in the following areas due to their efforts exerted in the completion of this project:

- Development of effective hardware and software testing plans and strategies.
- Calculating noise figure, temperature, power gain and loss in communication systems.
- Soldering active electrical components and ensuring that one utilizes the appropriate equipment relative to the parts that need to be soldered.
- Developed skill in OrCAD Capture and PSpice Simulation software.
- Deconstructing fast Fourier transformations for utilization in VHDL coding language.
- Proficiency in VHDL was improved.
- Translating incoming signals for formation of an image on a VGA display.
- Understanding the basic theory behind Radio Frequency Engineering.
- Gained knowledge in the design and variation of Anechoic Absorber Chambers.
- Operational skill with a high frequency Signal Generator and a Spectrum Analyzer increased.
- Understanding of radar theory increased, especially concerning the design and use of array factors, element factors, grading and main beam lobes, phase centers, and signal and signal chain processing.

8.3 Mechanical Engineering Lessons

The Mechanical Engineering team found a greater understanding in the following areas due to their efforts exerted in the completion of this project:

- Applying knowledge of thermal analysis to evaluate the placement of electrical components.
- Learned how to negotiate contracts concerning metal fabrication, specifically cost and quality analysis between viable vendors.
- Developed conflict resolution skills when dealing with vendors concerning breach of contract matters.

8.4 Industrial Engineering Lessons

The Industrial Engineering team found a greater understanding in the following areas due to their efforts exerted in the completion of this project:

- Developed an increased understanding of utilizing a convoluted Gantt chart.
- Strengthened skills in technical writing and standardizing report formatting.
- Developed greater proficiency in website design.
- Enhanced effective communication skills concerning the transfer of knowledge between team members and stake holders.
- Enhanced budget management skills.
- Learned how to request and adjust quotations from vendors and perform an analysis of all options within the constraints of the project time line.
- Integrated all factors concerned with components ordering into the Gantt chart to ensure the lead time issues would cooperate with the time line of events.
- Learned the value of establishing a thorough agenda before every team and committee meeting.

9 Future Recommendations

9.1 General Engineering Recommendations

The interdisciplinary, eight member team responsible for the development of the SAR Imager recommend that any future team continuing this project adhere to and accomplish the following:

- Establish a mission statement/vision statement for each team so that members can establish shared values and use them to encourage each other to keep up good work.
- Utilize Gate Reviews within the project time-line to ensure that the project deliverables are completed at least two days before the due date. This will ensure proper time to prepare for any necessary demonstration or presentation.
- Establish all deliverables and requirements for each involved discipline so that these items can be integrated within the Gantt chart.
- Develop a system to keep team members accountable for their actions and inactions and clearly define every responsibility for each team member for every milestone.

9.2 Electrical Engineering Recommendations

The Electrical Engineering team recommends that any future team continuing this project adhere to and accomplish the following:

- Develop a good understanding of digital communications concepts, specifically noise temperature, noise figure, and power gain and loss.
- Become familiar with the operating principles behind the following pieces of test equipment: multimeters, voltmeters, signal generators, spectrum analyzers, and oscilloscopes.
- Learn how to write trigonometric functions in VHDL coding language.
- Ensure that each component that the team wishes to purchase has the correct specifications as noted on the data sheets supplied by the manufacturer. If the data is not present, contact the manufacturer directly.
- Ensure that all parts are stored neatly and in an organized manner so that one can easily determine what each item is and where and how it should be stored.
- Develop an appropriate wiring system in parallel to the design of the entire system.

9.3 Mechanical Engineering Recommendations

The Mechanical Engineering team recommends that any future team continuing this project adhere to and accomplish the following:

- Improve the rigidity of the frame.
- Reevaluate the current method on how to align the antenna horns.
- Consider adding wheels to the frame for ease of transportation.
- Redesign the frame with the purpose of maintaining its structure but reducing unnecessary parts. Reevaluate design through the lens of DFMA.

9.4 Industrial Engineering Recommendations

The Industrial Engineering team recommends that any future team continuing this project adhere to and accomplish the following:

- Formalize a procurement procedure for other members to submit requests to the procurement engineer which establishes a more transparent method at communicating order statuses on parts.
- Define each item's technical and schedule requirements to ensure that the best option is selected, these items include: lead time, shipping availability, importance on the testing schedule.
- Create a positive relationship with Donna Butka so ordering parts will seem like less of a hassle.
- Reevaluate the entire system design to ensure electrical reliability is achieved. (Suggested advisor: Mr. John Taylor)
- Reevaluate the entire system to ensure that DFMA is accomplished successfully and that the system is constructed from the vantage point of Design for Repair and Assembly. (Suggested Advisor: Dr. Tarik Dickens)

- Always request the shipping availability and pricings when requesting a quote from vendors.
- Follow the outline for ordering parts as detailed in Appendix D.
- Order spare parts for all active electrical components regardless of cost as long as the necessary parts have been designed for.
- Send a request for a quote from a vendor as immediate as a team request has been submitted.
- Establish a checks and balances system between the team members and committees to ensure that information is communicated effectively and that tasks are completed in a timely manner.

10 Conclusion

The initial goals of the project were to design and assemble an SAR Imager in order to detect a metal object at a distance of twenty feet and to form an image of the location of the object. However, after much planning and work, the team sponsor wanted the team to incrementally achieve small milestones that would lead closer to the end goals. First, the theoretical implementations of the system were determined, such as finding the noise figure and temperature and power gain and loss for each of the component of the electrical system and working on the antenna design and spacing as well as the mechanical structure. After the components were received, the transmit and receive chains were tested in order to determine if it worked as determined theoretically. In parallel, the code to transmit and receive the required 20 ns pulses and the A/D conversion was worked on, as well as the theoretical calculations for signal processing. Some design changes were made as needed with some of the components with the sponsor's approvals.

The antenna horns were put together in the structure and the electrical components were placed in the component box in order to realize the integrated testing. The RF signal generator was used to transmit the signal from one antenna horn and a second antenna horn was placed at a distance of twenty feet in order to determine whether a signal was actually being transmitted using the spectrum analyzer. Once those tests were accomplished, the next milestone was to test whether the signal transmitted was received back. A trihedral corner reflector was held at the specified distance of twenty feet, and the signal was transmitted. To verify whether the signal was being received back, the voltages coming in from the IQ demodulator were analyzed to see if there were any changes when the reflector was moved. The obtained results were not exact as there was no foam absorber in the surrounding area. These milestones were accomplished to meet the sponsor's expectations as the system was working as designed. He determined that further testing of the whole system with the four transmit and sixteen receive antennas could be realized in the future if the project is continued, as well as actually forming the image using the signal processing calculations that have already been accomplished.

11 Works Cited

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12 Appendix A – User's Guide

FAMU-FSU College of Engineering
Department of Electrical and Computer Engineering
Department of Industrial and Manufacturing Engineering
Department of Mechanical Engineering

User-Assembly & Operations Manual

EEL4911C – ECE Senior Design Project II

Multi-Static Synthetic Active Array Radar Aperture (SAR) Imager

Team #: E11 – M27

Student Team Members:

- **Matthew Cammuse**, Electrical Engineering (Email: mgc11@my.fsu.edu)
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- **Benjamin Mock**, Industrial Engineering (Email: bam11g@my.fsu.edu)
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Project Sponsor:

Pete Stenger

Contents

12.1 Introduction

This report will mention generally safety concerns that relate to the use and assembly of the SAR Imager as well as the necessary software installation. This report, for sake of clarity and succinctness, will not repeat the electronic assembly and troubleshooting as defined in Appendix B – Complete Test Reports. The Assembly Instructions will assume that the user has not seen the structure before and will therefore present pictorial evidence of the structures defined in the operations listed.

12.2 Safety Information

Despite the fact that the SAR Imager was designed for the use of human operators, there still exists a possibility that the components and assemblies associated with this structure can cause harm, permanent injury, or even death to those who improperly utilize them. The team has attempted to clearly define all procedures, risks, and concerns associated with the assembly, use, and repair of the SAR Imager.

12.2.1 Mechanical Safety

The weight of the entire steel structure exceeds 350 lbs. therefore it is important that at least two able-bodied people whom can lift over 175 lbs. are present during the structures movement and assembly. Failure to properly lift and assemble the structure as clearly defined below can result in damage to the frame, permanent injury, or even death.

12.2.2 Electrical Safety

The use of electrical systems always presents the hazard of electricity. By utilizing a proper power structure and wearing appropriate personal protective gear any user will significantly decrease their risk of electric shock. Additionally, handling each electrical component with care and ensuring that direct and close contact with these items is limited that user will prevent the risk of destroying these devises through electrostatic discharge. The microwave radiation emitted by the radar is calibrated at a safe density according the General OSHA guidelines as indicated in 1910.97

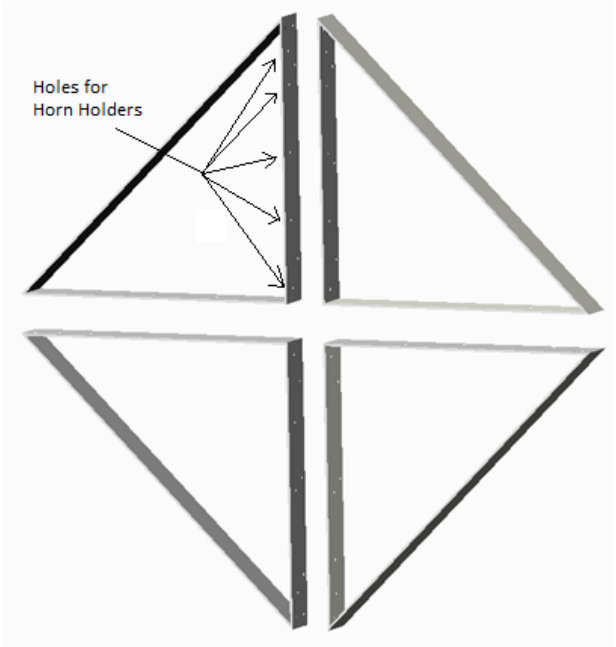
12.3 List of Components

- 1 Steel Structure Stand Base
- 3 C-Connectors
- 1 Extended Base C-Connector
- 4 Triangular Quadrant Panels
- 4 Aluminum Horn Cover Panels
- 40 Horn Holding Apparatus Halves
- 2 Support Poles
- 20 Pyramidal Horn Antennas
- 20 46” SMA Male Connectors
- 20 Blue Powder Coated Waveguide Adapters
    - 80 M6 Bolts
    - 80 M6 Nuts
- 52 ½” Grade 8 Bolts
- 116 ½” Nuts

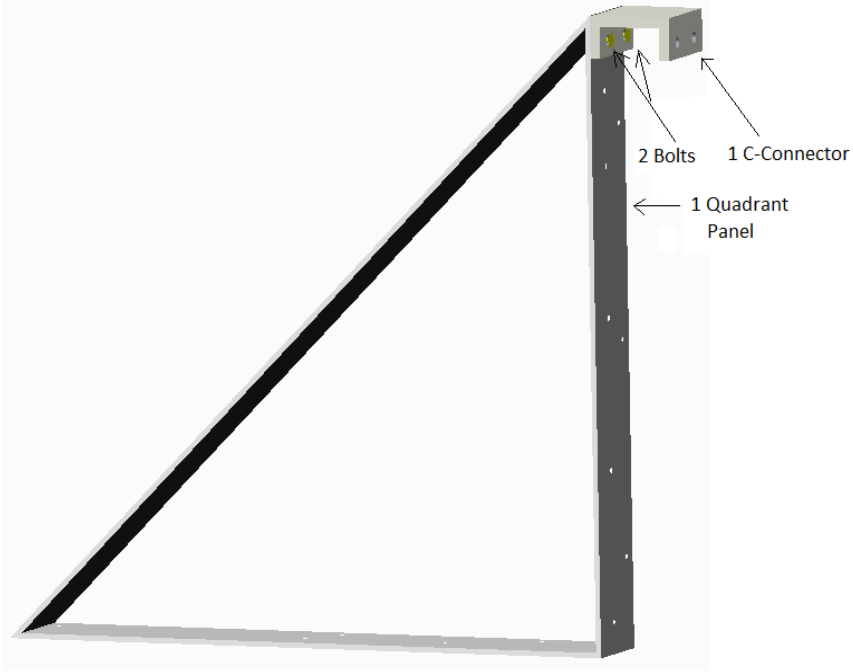
- Component Box
  - 1 Field Programmable Gate Array (FPGA) Evaluation Board
  - 4 Transmit Antennas
  - 16 Receive Antennas
  - 1 Voltage Controlled Oscillator (VCO) Evaluation Board
  - 1 IQ Demodulator
  - 1Single Pole Double Throw (SPDT) Switch
  - 1Single Pole Four Throw (SP4T) Switch
  - 1Single Pole Sixteen Throw (SP16T) Switch
  - 2 Frequency Multipliers
  - 2 Low Noise Amplifiers (LNA)
  - 1 Super Ultra Wideband Amplifier
  - 2 Ultra Wide Bandwidth Amplifiers
  - 3 Fixed Attenuators
  - 2 Variable Attenuators
  - 1 Power Amplifier
  - 2 Band Pass Filters (BPF)
  - 4 Analog-to-Digital Converters
  - 1 Power Supply Board
- 1 Computer
- 1 VGA Display

12.4 Assembly

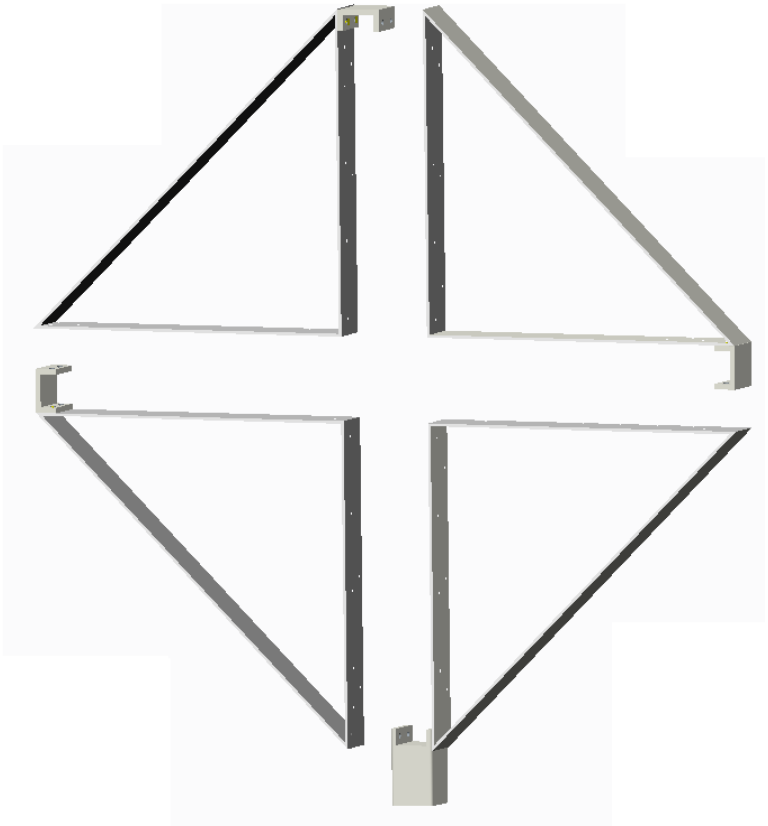
1. Ensure all components listed are available.
2. Lay the 4 Quadrant Panels on the ground making sure the holes for the Horn Holders are furthest from the ground as possible.



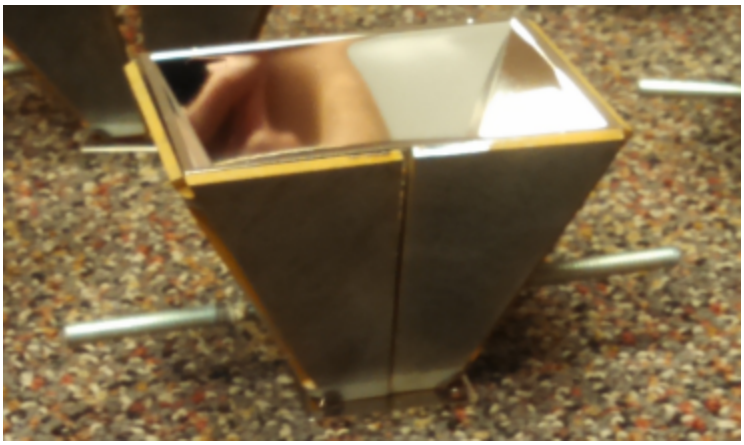
3. Connect 1 C-Connector to 1 Quadrant Panel with 2 1/2 Grade 8 Bolts and repeat 2 more times.



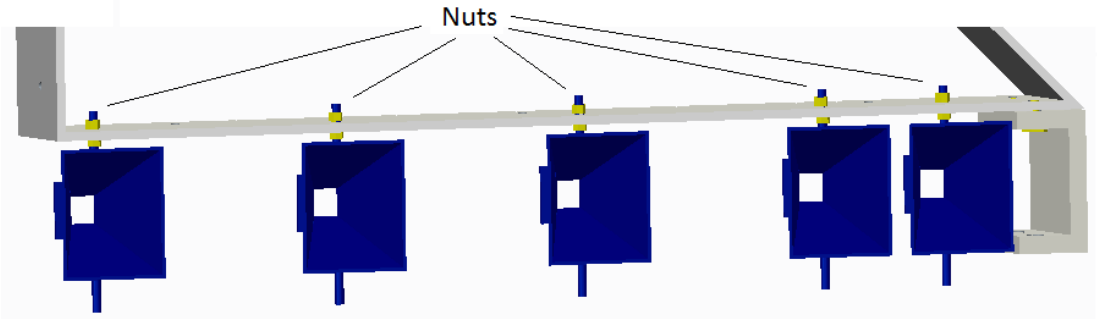
4. Connect Structure to Stand C-Connector to the last Quadrant Panel.

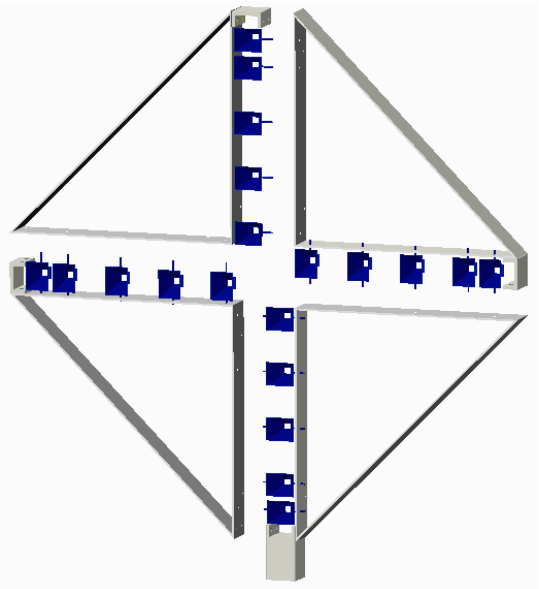


5. Slide 2 Horn Holders over 1 Horn Antenna; repeat 19 more times.

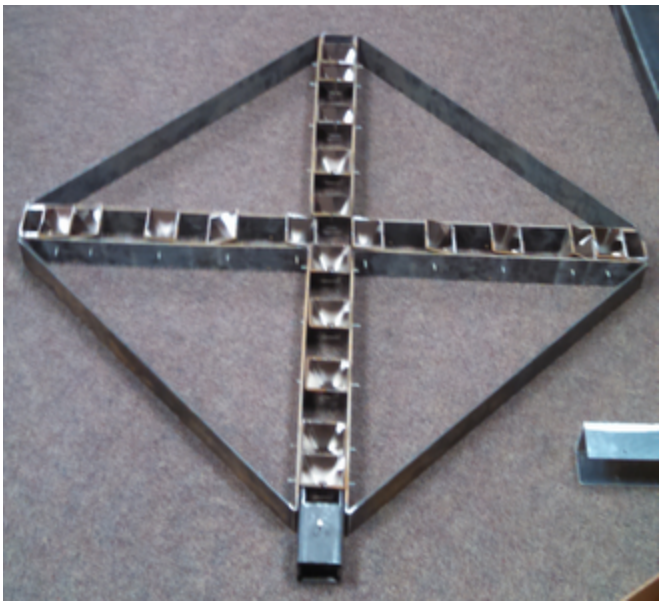


6. Screw 1 nut onto each Horn Holder's threaded rod.
7. Insert threaded rod into the hole for the Horn Holder and place nut for compression facing the Horn Antenna up. Repeat 19 more times.

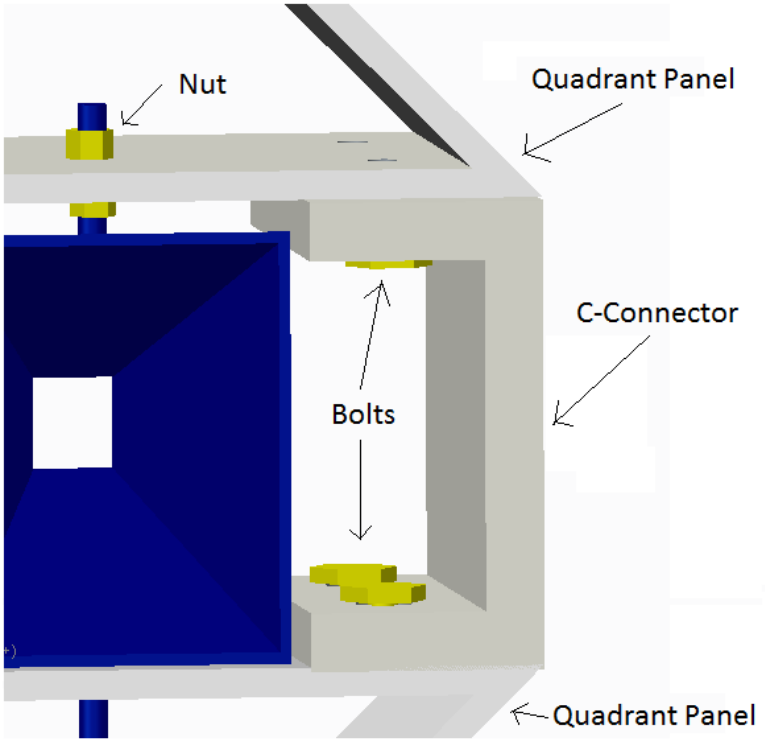




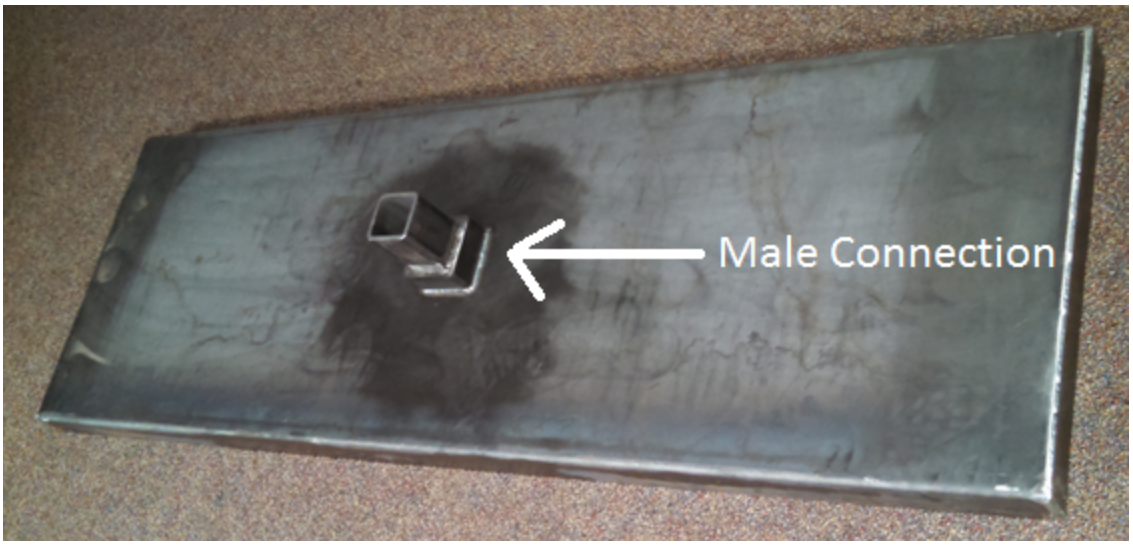
8. Combine all 4 Quadrant Panels together by sliding the open end of Horn Holders threaded rod into the adjacent Quadrant Panel
9. Put nuts on the 20 remaining threaded rods on Horn Holders.



10. Attach bolts to remaining holes of Quadrant Panel and C-Connectors and make sure all 16 bolts are securely tightened.

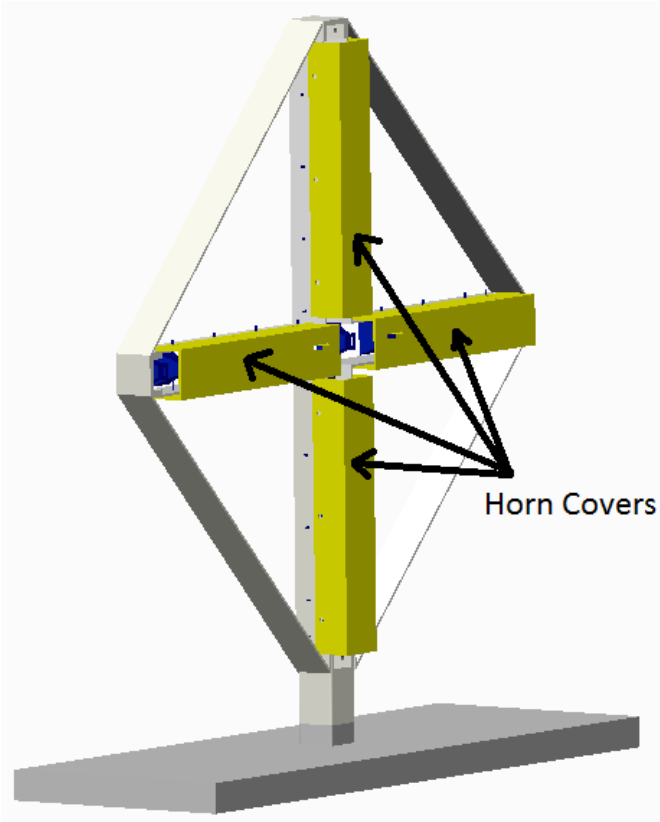


11. Place Stand in the appropriate location

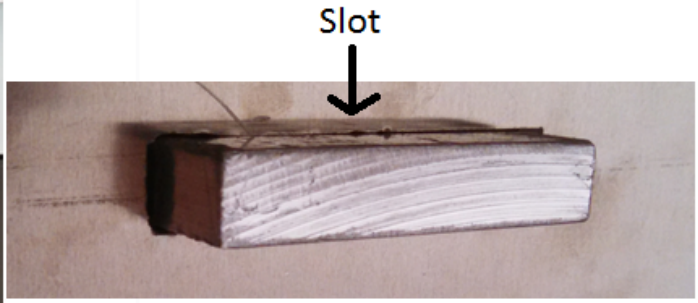


12. Have at least 2 people lift on opposite ends of the Stand to Structure C-Connector to set partially assembled structure upright.
13. Carefully lift the structure with 1 person on each end of the partially assembled structure onto the male end connector on the stand and tighten down the bolt to secure the structure.

14. Attach 1 Waveguide Adapter to a Horn Antenna with 4 M6 bolts and nuts. Repeat until all adapters are connected to Horn Antennas.
15. Attach all 46” SMA cables to the waveguide adapters.
16. Place the 4 Horn Covers over the back Quadrant Panels and attach the remaining 24 bolts and nuts to secure them onto the structure.



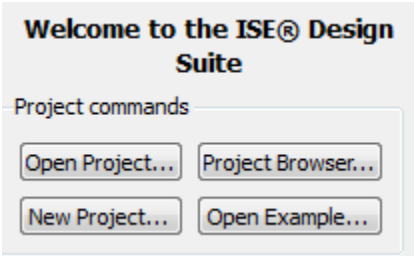
17. Slide all 20 46” SMA cables through the hole in the component box and slide the component box onto the appropriate slot to secure the component box.



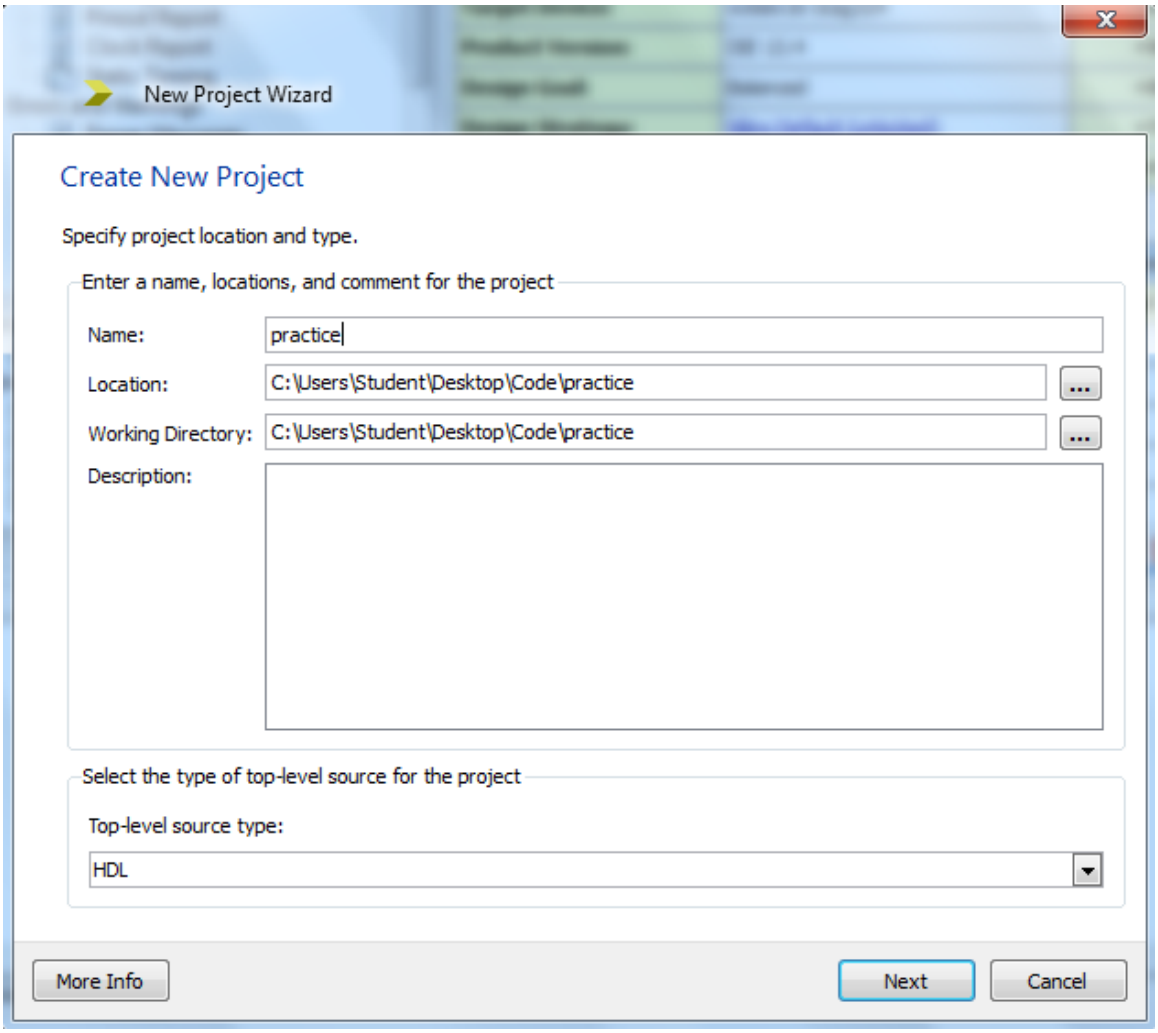
18. Wrap cables accordingly and connect labeled cables to appropriate pins on the SP4T and SP16T Switches inside the component box.

12.5 Software Installation

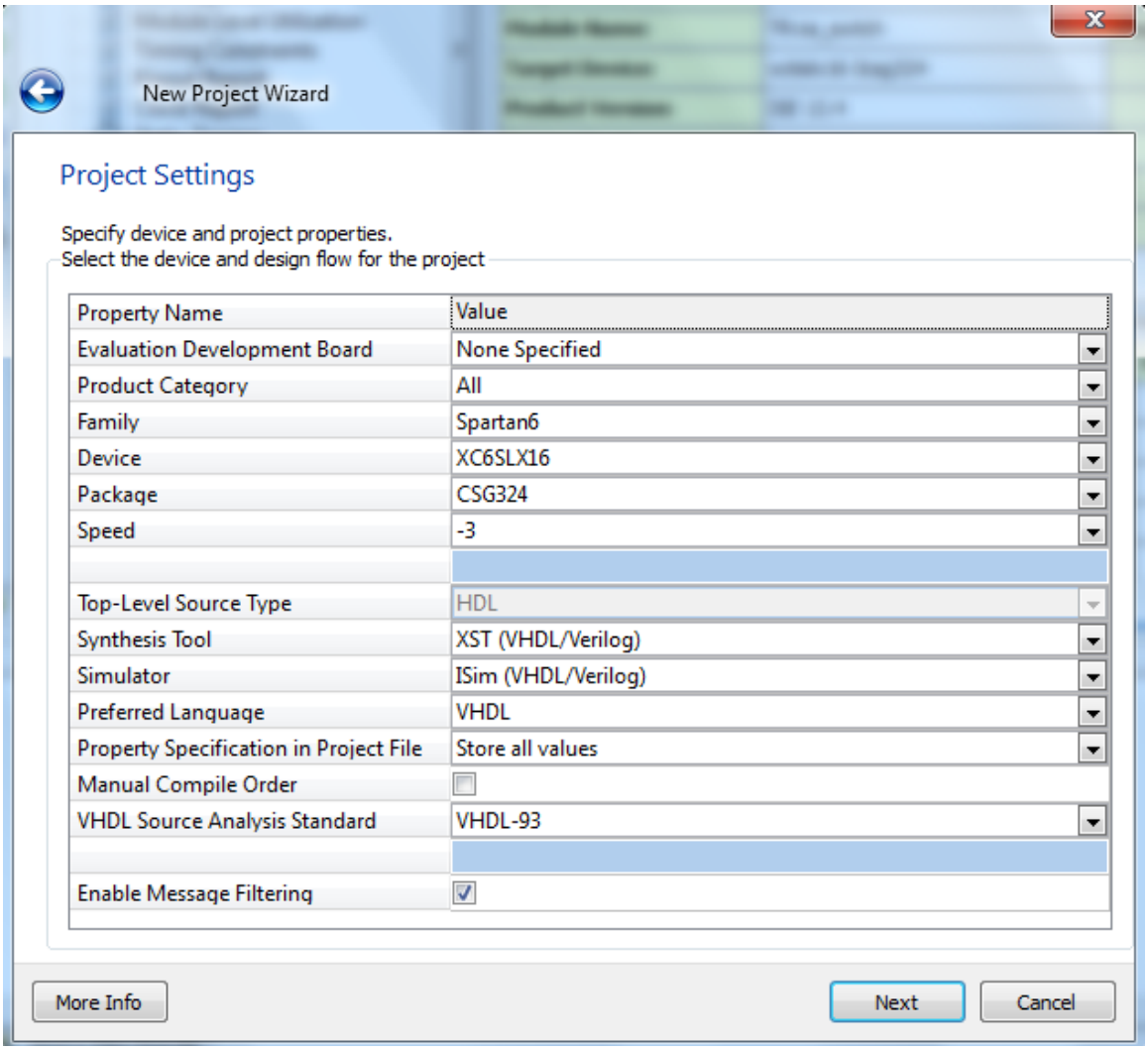
1. You must download ISE Design Suite 13.4. This is an older version of the Xilinx software for Xilinx FPGA's because the Digilent Nexys 3 is an older model. This file can be found on the website for the project.
2. You need to have a windows 7 or below for this Xilinx software. One can be procured at the CMS office in the engineering school. Versions of windows after Windows 7 for Xilinx Design Suite 13.4 are not supported.
3. Once you download Xilinx Design Suite 13.4, a node locked license needs to be acquired. Instructions on how to do this specifically are given when downloading Xilinx Design Suite 13.4. For more detailed instructions, look on the Xilinx website.
4. You need to download the Adept 2 software for Digilent FPGA's. This can be downloaded on the Digilent website.
5. For this project, the FPGA is plugged into the laptop via USB port on the computer and micro USB port on the FPGA. To program for this project, when a file is compiled, a .bit file is created. This .bit file is what is downloaded onto the FPGA.
6. The code for this project is on the school website as well. The two files to look at most are the transmitrecieveswitches, and the transmitrecieveswitches_DEMO.The transmirecieveswitches just has the completed timing and the A/D conversion, which is a good place to start coding for the next semester. The transmitrecieveswitches_DEMO has the completed timing, A/D conversion, and the VGA display in correspondence with the FPGA by altering the brightness depending on the amplitude of the input voltage. This was done to show that the VGA display would light up if a signal was reflected off a target.
    a. Suggestion: Start the VGA code from a separate file, but use the transmitrecieveswitches_DEMO as sample code to see how it was implemented. Use the regular transmitrecieveswitches file as an actual starting point.
7. The VGA display used was a 480x640 display. This display was stored where the structure was stored, if the same display is desired to be used.
8. Steps to program code onto the FPGA. Do this once a node locked liscence is acquired.
9. Click new project



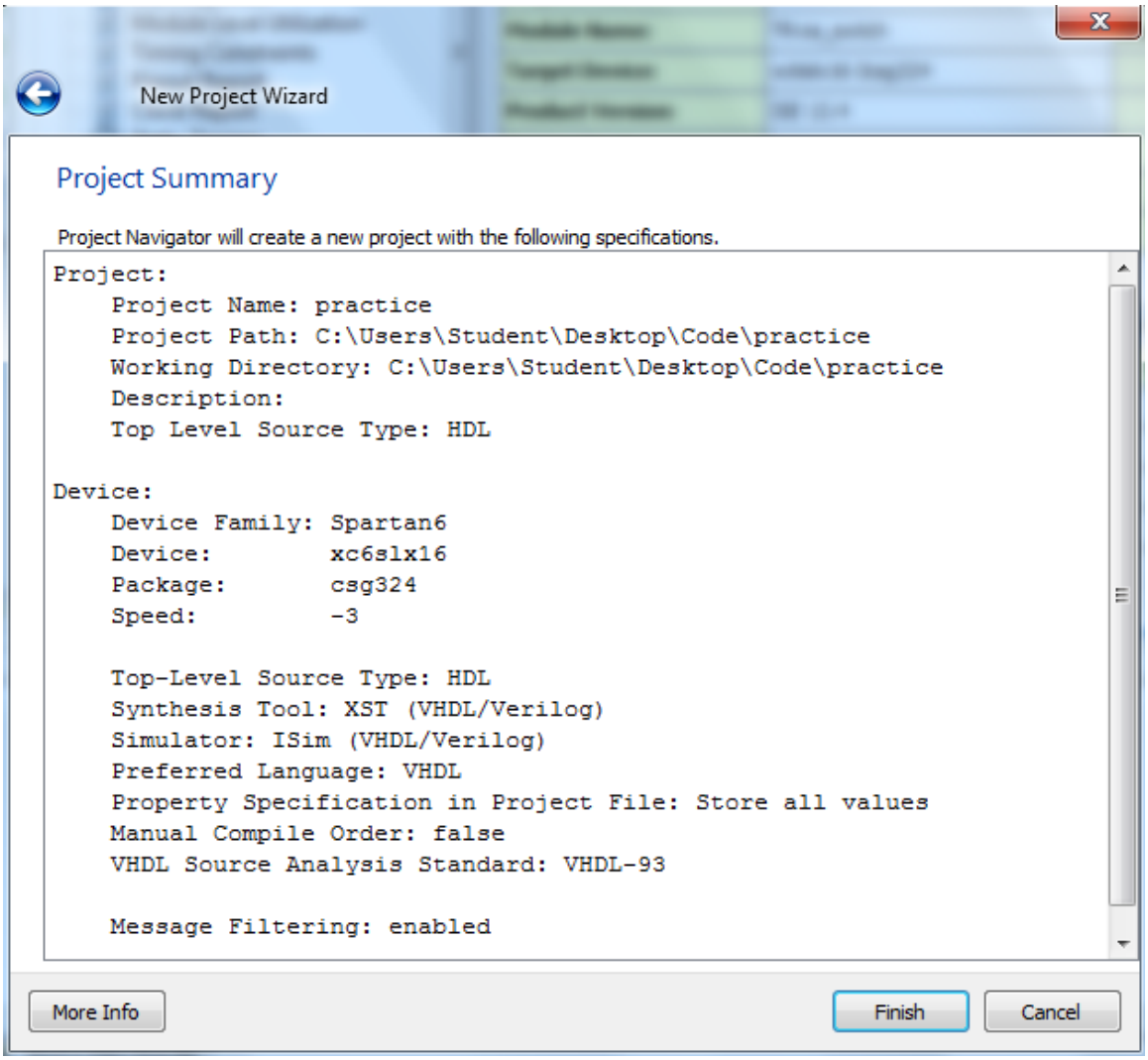
10. Create folder for project. Make sure HDL is chosen



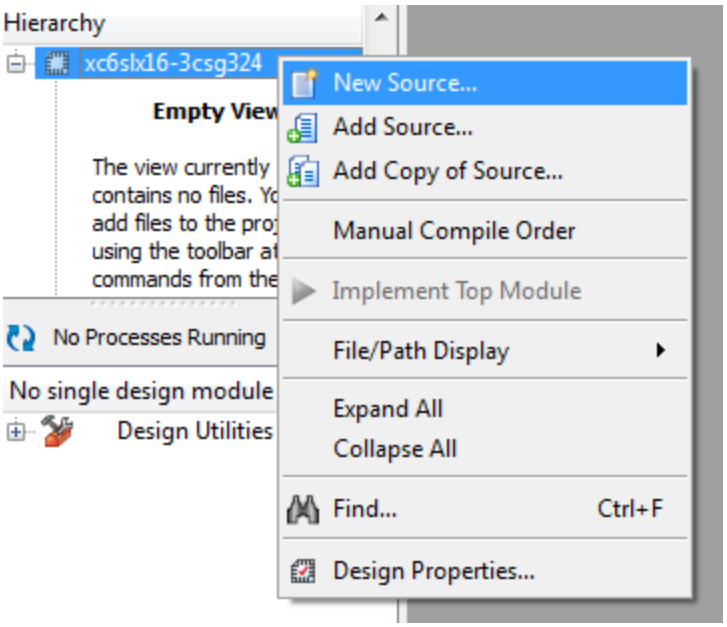
11. Pick the below settings for project settings



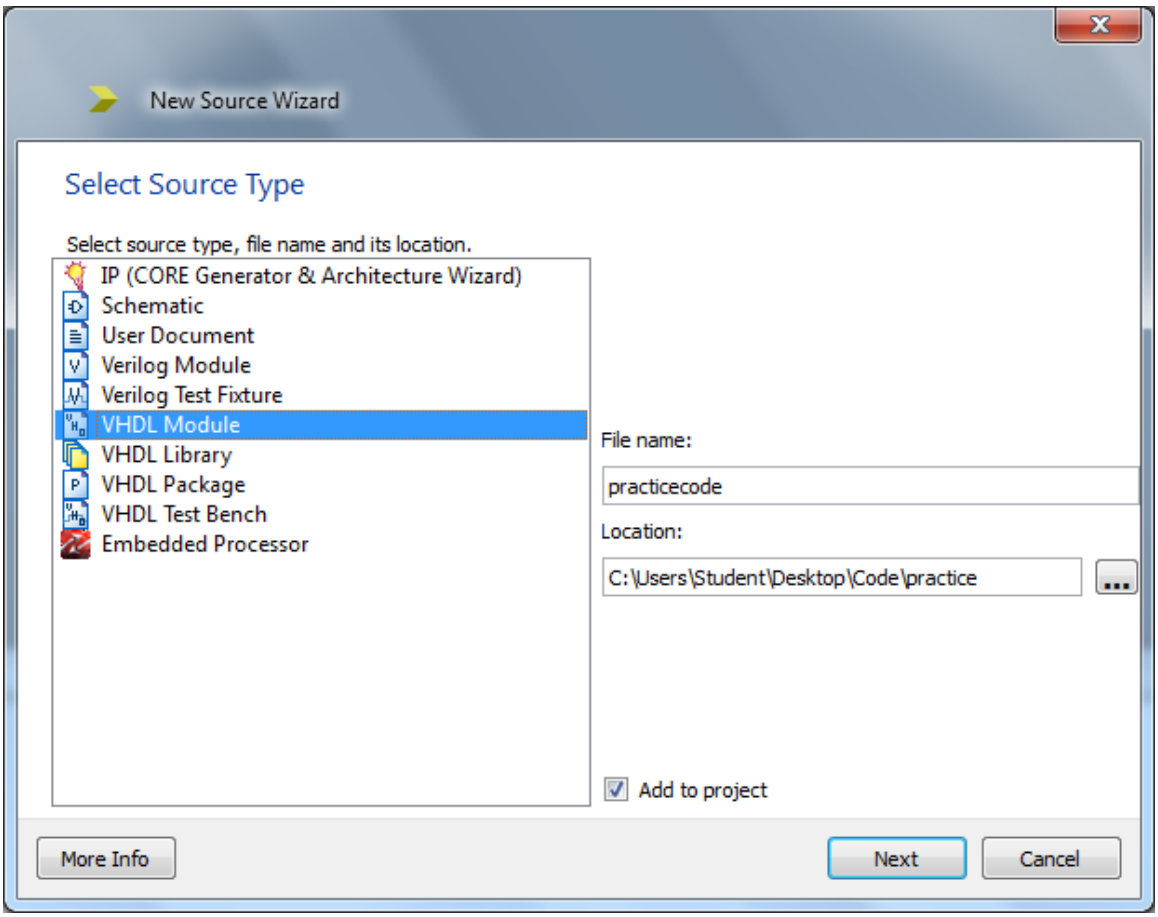
12. Click Finish



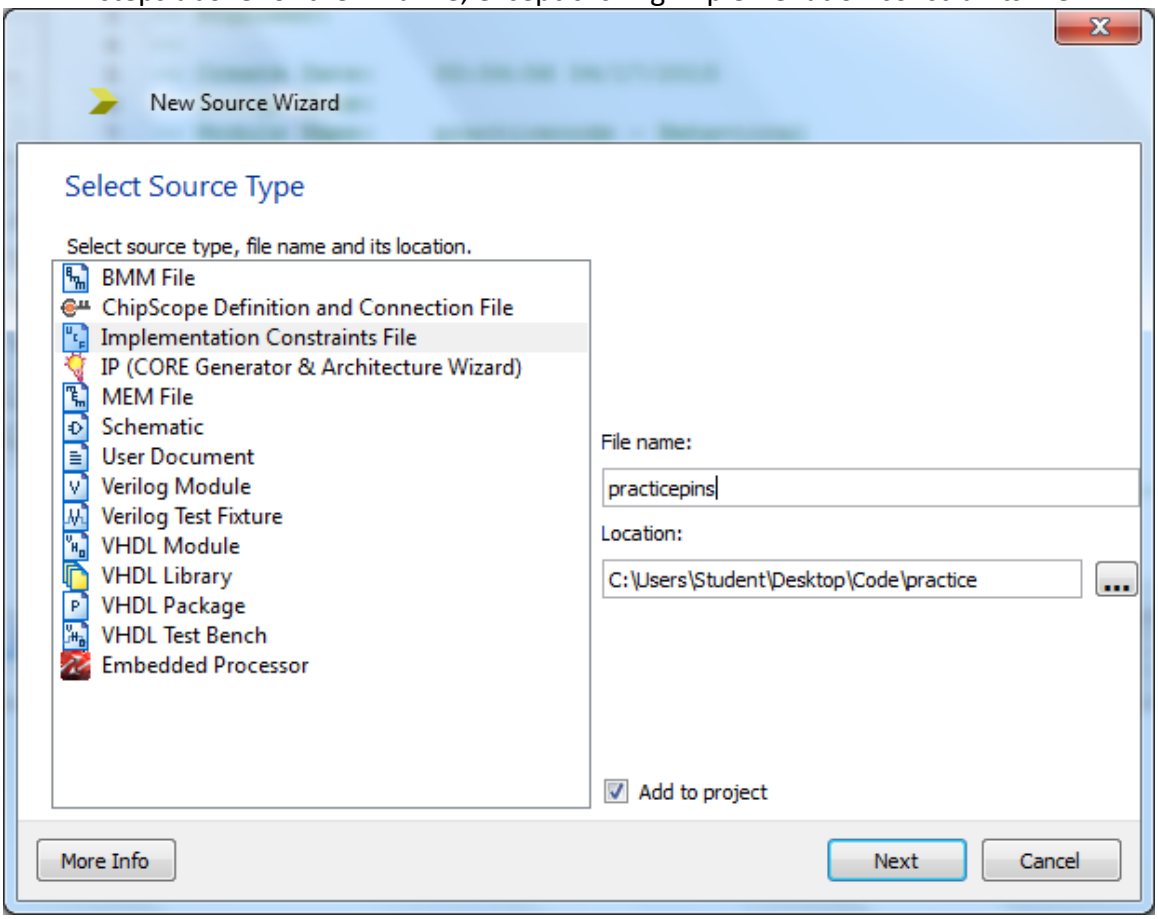
13. Right click hierarchy and click New Source. Note for future projects, clicking add source or add copy of source will just add a source or add a copy of a source respectively.



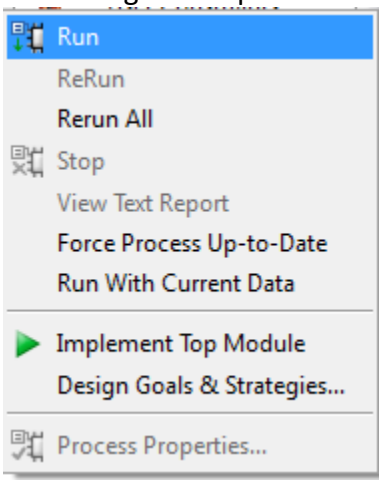
14. Click Add VHDL module. This creates a .vhd file. Click next all the way through and then finish.



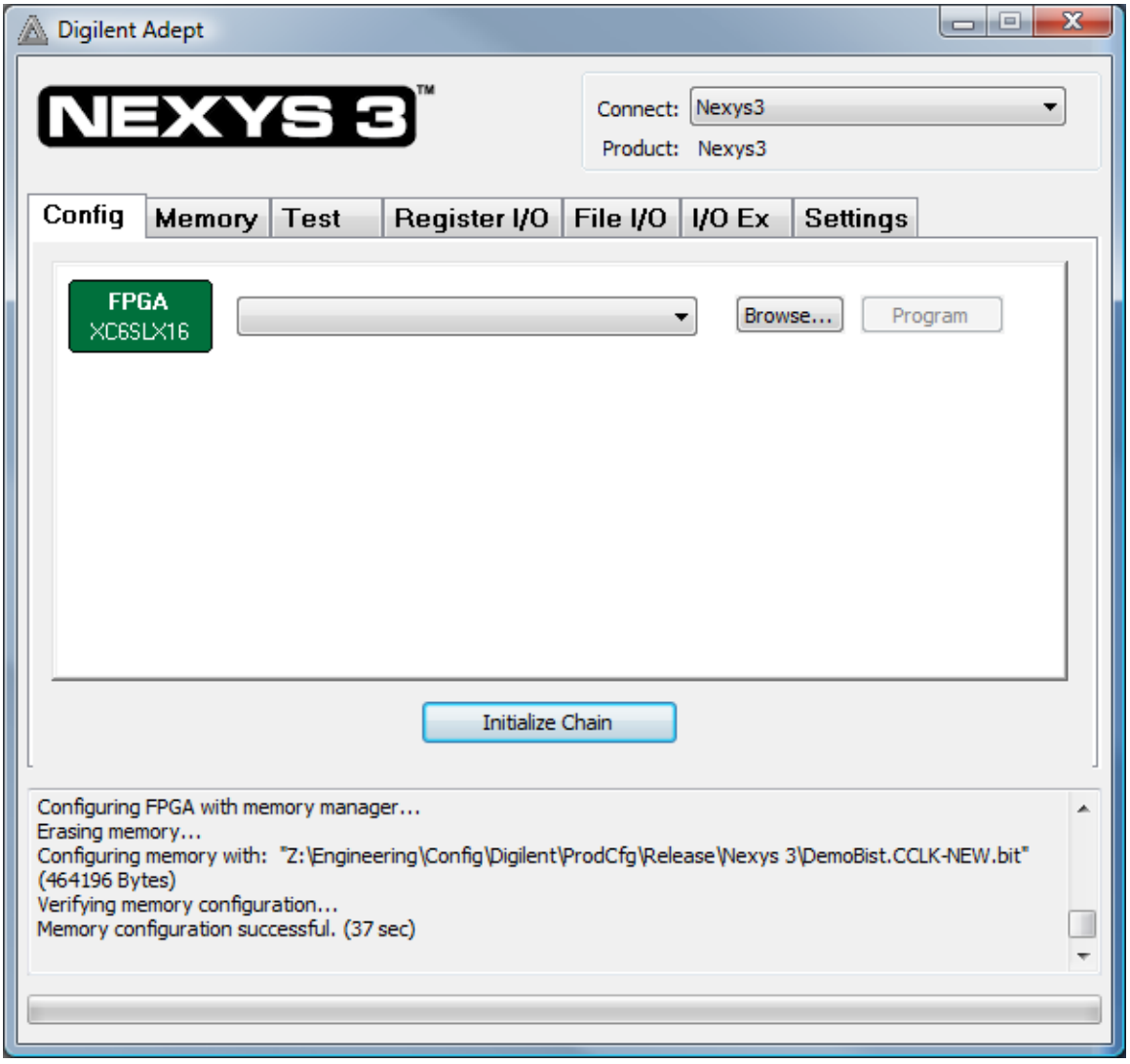
15. Add a .UCF file (user constraints file) for the pin assignments by following the same steps above for the .vhd file, except clicking Implemenation constranits file.



16. Right click process and click run until Generate Programming File has been completed.



17. Go to the adept software, and click browse until the practice.bit file is selected. Click Program and then the FPGA will be programmed.


Digilent Adept
NEXYS 3™
Connect: Nexys3
Product: Nexys3
Config
Memory
Test
Register I/O
File I/O
I/O Ex
Settings
FPGA
XC6SLX16
Browse...
Program
Initialize Chain
Configuring FPGA with memory manager...
Erasing memory...
Configuring memory with: "Z:\Engineering\Config\Digilent\ProdCfg\Release\Nexys 3\DemoBist.CCLK-NEW.bit"
(464196 Bytes)
Verifying memory configuration...
Memory configuration successful. (37 sec)

13 Appendix B – Complete Test Reports

13.1 Appendix B1 - VCO (RF Detector)

Scheduled Test Reporting Form

Test Item: Voltage Controlled Oscillator (VCO) – RF Detector
Tester Name: Joshua Cushion, Matthew Cammuse
Test Date: 2/17/2015
Test Time: 3:30 PM
Test Location: A314
Test Objective: To ensure that the VCO generated a signal with enough power.

Requirements:

- 1- HMC820LP6CE VCO board and USB interface board
- 1- DC power supply
- 1- voltmeter/multimeter
- 1- RF signal detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 30 dB attenuation pads

Procedure:

1. Mount the VCO board at connector J3 onto the USB board at J2. The SEN pin on J3 should be connected to pin 11 of J2.
2. Set the DC power supply to +5.5Vdc
3. Connect the USB interface board and the PC using the USB cable
4. Copy serial number FTVD4CZ8A into blank serial number space and click open interface
5. Select the HMC820LP6CE from the PLL with Integrated RF VCOs dropdown box
6. Connect the RF out connecter to the RF detector
7. Connect the RF detector (BNC female) to the voltmeter using the BNC male to banana jack connector
8. Connect the cables from the power supply to the terminals on the VCO board
    a. TP3: +5.5Vdc
    b. TP4: GND
9. Enable the power supply
10. Record the voltage on the voltmeter

Results:

	Measured				Theoretical		
trial	measured (mV)	output power (uW)	output power (mW)	output power (dBm)	output power (dBm)	output power (mW)	output power (uW)
1	-100	200	0.2	-6.990	-4	0.398	398.1
2	-93.8	187.6	0.188	-7.268	-4	0.398	398.1
3	-104.6	209.2	0.209	-6.794	-4	0.398	398.1
4	-102.1	204.2	0.204	-6.899	-4	0.398	398.1

Comments: It appeared that the VCO did not generate a signal with enough power. However, it was proved that the RF detector had to have attenuation added into the input in order to operate within the square law region. Once this was realized there was 30dB attenuation added and the results for the table below were received.

Measured						
voltmeter (mV)	detector attenuation (dB)	Calibration (uW/mV)	output power w/ detector (uW)	output power w/ detector (mW)	output power w/ detector (dBm)	Calibrated Pout(dBm)
-0.2	30	-2	0.40	0.0004	-33.979	-3.979

13.2 Appendix B2 - Super Ultra Bandwidth Amp

Scheduled Test Reporting Form

Test Item: Super Ultra Wideband Amplifier (TX Chain) – RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the Super Ultra Wideband amplifier is at the designed level.

Requirements:

- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 1- 3 inch RF cable
- Attenuator pads (48 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	V+(V)	I+ (mA)	V-(V)	I-(mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO
2. Using the RF cable to the RF Out connector on the VCO to the RF In connector on the amplifier.
3. Connect the RF Out connector on the amplifier to the input of the attenuator pads.
4. Connect the attenuator pads to the RF detector.
5. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
6. Record the voltage on the voltmeter
7. Disable the power supplies in this order:
    a. +12V
    b. +5.5V

Results:

Measured							Designed Amplifier Output	
Output from VCO		**Output from Amplifier**						
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
-3.979	0.400	-1.70	0.003	-24.685	23.315	214.536	21.88	154.1700

Comments:
n/a

13.3 Appendix B3 – SPDT

Scheduled Test Reporting Form

Test Item: Single Pole Double Throw (SPDT) Switch - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the SPDT switch is at the designed level. Also to determine the level at which the control voltage will cause the output to switch channels.

Requirements:

- 1- SPDT Switch (HMC-C011)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 2- 3 inch RF cables
- Attenuator pads (48 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Control Voltage	Variable	-	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier
3. Using the RF cable to the RF Out connector on the amplifier to the RF COM connector on the amplifier.
4. Connect the RF2 connector on the SPDT to the input of the attenuator pads.
5. Connect the attenuator pads to the RF detector.
6. Ground the CTL pin.
7. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V

d. CTL supply

8. Record the voltage on the voltmeter.
9. Increase the voltage of the power supply connected to the CTL pin until the voltmeter reads 0V.

10. Disable the power supplies in this order:
    a. CTL supply
    b. +5V
    c. +12V
    d. +5.5V

Results:
See table 2 for calibrated output power column (this accounts for the attenuation needed in order to avoid stressing the RF detector).
The output switched from RF2 to RF1 at +3.2 V.

Comments:
n/a

Output from Amplifier		**Measured Output from SPDT**					**Designed SPDT Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
23.315	214.525	-1.10	0.002	-26.576	21.424	138.803	19.530	89.743

13.4 Appendix B4 – Frequency Multiplier

Scheduled Test Reporting Form

Test Item: Frequency Multiplier - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the frequency multiplier is at the designed level.

Requirements:

- 1- Frequency Multiplier (ZX90-2-50-S+)
- 1- SPDT Switch (HMC-C058)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 3- 3 inch RF cables
- 1- 5 inch RF cable
- 1- 10dB attenuator pad
- Attenuator pads (20 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO.
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier.
3. SPDT setup: follow the steps shown in the test form for the SPDT. Leave the CTL pin empty.
4. Using the RF cable to the RF2 connector on the SPDT to the input of the 10dB attenuator pad. Connect the output of the attenuator pad to the RF IN connector on the frequency multiplier using a 5 inch RF cable.
5. Connect the RF Out connector on the frequency multiplier to the input of the attenuator pads.
6. Connect the attenuator pads to the RF detector.

7. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V

8. Record the voltage on the voltmeter.
9. Disable the power supplies in this order:
    a. +5V
    b. +12V
    c. +5.5V

Results:
See table 2 for calibrated output power column (this accounts for the attenuation needed in order to avoid stressing the RF detector).

Comments:
n/a

Output from 10dB pad		**Measured Output from Multiplier**					**Designed Multiplier Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
11.424	13.88	-3.40	0.007	-21.675	-1.675	0.680	-3.088	0.491

Table 2: Output Power Results

13.5 Appendix B5 – Ultra Amp

Scheduled Test Reporting Form

Test Item: Ultra Wide Bandwidth Amplifier - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the ultra-wide bandwidth amplifier is at the designed level.

Requirements:

- 1- Frequency Multiplier (ZX90-2-50-S+)
- 1- SPDT Switch (HMC-C058)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 3- 3 inch RF cables
- 1- 5 inch RF cable
- 1- 10dB attenuator pad
- Attenuator pads (38 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO.
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier.
3. SPDT setup: follow the steps shown in the test form for the SPDT.
4. Frequency Multiplier setup: follow the steps shown in the test form for the multiplier.
5. Connect the RF Out connector on the frequency multiplier to the input of the ultra-wide bandwidth amplifier using the appropriate SMA adapter.
6. Connect the output of the ultra-wide bandwidth amplifier to the input of the attenuator pads.

7. Connect the attenuator pads to the RF detector.
8. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V
    d. +12V (ultra-wide bandwidth amp)

9. Record the voltage on the voltmeter.
10. Disable the power supplies in this order:
    a. +12V (ultra wide bandwidth amp)
    b. +5V
    c. +12V
    d. +5.5V

Results:
See table 2 for calibrated output power column (this accounts for the attenuation needed in order to avoid stressing the RF detector).
PASSED.

Comments:
n/a

Output from Multiplier		**Measured Output from Amplifier**					**Designed Amplifier Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
-1.675	0.680	-0.70	0.001	-28.539	9.461	8.833	8.913	7.785

Table 2: Output Power Results

13.6 Appendix B6 – BPF

Scheduled Test Reporting Form

Test Item: Band Pass Filter - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the band pass filter is at the designed level.
Requirements:

- 1- Band Pass Filter (FB-1050)
- 1- Frequency Multiplier (ZX90-2-50-S+)
- 1- SPDT Switch (HMC-C058)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 5- 3 inch RF cables
- 1- 5 inch RF cable
- 1- 10dB attenuator pad
- 1- 3dB attenuator pad
- 1- variable attenuator or a 15dB attenuator pad
- Attenuator pads (20 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO.
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier.
3. SPDT setup: follow the steps shown in the test form for the SPDT.
4. Frequency Multiplier setup: follow the steps shown in the test form for the multiplier.
5. Ultra wide bandwidth amplifier setup: follow the steps shown in the test form for the ultra-wide bandwidth amplifier.
6. Connect the RF Out connector on the ultra-wide bandwidth amplifier to the input of the variable attenuator (15dB) or the 15dB attenuator pad using a 3 inch RF cable.

7. Connect the output of the variable attenuator or the 15 dB attenuator pad to the input of the band pass filter using a 3 inch RF cable.
8. Connect the output of the band pass filter to the input of the 20dB attenuator pads.
9. Connect the output 20dB attenuator pads to the RF detector.
10. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V
    d. +12V (ultra-wide bandwidth amp)

11. Record the voltage on the voltmeter.
12. Disable the power supplies in this order:
    a. +12V (ultra-wide bandwidth amp)
    b. +5V
    c. +12V
    d. +5.5V

Results:

Output from Variable Attenuator		**Measured Output from Band Pass Filter**					**Designed Band Pass Filter Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
-5.54	0.280	-0.01	0.000016	-47.96	-27.960	0.0016	-6.323	0.233

Table 2: BPF Output Power Results

Output from Variable Attenuator		**Measured Output from 3dB Attenuator**					**Designed 3dB Attenuator Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
-5.54	0.280	-0.6	0.0.001	-29.208	-9.208	0.12	-6.323	0.233

Table 3: 3dB Attenuator Output Power Results

Comments:
The gain of the band pass filter is not -3 dB as stated in the datasheet. It is suggested that the frequency of the signal may not be 10 GHz.

13.7 Appendix B7 – Power Amplifier

Scheduled Test Reporting Form

Test Item: Power Amplifier - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the power amplifier is at the designed level.

Requirements:

- 1- Power Amplifier (SPA-110-30-01-SMA)
- 1- Band Pass Filter (FB-1050)
- 1- Frequency Multiplier (ZX90-2-50-S+)
- 1- SPDT Switch (HMC-C058)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 5- 3 inch RF cables
- 2- 5 inch RF cables
- 1- 10dB attenuator pad
- 1- 3dB attenuator pad
- 1- variable attenuator or a 15dB attenuator pad
- Attenuator pads (44 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-
Power Amplifier	15	900	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO.
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier.
3. SPDT setup: follow the steps shown in the test form for the SPDT.
4. Frequency Multiplier setup: follow the steps shown in the test form for the multiplier.
5. Ultra wide bandwidth amplifier setup: follow the steps shown in the test form for the ultra-wide bandwidth amplifier.
6. Band pass filter (3dB pad) setup: follow the steps shown in the test form for the band pass filter.
7. Connect the RF Out connector on the band pass filter (3dB attenuator pad) to the input of the power amplifier using a 5 inch RF cable.
8. Connect the output of the power amplifier to the input of the 44dB attenuator pads.
9. Connect the output 44dB attenuator pads to the RF detector.
10. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V
    d. +12V (ultra-wide bandwidth amp)
    e. +15V

11. Record the voltage on the voltmeter.
12. Disable the power supplies in this order:
    a. +15V
    b. +12V (ultra-wide bandwidth amp)
    c. +5V
    d. +12V
    e. +5.5V

Results:

Output from BPF/3dB Attenuator		**Measured Output from Power Amplifier**					**Designed Power Amplifier Output**	
Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)	Output Power (dBm)	Output Power (mW)
-9.208	0.12	-2.4	0.005	-23.188	20.812	120.6	25.482	353.319

Table 2: Output Power Results

Comments:
Used the 3dB attenuator pad in place of the band pass filter.

13.8 Appendix B8 – SP4T

Scheduled Test Reporting F

Test Item: Single Pole Four (SP4T) Throw Switch - RF Detector
Tester Name: Joshua Cushion
Test Date: 3/3/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the signal power coming from the SP4T switch is at the designed level. Also to verify that the switch will switch output ports at the specified 5V level.

Requirements:

- 1- SP4T Switch (RFSP4TA0812G)
- 1- Power Amplifier (SPA-110-30-01-SMA)
- 1- Band Pass Filter (FB-1050)
- 1- Frequency Multiplier (ZX90-2-50-S+)
- 1- SPDT Switch (HMC-C058)
- 1- Super Ultra Wideband Amplifier (ZVA-183-S+)
- 1- HMC820LP6CE VCO board and USB interface board
- Power supply voltages (see table 1 below)
- 1- voltmeter/multimeter
- 1- RF power detector (Agilent -8472B)
- 1- BNC male to dual banana jacks cable
- 2- Banana jack to push clip cables
- 1- USB cable (provided with evil. kit)
- 1- Computer with Hittite PLL Eval. Software
- 6- 3 inch RF cables
- 2- 5 inch RF cables
- 1- 10dB attenuator pad
- 1- 3dB attenuator pad
- 1- variable attenuator or a 15dB attenuator pad
- Attenuator pads (44 dB total)
- Multiple SMA: male-male, male-female, female-female connectors

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
VCO	5.5	45	-	-
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-
Power Amplifier	15	900	-	-
SP4T Switch	5	160	5	50
4- 5V (SP4T VCTL)	5	-	-	-

Table 1: Power Supply Requirements

Procedure:

1. VCO setup: follow the steps shown in the test form for the VCO.
2. Super Ultra Wideband amplifier setup: follow the steps shown in the test form for the amplifier.
3. SPDT setup: follow the steps shown in the test form for the SPDT.
4. Frequency Multiplier setup: follow the steps shown in the test form for the multiplier.
5. Ultra wide bandwidth amplifier setup: follow the steps shown in the test form for the ultra-wide bandwidth amplifier.
6. Band pass filter (3dB pad) setup: follow the steps shown in the test form for the band pass filter.
7. Power amplifier setup: follow the steps shown in the test form for the power amplifier.
8. Connect the RF Out connector on the power amplifier to the input of the SP4T switch using a 3 inch RF cable.
9. Connect the output of the SP4T switch to the input of the 44dB attenuator pads.
10. Connect the output 44dB attenuator pads to the RF detector.
11. Enable the power supplies in the following order:
    a. +5.5V
    b. +12V
    c. +5V
    d. +12V (ultra-wide bandwidth amp)
    e. +15V
    f. ±5V
    g. +5V(VCTL)
12. Apply the +5V control voltages as follows:

Control Input Pin				Output
C4	C3	C2	C1	Port
5V	5V	0V	0V	J1
5V	5V	0V	5V	J2
5V	0V	5V	5V	J3
0V	0V	5V	5V	J4

Table 2: Switch Truth Ta

NOTE: Instead of leaving the pins unconnected to apply 0V using as stated in the truth table.

13. Record the voltage on the voltmeter.
14. Disable the power supplies in this order:
    a. +5V(VCTL)
    b. ±5V
    c. +15V
    d. +12V (ultra-wide bandwidth amp)
    e. +5V
    f. +12V
    g. +5.5V

Results:

	Measured						
	Output from Power Amplifier			Output from SP4T			
Port	Output Power (dBm)	Output Power (mW)	Voltmeter Reading (mV)	Output Power (mW)	Output Power (dBm)	Calibrated Output Power (dBm)	Calibrated Output Power (mW)
J1	20.812	120.57	-1.00	0.002	-26.990	17.01	50.238
J2	20.812	120.57	-1.00	0.002	-26.990	17.01	50.238
J3	20.812	120.57	-1.00	0.002	-26.990	17.01	50.238
J4	20.812	120.57	-1.00	0.002	-26.990	17.01	50.238

Table 3A: Output Power Resul

	Designed SP4T Output	
Port	Output Power (dBm)	Output Power (mW)
J1	20.364	108.747
J2	20.364	108.747
J3	20.364	108.747
J4	20.364	108.747

Table 3B: Output Power Resul

Comments:
Used the 3dB attenuator pad in place of the band pass filter.

13.9 Appendix B9 – Transmit Chain No Pulse

Scheduled Test Reporting Form

Test Item: Transmit Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the peak power output from the SP4T switch of the transmit chain is at the correct level and frequency.
Requirements:

- Assembled Transmit chain (see SP4T RF detector form)
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (39 dB total)

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-
Power Amplifier	15	900	-	-
SP4T Switch	5	160	5	50
4- 5V (SP4T VCTL)	5	-	-	-
1- 5V (SPDT VCTL)	5	-	-	-

Table 1: Power Supply Requirements

Procedure:

12. Connect the output of the RF signal generator to the input of the spectrum analyzer using a short RF cable.
13. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
14. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -4 dBm and frequency of 5 GHz.
15. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the super ultra-wide bandwidth amplifier.
16. Connect the RF Out (J1) connector on the SP4T to the input of the attenuator pads using the short RF cable.
17. Connect the output of the pads to the input of the analyzer.
18. Set one of the CTL voltage supplies to 5V and connect it to the SPDT. The positive terminal to the CTL pin and the ground terminal to the GND pin.
19. Enable the power supplies in the following order:
    a. +12V

b. +5V
c. +12V (ultra-wide bandwidth amp)
d. +15V
e. ±5V
f. +5V(VCTL)

20. Apply the +5V control voltages as follows:

Control Input Pin				Output Port
C4	C3	C2	C1	
5V	5V	0V	0V	J1
5V	5V	0V	5V	J2
5V	0V	5V	5V	J3
0V	0V	5V	5V	J4

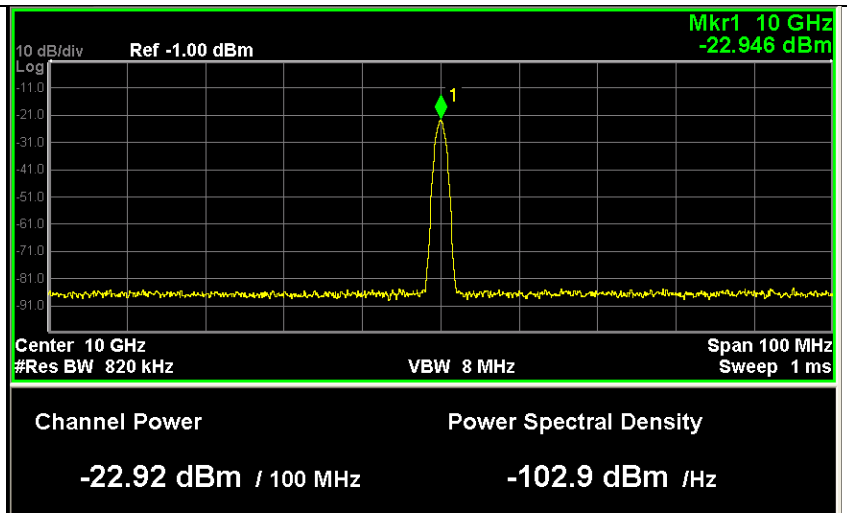
Table 2: Switch Truth Table

NOTE: Instead of leaving the pins unconnected to apply 0V using as stated in the truth table.

21. Record the peak power and frequency shown on the spectrum analyzer.
22. Disable the power supplies in this order:
    a. +5V(VCTL)
    b. ±5V
    c. +15V
    d. +12V (ultra-wide bandwidth amp)
    e. +5V
    f. +12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
42	-22.946	19.054	80.427	10	21.804	78.599	10



Comments:
PASSED
39 dB loss for attenuation pads, 3 dB for the RF cable connected at the output of the SP4T to the spectrum analyzer. The power can be increased or decreased by using the variable attenuator.

13.10 Appendix B10 – Transmit Chain Pulse

Scheduled Test Reporting Form

Test Item: Transmit Chain – Frequency, Pulse width, power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the transmit signal from the SP4T switch is pulsing at 20nS and the period is approximately 65nS.
Requirements:

- Assembled Transmit chain (see SP4T RF detector form)
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 1- Pulse generator
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (39 dB total)

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-
Power Amplifier	15	900	-	-
SP4T Switch	5	160	5	50
4- 5V (SP4T VCTL)	5	-	-	-

Table 1: Power Supply Requirements

Procedure:

1. Connect the output of the RF signal generator to the input of the spectrum analyzer using a short RF cable.
2. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
3. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -4 dBm and frequency of 5 GHz.
4. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the super ultra-wide bandwidth amplifier.
5. Connect the RF Out (J1) connector on the SP4T to the input of the attenuator pads using the short RF cable.
6. Connect the output of the pads to the input of the analyzer.
7. Pulse generator/SPDT: connect the positive terminal to the CTL pin and the ground terminal to the GND pin. Input the following settings:
    a. Amplitude: 2V
    b. Pulse width: 25nS
    c. Period: 65nS
8. Enable the power supplies in the following order:

a. +12V
b. +5V
c. +12V (ultra wide bandwidth amp)
d. +15V
e. ±5V
f. Pulse generator
g. +5V(VCTL)

9. Apply the +5V control voltages as follows:

Control Input Pin				Output Port
C4	C3	C2	C1	
5V	5V	0V	0V	J1
5V	5V	0V	5V	J2
5V	0V	5V	5V	J3
0V	0V	5V	5V	J4

Table 2: Switch Truth Table

NOTE: Instead of leaving the pins unconnected to apply 0V using as stated in the truth table.

10. Record the frequency at the peak of the spectral line to the immediate right of the center line on the spectrum analyzer.
11. Record the frequency of the null of the first lobe that contains the center spectral line.
12. Disable the power supplies in this order:
    a. +5V(VCTL)
    b. Pulse generator
    c. ±5V
    d. +15V
    e. +12V (ultra wide bandwidth amp)
    f. +5V
    g. +12V

Results:

In order to measure the period of the pulse using the spectrum analyzer, one must measure the frequency of the spectral lines (not the center frequency). Marker 1 in figure 1 shows that the first spectral line to the right of the center frequency is 15 MHz. This shows that the period of the pulse is about 66.67 nS. This data is supported by the fact that the Fourier transform of a pulse train is a sinc function and the spectral lines occur at frequencies of the multiples of 1/period. Thus the measured period is close enough to 65nS.

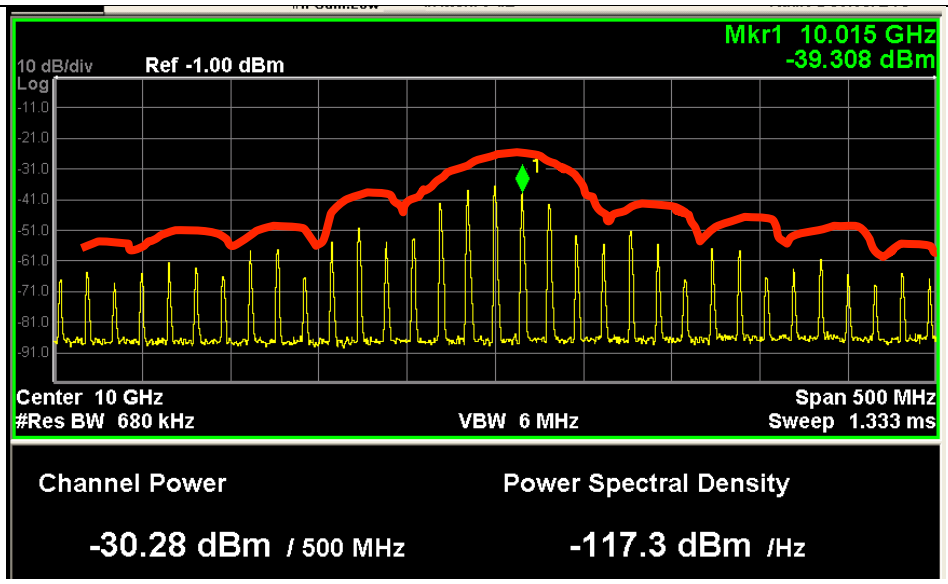


Figure 1: Period of Transmit Signal

Figure 2 shows the pulse width. As shown in the figure the spectral lines take the shape of a sinc function. The nulls of each lobe in the sinc function are where the frequency of the pulse width occur. The designed pulsed width is 20 nS which is 50 MHz in the frequency domain. As shown if figure 2 marker 1 occurs at about 50 MHz.

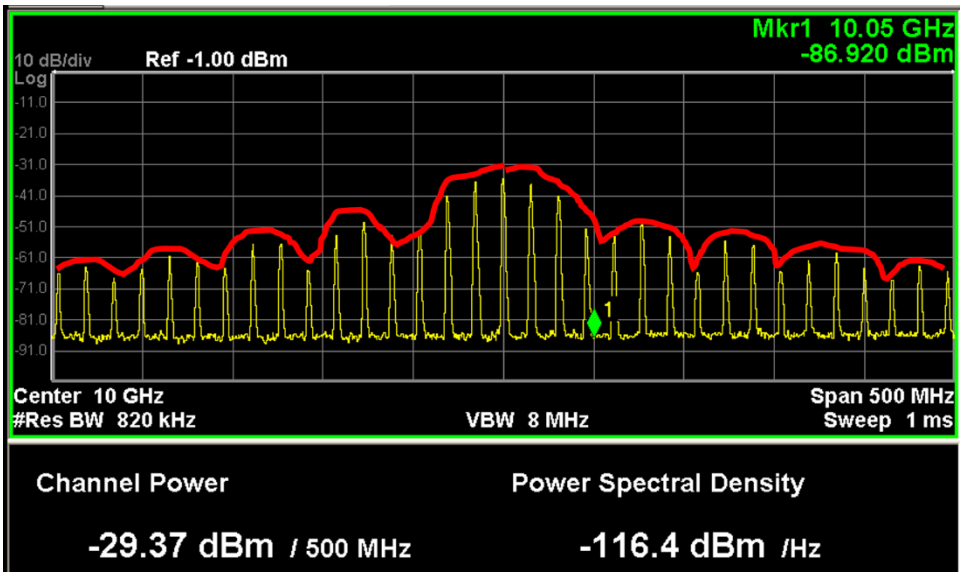


Figure 2: Pulse Width of Transmit Signal

Comments: PASSED

The pulse generator was set to a 25nS pulse to account for the rise and fall time in the SPDT switch. The period was set to 65nS to have a low signal for 40nS. To calculate the power of the pulse the equation used was:

Power (dBm) = power/span(dBm) + attenuation(dB) -10*log(duty cycle)

Power Equation

Power/span: -29.37 dBm/500 MHz
Attenuation: 39 dB (pads), 3 dB (cable)
Duty cycle: 20nS/66.6nS
Measured Power: 19.815 dBm Designed power: 18.954 dBm

13.11 Appendix B11 – RX lna1 No Pulse –Spec Analyzer

Scheduled Test Reporting Form

Test Item: Receive Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the peak power output from the first low noise amplifier (SLNA-120-38-22-SMA) in the receive chain.
Requirements:

- Assembled Receive Chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (20 dB) – needed if RF signal generator cannot generate an output signal with and amplitude of -50 dBm

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
LNA:SLNA-120-38-22-SMA	12	250	-	-
Single Pole 16 Throw Switch	5	550(max)	-12	200(max)
1- 0V (SP16T VCTL)	0	-	-	-

Table 1: Power Supply Requirements

Procedure:

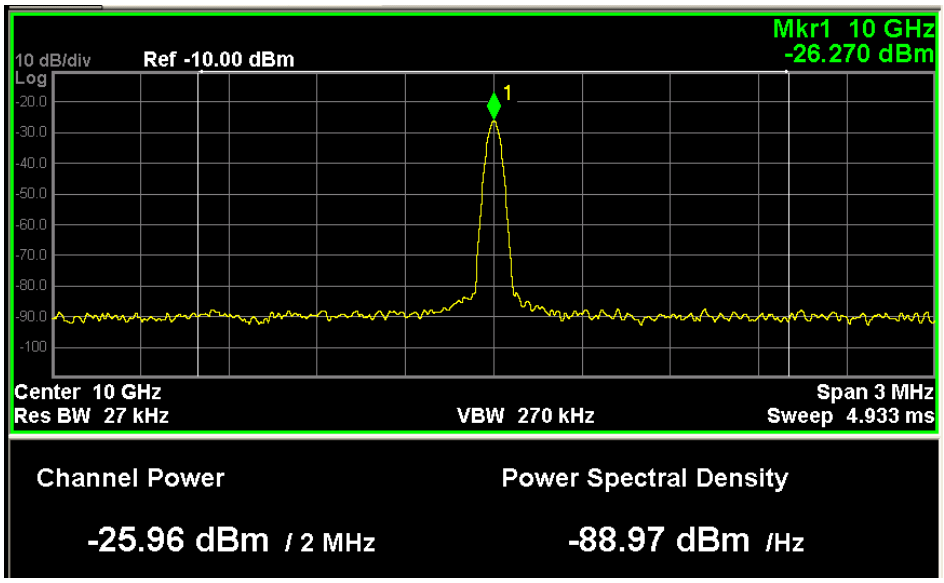
13. Connect the output of the RF signal generator to the input of the 20 dB attenuator pads.
14. Connect the output of the 20 dB pads to the input of the spectrum analyzer using a short RF cable.
15. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
16. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -51 dBm and frequency of 10 GHz.
17. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the SP16T switch at the desired channel.
18. The COM port of the SP16T switch should be connected to the band pass filter.
19. The BPF should be connected to the input of the low noise amplifier.
20. Connect the RF Out connector on the LNA to the input of the analyzer.
21. Set one of the CTL voltage supplies to 0V and connect it to the SP16T control pin that corresponds to the correct channel connected to the RF signal generator. The positive terminal to the CTL pin and the ground terminal to the GND pin.
22. Enable the power supplies in the following order:
    a. -12V
    b. +5V
    c. +12V

d. +0V(VCTL)

23. Record the peak power and frequency shown on the spectrum analyzer.
24. Disable the power supplies in this order:
    a. +0V(VCTL)
    b. +12V
    c. +5V
    d. -12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
3	-26.270	-23.270	0.00471	10	-23.068	4.934E-3	10



Comments:

PASSED

The attenuation was due to the loss in the cable connected to the spectrum analyzer.

13.12 Appendix B12 – RX lna2 No Pulse –Spec Analyzer

Scheduled Test Reporting Form

Test Item: Receive Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the peak power output from the second low noise amplifier (SLNA-180-38-25-SMA) in the receive chain.
Requirements:

- Assembled Receive Chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (16 dB)
- Attenuator pads (20 dB) – needed if RF signal generator cannot generate an output signal with and amplitude of -50 dBm

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
LNA:SLNA-120-38-22-SMA	12	250	-	-
LNA:SLNA-180-38-25-SMA	12	280	-	-
Single Pole 16 Throw Switch	5	550(max)	-12	200(max)
1- 0V (SP16T VCTL)	0	-	-	-

Table 1: Power Supply Requirements

Procedure:

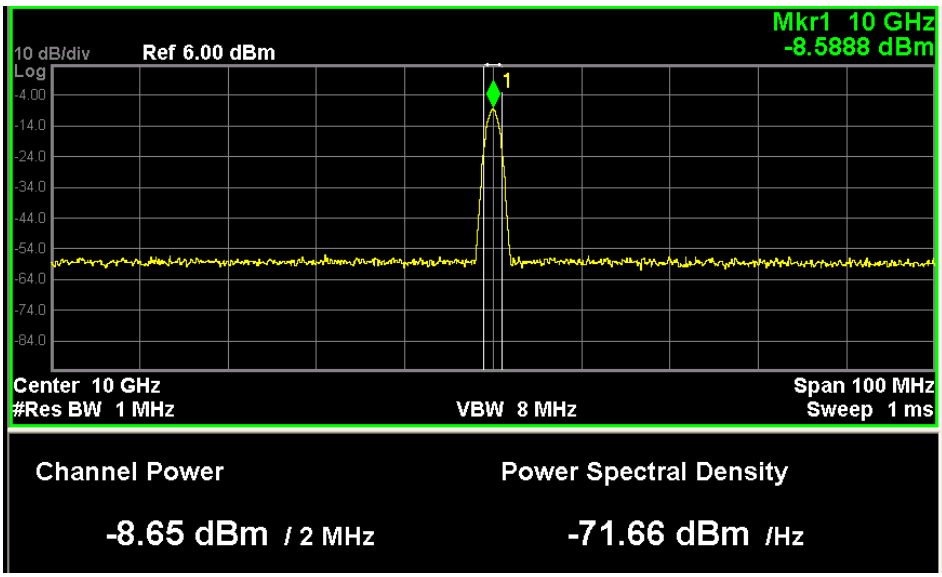
1. Connect the output of the RF signal generator to the input of the 20 dB attenuator pads.
2. Connect the output of the 20 dB pads to the input of the spectrum analyzer using a short RF cable.
3. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
4. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -51 dBm and frequency of 10 GHz.
5. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the SP16T switch at the desired channel.
6. The COM port of the SP16T switch should be connected to the band pass filter.
7. The BPF should be connected to the input of the low noise amplifier 1.
8. The output from the LNA 1 should be connected to the input of the variable attenuator and the output of the variable attenuator should be connected to the input of the LNA 2.
9. Connect the RF Out connector on the LNA2 to the 6dB attenuation pad then to the input of the analyzer.
10. Set one of the CTL voltage supplies to 0V and connect it to the SP16T control pin that corresponds to the correct channel connected to the RF signal generator. The positive

terminal to the CTL pin and the ground terminal to the GND pin.

11. Enable the power supplies in the following order:
    a. -12V
    b. +5V
    c. +12V (LNA1)
    d. +12V(LNA2)
    e. +0V(VCTL)
12. Record the peak power and frequency shown on the spectrum analyzer.
13. Disable the power supplies in this order:
    a. +0V(VCTL)
    b. +12V (LNA1)
    c. +12V(LNA2)
    d. +5V
    e. -12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
9	-8.5888	10.411	10.993	10	0.540	1.132	10



Comments:

PASSED

The attenuation is due to the 3 dB loss in the cable and 6 dB loss due to the attenuation pad at the input of the spectrum analyzer.

13.13 Appendix B13 – IQ No Pulse Spec Analyzer

Scheduled Test Reporting Form

Test Item: LO IQ Demodulator Chain – Peak Power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the transmit signal from the going into the LO port of the IQ demodulator is at the designed peak power of approximately 5.559dBm.
Requirements:

- Assembled LO IQ demodulator chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 1- Pulse generator
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (39 dB total)

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-

Table 1: Power Supply Requirements

Procedure:

1. Connect the output of the RF signal generator to the input of the spectrum analyzer using a short RF cable.
2. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
3. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -4 dBm and frequency of 5 GHz.
4. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the super ultra-wide bandwidth amplifier.
5. Connect the RF Out connector on the 3dB pad (connected to the ultrawide bandwidth amplifier) to the input of the attenuator pads using the short RF cable.
6. Connect the output of the pads to the input of the analyzer.
7. Set one of the CTL voltage supplies to 0V and connect it to the SPDT. The positive terminal to the CTL pin and the ground terminal to the GND pin.
8. Enable the power supplies in the following order:
    a. +12V
    b. +5V
    c. +12V (ultra wide bandwidth amp)

9. Record the peak power and frequency shown on the spectrum analyzer.
10. Disable the power supplies in this order:
    a. +12V (ultra wide bandwidth amp)
    b. +5V
    c. +12V

Results:

	Measured				Theoretical		
Attenuation (dB)	Measured Output Power (dBm)	Calibrated Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)	Output Power (dBm)	Output Power (mW)	Output Frequency (GHz)
42	-37.262	4.738	2.977	10	5.599	3.258	10

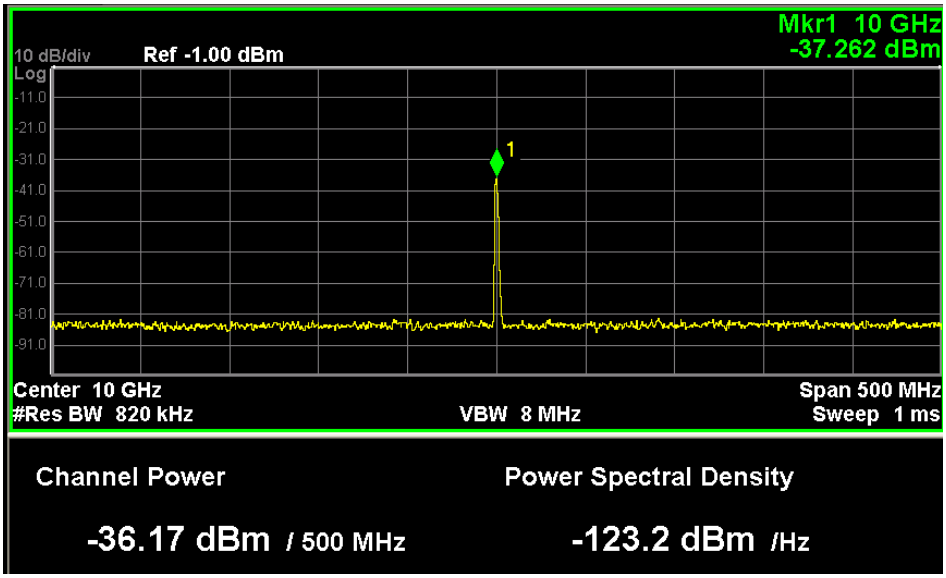


Figure 1: Peak power measured

Comments:

PASSED

39 dB loss for attenuation pads, 3 dB for the RF cable connected at the output of the 3dB pad coming from the ultra-wide bandwidth amplifier to the spectrum analyzer.

13.14 Appendix B14 – IQ Pulsing Spec Analyzer

Scheduled Test Reporting Form

Test Item: LO IQ Demodulator Chain – Frequency, Pulse width, power
Tester Name: Joshua Cushion
Test Date: 4/2/2015
Test Time: -
Test Location: A314
Test Objective: To ensure that the transmit signal from the going into the LO port of the IQ demodulator is pulsing at 40nS and the period is approximately 65nS.
Requirements:

- Assembled LO IQ demodulator chain
- 1- RF Signal Generator (>10 GHz, >-4dBm)
- 1- Spectrum Analyzer (>10.5GHz Capability)
- Power supply voltages (see table 1 below)
- 1- Pulse generator
- 2- short RF cables (SMA Connectors), minimal loss
- Attenuator pads (39 dB total)

Part Name	+V (V)	+I (mA)	-V (V)	-I (mA)
Super Ultra Wideband	12	400(max)	-	-
SPDT Switch	5	1.4	-	-
Ultra Wide Bandwidth Amplifier	12	62	-	-

Table 1: Power Supply Requirements

Procedure:

1. Connect the output of the RF signal generator to the input of the spectrum analyzer using a short RF cable.
2. Put the spectrum analyzer in output power mode. Use the peak power search function. Note the power and frequency of the spectral line shown on the screen.
3. Set the RF signal generator to generate a pulse such that the measured signal on the spectrum analyzer shows an amplitude of -4 dBm and frequency of 5 GHz.
4. Disconnect the end of that cable that is connected to the analyzer and connect it to the input of the super ultra wide bandwidth amplifier.
5. Connect the RF Out connector on the 3dB pad (connected to the ultrawide bandwidth amplifier) to the input of the attenuator pads using the short RF cable.
6. Connect the output of the pads to the input of the analyzer.
7. Pulse generator/SPDT: connect the positive terminal to the CTL pin and the ground terminal to the GND pin. Input the following settings:
    a. Amplitude: 2V
    b. Pulse width: 25nS
    c. Period: 65nS
8. Enable the power supplies in the following order:

a. +12V
b. +5V
c. +12V (ultra wide bandwidth amp)
d. Pulse generator

9. Record the frequency at the peak of the spectral line to the immediate right of the center line on the spectrum analyzer.
10. Record the frequency of the null of the first lobe that contains the center spectral line.
11. Disable the power supplies in this order:
    a. Pulse generator
    b. +12V (ultra wide bandwidth amp)
    c. +5V
    d. +12V

Results:

In order to measure the period of the pulse using the spectrum analyzer, one must measure the frequency of the spectral lines (not the center frequency). Marker 1 in figure 1 shows that the first spectral line to the right of the center frequency is 15 MHz. This shows that the period of the pulse is about 66.67 nS. This data is supported by the fact that the Fourier transform of a pulse train is a sinc function and the spectral lines occur at frequencies of the multiples of 1/period. Thus the measured period is close enough to 65nS.

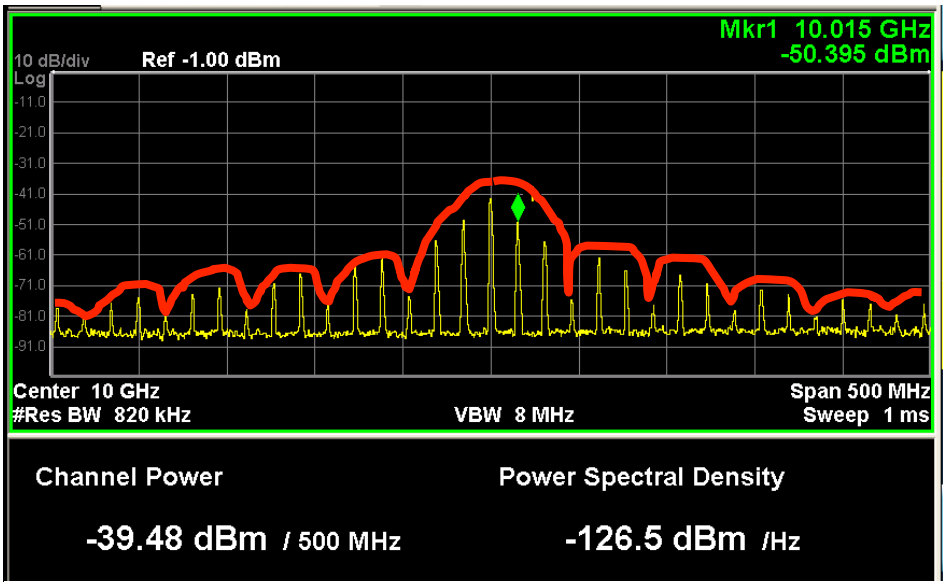


Figure 1: Period of Transmit (LO) Signal

Figure 2 shows the pulse width. As shown in the figure the spectral lines take the shape of a sinc function. The nulls of each lobe in the sinc function are where the frequency of the pulse width occur. The designed pulsed width is 40 nS which is 25 MHz in the frequency domain. As shown if figure 2 marker 1 occurs at about 34 MHz. This is not the designed 40nS.

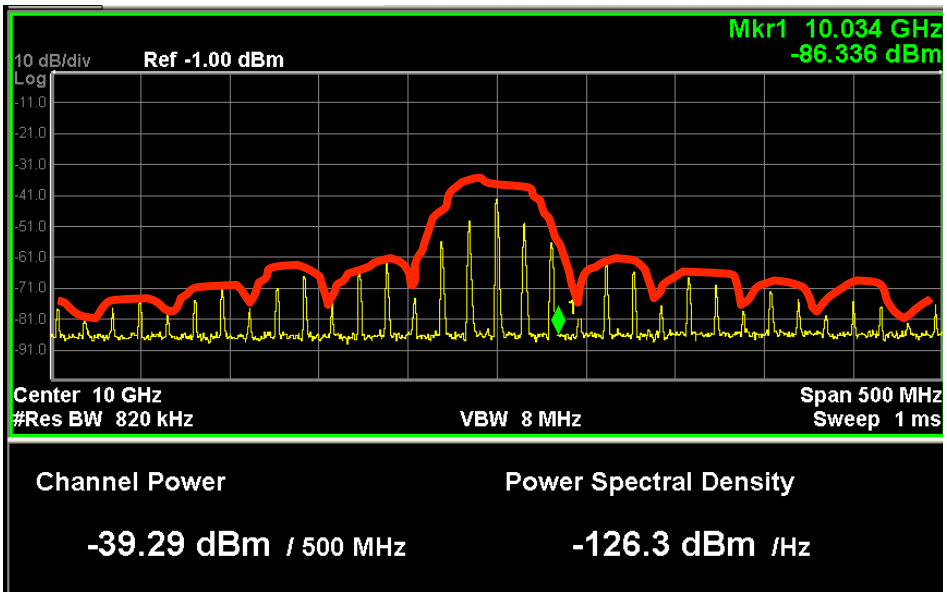


Figure 2: Pulse Width of Transmit Signal

Comments:

The pulse generator was set to a 25nS pulse to account for the rise and fall time in the SPDT switch. The period was set to 65nS to have a LO signal for 40nS. As shown in figure 2 the measured pulse width of the LO transmit chain is about 29nS. To calculate the power of the pulse the equation used was:

Power (dBm) = power/span(dBm) + attenuation(dB) -10*log(duty cycle)

Power Equation

Power/span: -29.37 dBm/500 MHz
Attenuation: 39 dB (pads), 3 dB (cable)
Duty cycle: 40nS/66.6nS
Measured Power: 4.805 dBm
Designed power: 5.599 dBm

13.15 Appendix B15 – Integrated System Test

Scheduled Test Reporting Form

Test Item: Integrated System Test
Tester Name: Joshua Cushion
Test Date: 4/3/2015
Test Time: -
Test Location: CAPS Room 130
Test Objective: To ensure that the voltages read by the FPGA change as the trihedral corner reflector moves along the horizontal and vertical axis in the scene extent. Note it must stay at a distance of 20 feet from the antenna.

Requirements:

- The SAR Imager system fully assembled
- 1- trihedral corner reflector (2in x 2in x 2in)
- A controlled testing room with RF absorbing foam covering the entire room

Procedure:

1. Ensure that variable attenuator in the transmit chain is (12 dB) set such that the transmit signal peak power is as close to 18.954 dBm as possible.
2. Ensure that variable attenuator in the transmit chain is (14 dB).
3. Enable the switching of the SPDT, SP4T, andSP16T switches.
4. Enable the power supplies to turn on the system.
5. Place the trihedral corner reflector at a distance of 20 feet from the antenna structure.
6. Move the reflector along the horizontal and vertical axis while maintaining a distance of 20 feet.
7. Monitor the I and Q channel voltages as the reflector moves.

Results:
As the trihedral moved from side to side at a distance of 20 feet, the I and Q channel voltages changed.

Comments:
The room was not lined with RF absorbing foam. The results are valid but are not accurate.

14 Appendix C – Software

This section shows the code used to run the SAR Imager in the system demonstration. They are separated into different sections for simplicity. Note that the complete set of code used for the project which includes reference code and look up tables this can be checked on the team website. This only includes the code used to run the final demonstration, which is what the students in this team were graded on.

14.1–Main vhd file. Shows the code used for system timing, A/D conversion, and the VGA display.

```
Library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use work.all;


entity TRvia_switch is port(
clk_50,rst: in std_logic;
spdt,pulse: out std_logic;
sw: in std_logic_vector (5 downto 0);
swvga: in std_logic_vector(1 downto 0);
sp4t: out std_logic_vector(3 downto 0);
sp16t: out std_logic_vector(15 downto 0);
pushbuttons,pushbuttons_out,pushbuttons_out2,pushbuttons_out3,pushbuttons_out4: in
std_logic;
--AtoD ports
CS : out std_logic;
CS2: out std_logic;
din : in std_logic; --adc
din2 : in std_logic;
din3 : in std_logic;
din4: in std_logic;
SClk : out std_logic; --adc
SClk2: out std_logic;
--SYNC : out std_logic;

-- seg7  display outputs
anodesa : out std_logic_vector (3 downto 0);
enc_chara : out std_logic_vector (6 downto 0);


--VGA display only stuff
PulseOut: out std_logic;
Hsync : out std_logic ;
```

```
Vsync : out std_logic ;
vgaRed : out std_logic_vector (2 downto 0) ;
vgaGrn : out std_logic_vector (2 downto 0) ;
vgaBlu : out std_logic_vector (1 downto 0)) ;


end TRvia_switch;
--
architecture top of TRvia_switch is
signal temporary : std_logic;
signal temporary2 : std_logic;
signal temporaryout : std_logic;
signal temporaryout2 :  std_logic;
type state_type is (idle, read);
type state_type2 is (idle2, read);
signal state : state_type := read;
signal state2 : state_type2 :=read;
signal data : signed(11 downto 0);  --changed back to signed
signal data2 : signed(11 downto 0);
signal data3 : signed (11 downto 0);
signal data4 : signed (11 downto 0);
--signal data1 : signed(11 downto 0);
signal cnt : integer range 0 to 20 := 0;
signal cnt2 : integer range 0 to 20 :=0;
signal clkdiv : integer range 0 to 6;
signal newclk : std_logic := '0';
signal risingedge : std_logic := '1';
signal reset : std_logic := '0';
--constant A :signed := "0000001" ;

--seg7 Display signals
signal char0a : std_logic_vector (3 downto 0);
signal char1a : std_logic_vector (3 downto 0);
signal char2a : std_logic_vector (3 downto 0);
signal char3a : std_logic_vector (3 downto 0);

signal dataSL : std_logic_vector (11 downto 0);
signal dataSL2 : std_logic_vector (11 downto 0);
signal dataSL3 : std_logic_vector (11 downto 0);
signal dataSL4 : std_logic_vector(11 downto 0);

signal temp_data: signed (11 downto 0);
signal temp_data2: signed(11 downto 0);
signal temp_data3: signed (11 downto 0);
signal temp_data4: signed (11 downto 0);
```

```
--VGA DISPLAY only stuff
--Pulser signals
signal cntr: unsigned (11 downto 0); -- counter value in pulser
signal syncr : std_logic; -- synchronous reset in pulser
signal MaxCounter : unsigned ( 11 downto 0); --8 bits for the 8 slider switches

--VGA signals
signal cntr1v : unsigned (1 downto 0);
signal cntr2v : unsigned (9 downto 0);
signal cntr3v : unsigned (9 downto 0);

signal syncr1v : std_logic;
signal syncr2v : std_logic;
signal syncr3v : std_logic ;

signal en25 : std_logic;
signal Horizontal_Counter  : unsigned(9 downto 0);
signal vertical_counter : unsigned (9 downto 0);
signal vgaRedT : std_logic;
signal vgaGrnT : std_logic ;
signal vgaBluT : std_logic;
----
signal PulseOut_fordata : std_logic;
signal PulseOut_fordata2: std_logic;
signal PulseOut_fordata3: std_logic;
signal PulseOut_fordata4: std_logic;

signal cntr1a : unsigned(25 downto 0);
signal load : unsigned(1 downto 0);
signal syncr1 : std_logic;
signal hzpulse : std_logic;
signal switchprac: std_logic_vector (7 downto 0);




begin
-----------------------------------------instantiation of the seg7_driver
```

```
Inst1: entity seg7_driver port map (
clk50=>clk_50, rst=>pushbuttons, char0=>char0a, char1=>char1a, char2=>char2a,
char3=>char3a,
anodes=>anodesa, enc_char=>enc_chara);
-----------------------------------------------------drive the adc  clock pins
SClk <= newclk;
SClk2<= newclk;
--data1<= data - ("000001")*A;
dataSL<=std_logic_vector(data);
dataSL2<=std_logic_vector(data2);
dataSL3<=std_logic_vector(data3);
dataSL4<=std_logic_vector(data4);



        ----------making the 2000 ns clock for spdt

        process(clk_50, rst)
        variable count : integer :=0;
        variable temp : std_logic :='0';
        begin

                if rst='1' then
                count :=0;
                temp :='0';
                elsif rising_edge(clk_50) then
                count:=count+1;
                        if(count=200) then
                        temp:=not temp;
                        count:=0;
                        end if;
                end if;
                temporary <= temp;
        end process;
        spdt <=temporary;


process(sw)
begin

if (sw="000000")
 then
sp4t<="1111";    --might have to  change this back to 0000 to get it working.
sp16t<="1111111111111111";
end if;
```

```
--first horizontal direction   starts at t0r0-t0r7
if(sw="000001")                  then
sp4t<="1110";
sp16t<="1111111111111110";
elsif(sw="000010")    then
sp4t<="1110";
sp16t<="1111111111111101";
elsif(sw="000011")    then
sp4t<="1110";
sp16t<="1111111111111011";
elsif(sw="000100")    then
sp4t<="1110";
sp16t<="1111111111110111";
elsif(sw="000101")    then
sp4t<="1110";
sp16t<="1111111111101111";
elsif(sw="000110")    then
sp4t<="1110";
sp16t<="1111111111011111";
elsif(sw="000111")    then
sp4t<="1110";
sp16t<="1111111110111111";
elsif(sw="001000")    then
sp4t<="1110";
sp16t<="1111111101111111";

------Other horizontal direction    t1r7-t1r0
elsif(sw="001001")               then
sp4t<="1101";
sp16t<="1111111101111111";
elsif(sw="001010")    then
sp4t<="1101";
sp16t<="1111111110111111";
elsif(sw="001011")    then
sp4t<="1101";
sp16t<="1111111111011111";
elsif(sw="001100")    then
sp4t<="1101";
sp16t<="1111111111101111";
elsif(sw="001101")    then
sp4t<="1101";
sp16t<="1111111111110111";
elsif(sw="001110")    then
sp4t<="1101";
sp16t<="1111111111111011";
```

```
elsif(sw="001111")    then
sp4t<="1101";
sp16t<="1111111111111101";
elsif(sw="010000")    then
sp4t<="1101";
sp16t<="1111111111111110";


--vertical direction   t2r8-t2r15


elsif(sw="010001")    then
sp4t<="1011";
sp16t<="1111111011111111";
elsif(sw="010010")    then
sp4t<="1011";
sp16t<="1111110111111111";
elsif(sw="10011")      then
sp4t<="1011";
sp16t<="1111101111111111";
elsif(sw="010100")    then
sp4t<="1011";
sp16t<="1111011111111111";
elsif(sw="010101")    then
sp4t<="1011";
sp16t<="1110111111111111";
elsif(sw="010110")    then
sp4t<="1011";
sp16t<="1101111111111111";
elsif(sw="010111")    then
sp4t<="1011";
sp16t<="1011111111111111";
elsif(sw="011000")              then
sp4t<="1011";
sp16t<="0111111111111111";

--other vertical direction   t3r15-t3r8

elsif(sw="011001")    then
sp4t<="0111";
sp16t<="0111111111111111";
elsif(sw="011010")    then
sp4t<="0111";
sp16t<="1011111111111111";
elsif(sw="011011")    then
sp4t<="0111";
```

```
sp16t<="1101111111111111";
elsif(sw="011100")    then
sp4t<="0111";
sp16t<="1110111111111111";
elsif(sw="011101")    then
sp4t<="0111";
sp16t<="1111011111111111";
elsif(sw="011110")    then
sp4t<="0111";
sp16t<="1111101111111111";
elsif(sw="011111")    then
sp4t<="0111";
sp16t<="1111110111111111";
elsif(sw="100000")    then
sp4t<="0111";
sp16t<="1111111011111111";

else null;

end if;



--this is where the a/d data gets stored.  Signal processing from these signals.
                temp_data <=data;
                temp_data2 <=data2;
                temp_data3 <=data3;
                temp_data4 <=data4;
end process;


----------clock divider
clock_divider: process(clk_50, pushbuttons)
begin
if(pushbuttons = '1') then
elsif(rising_edge(clk_50)) then
if(clkdiv = 5) then
risingedge <= risingedge xor '1';
newclk <= newclk xor '1';
clkdiv <= 0;
else
clkdiv <= clkdiv + 1;
end if;
end if;
end process clock_divider;
```

```
----------send pusbutton values to seg7 display
Process ( clk_50, pushbuttons)
begin

if (pushbuttons='1') then
 char0a<= (others =>'0');
 char1a<= (others =>'0');
 char2a<= (others =>'0');
 char3a<= (others =>'0');
elsif(rising_edge(clk_50)) then
 -- if (pushbutton(1)='1')then

          if (pushbuttons_out='1') then
  char0a<= (others =>'0');              --These were switched around
  char1a<= (dataSL(11 downto 8));
  char2a<= (dataSL(7 downto 4));
  char3a<= (dataSL(3 downto 0));

  elsif (pushbuttons_out2='1') then
  char0a<= (others =>'0');
  char1a<= (dataSL2(11 downto 8));
  char2a<= (dataSL2(7 downto 4));
  char3a<= (dataSL2(3 downto 0));

  elsif(pushbuttons_out3='1') then
  char0a<= (others =>'0');
  char1a<= (dataSL3(11 downto 8));
  char2a<= (dataSL3(7 downto 4));
  char3a<= (dataSL3(3 downto 0));

  elsif(pushbuttons_out4='1') then
  char0a<= (others =>'0');
  char1a<= (dataSL4(11 downto 8));
  char2a<= (dataSL4(7 downto 4));
  char3a<= (dataSL4(3 downto 0));

  end if;

end if ;
end process ;

main: process(clk_50, pushbuttons)
variable temp : integer;
begin
if(pushbuttons = '1') then
```

```
elsif(rising_edge(clk_50)) then
if(clkdiv = 5 and risingedge = '1') then
case state is
when idle =>
CS <= '1';
--SYNC <= '1';
if(cnt = 15) then
cnt <= 0;
state <= read;
else
cnt <= cnt + 1;
state <= idle;
end if;
when read =>
CS <= '0';
--SYNC <= '1';
cnt <= cnt + 1;
if(cnt < 4) then
cnt <= cnt + 1;
state <= read;
elsif(cnt > 3 and cnt < 16) then
cnt <= cnt + 1;
data2(15 - cnt) <=din2;
data(15 - cnt) <= din;
state <= read;
elsif(cnt = 16) then
cnt <= 0;
state <= idle;
end if;
end case ;
end if ;
end if ;
end process main;



main2: process(clk_50, pushbuttons)
variable temp2 : integer;
begin
if(pushbuttons = '1') then
elsif(rising_edge(clk_50)) then
if(clkdiv = 5 and risingedge = '1') then
case state2 is
when idle2 =>
CS2 <= '1';
--SYNC <= '1';
```

```
if(cnt2 = 15) then
cnt2 <= 0;
state2 <= read;
else
cnt2 <= cnt2 + 1;
state2 <= idle2;
end if;
when read =>
CS2 <= '0';
--SYNC <= '1';
cnt2 <= cnt2 + 1;
if(cnt < 4) then
cnt2 <= cnt2 + 1;
state2 <= read;
elsif(cnt2 > 3 and cnt2 < 16) then
cnt2 <= cnt2 + 1;
data4(15 - cnt2) <= din4;
data3(15 - cnt2) <= din3;
state2 <= read;
elsif(cnt2 = 16) then
cnt2 <= 0;
state2 <= idle2;
end if;
end case ;
end if ;
end if ;
end process main2;


---- process generates 1 hz pulse as switchrate between display values
process(clk_50,rst)
begin
  if (rst='1') then
  cntr1a<=(others=>'0');
  elsif ( rising_edge(clk_50)) then
    if (syncr1='1') then
            cntr1a<=(others=>'0');
            else
            cntr1a<=cntr1a+1;
            end if;
  end if;
 end process;

 syncr1<='1' when (cntr1a= "10111110101111000010000000") else '0';  -- around 50,000,000

 hzpulse<=syncr1;
```

```
-----  2 bit counter that creates sliderswitch load enabled by 1hz pulse

process(clk_50,rst)
begin
if (rst='1') then
load<=(others=>'0');
elsif ( rising_edge(clk_50)) then
if (hzpulse='1') then
load<=load+1;
end if;
end if;
end process;


---------------

process(clk_50,rst)
begin
if (rst='1') then
cntr<=(others=>'0') ;
elsif (rising_edge(clk_50)) then
  if (syncr='1') then
  cntr<=(others=>'0');
  else
  cntr<=cntr+1;
end if;
  end if;
end process;

switchprac<="11110001";

MaxCounter<= "111111111111" ;
syncr<= '1' when (cntr= MaxCounter) else '0';
PulseOut_fordata<= '1' when cntr <= unsigned(data) else '0' ;
PulseOut_fordata2<= '1' when cntr <= unsigned(data2) else '0' ;
PulseOut_fordata3<= '1' when cntr <= unsigned(data3) else '0' ;
PulseOut_fordata4<= '1' when cntr <= unsigned(data4) else '0' ;
PulseOut<= PulseOut_fordata ;
---------------------------Create 25 MHz Clock needed for display
process(clk_50,rst)
begin
 if ((rst='1')) then
  cntr1v<=(others=>'0');
  elsif ( rising_edge(clk_50)) then
```

```
   if (syncr1v='1') then
           cntr1v<=(others=>'0');
           else
           cntr1v<=cntr1v+1;
           end if;
 end if;
end process;

syncr1v<='1' when (cntr1v= "11") else '0';  ---syncr1v<='1' when (cntr1v= "01") else '0';
en25<=syncr1v;  ---used synchronous reset to keep counter going

----------------------Create Horizontal and Vertical Counter
Process (clk_50, rst)
begin
if (rst='1') then
           cntr2v<=(others=>'0');
           cntr3v<=(others=>'0');
           elsif (rising_edge(clk_50)) then

   if (en25='1') then
           cntr2v<=cntr2v+1;
           elsif (cntr2v="1100011111") then----------799
           syncr2v<='1';
           cntr3v<=cntr3v+1;

           elsif (cntr3v="0011001000") then----------520
           syncr3v<='1';

           elsif (syncr2v='1') then
           cntr2v<=(others=>'0');
           syncr2v<='0';
           if (syncr3v='1') then
           cntr3v<= (others=>'0');
           syncr3v<='0';

           end if;
           end if;
           end if;
           end process;

horizontal_counter<=cntr2v;
vertical_counter<=cntr3v;

Hsync<='0' when (horizontal_counter  < "0001100000") else '1';----------96
Vsync<='0' when  (vertical_counter <   "0000000010") else '1';----------2
```

```
vgaRed(0)<=vgaRedT;
vgaRed(1)<=vgaRedT;
vgaRed(2)<=vgaRedT;

vgaGrn(0)<=vgaGrnT;
vgaGrn(1)<=vgaGrnT;
vgaGrn(2)<=vgaGrnT;

vgaBlu(0)<=vgaBluT;
vgaBlu(1)<=vgaBluT;



process(swvga)
begin
if(swvga="00") then
                if(PulseOut_fordata='1') then
                vgaRedT<= '1';
                else vgaRedT<='0';
                end if;
end if;



if(swvga="01") then
                        if(PulseOut_fordata2='1') then
                        vgaGrnT<='1';
                        else vgaGrnT<='0';
                        end if;
end if;


if(swvga="10") then
                        if(PulseOut_fordata3='1') then
                        vgaRedT<='1';
                        else vgaRedT<='0';
                        end if;
end if;


if(swvga="11") then
                        if(PulseOut_fordata4='1') then
                        vgaGrnT<='1';
                        else vgaGrnT<='0';
                        end if;
```

```
end if;
end process;

--vgaRedT<= '1' when PulseOut_fordata='1'  else '0';
--
--vgaGrnT<= '1' when PulseOut_fordata='0'  else '0';

end top;
```

14.2–Display driver for the 7 segment display

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;
use work.all;


entity seg7_driver is
port (
clk50 : in std_logic;
rst : in std_logic;
char0 : in std_logic_vector (3 downto 0);
char1 : in std_logic_vector (3 downto 0);
char2: in std_logic_vector (3 downto 0);
char3 : in std_logic_vector (3 downto 0);
anodes: out std_logic_vector(3 downto 0);


enc_char : out std_logic_vector ( 6 downto 0));

end seg7_driver;

architecture behavioral of seg7_driver is
signal cntr1 : unsigned (15 downto 0);
signal cntr2: unsigned (1 downto 0);
signal syncr1 : std_logic;
signal indecode: std_logic_vector (3 downto 0);
signal khzpulse : std_logic;


begin


----------------------------------------------------------------1khz pulse
process (clk50, rst)
begin

        if(rst='1') then
                cntr1 <= (others=>'0');
        elsif(rising_edge(clk50)) then
                if(syncr1='1') then
                        cntr1 <=(others=>'0');
                else
                        cntr1 <= cntr1 + 1;
```

```
                end if;
        end if;
end process;

syncr1<='1' when (cntr1="1100001101010000") else '0';
khzpulse <=syncr1;



-----------------------------------------------2 bit counter hat creates select for the anodes


process(clk50, rst)
begin

        if (rst='1') then
                cntr2 <= (others=>'0');
                elsif(rising_edge(clk50)) then
                        if(khzpulse ='1') then
                        cntr2 <= cntr2 +1;
                        end if;
                end if;
end process;

---------------------------------anodes turned in scrolling manner on at the 1khz rate

with cntr2 select
anodes <= "1110" when "00",
                        "1101" when "01",
                        "1011" when "10",
                        "0111" when "11",
                        "0000" when others;

with cntr2 select                   --These were switched around
indecode <= char0 when "00",
                                char1 when "01",
                                char2 when "10",
                                char3 when "11",
                                "0000" when others;

-----------------------------------------------------------decode of sliderswitches to display segments

with indecode select
                                enc_char <="1000000" when x"0",
                                                                "1111001" when x"1",
                                                                "0100100" when x"2",
```

```
                                                    "0110000" when x"3",
                                                    "0011001" when x"4",
                                                    "0010010" when x"5",
                                                    "0000010" when x"6",
                                                    "1111000" when x"7",
                                                    "0000000" when x"8",
                                                    "0010000" when x"9",
                                                    "0001000" when x"A",
                                                    "0000011" when x"B",
                                                    "1000110" when x"C",
                                                    "0100001" when x"D",
                                                    "0000110" when x"E",
                                                    "0001110" when x"F",
                                                    "1111111" when others;

end behavioral;
```

14.3–User Constraints File (UCF)

```
net "pushbuttons" loc = "c4";
net "pushbuttons_out" loc="a8";
net "pushbuttons_out2" loc = "b8";
net "pushbuttons_out3" loc = "c9";
net "pushbuttons_out4" loc = "d9";
net "clk_50" loc = "v10";

net "CS" loc = "t12";
net "SClk" loc = "p11";
net "din" loc="v12";
net "din2" loc="n10";


net "CS2" loc="k2";
net "SClk2" loc="l3";
net "din3" loc="k1";
net "din4" loc="l4";


net "spdt" loc="g11";


net "sp4t<0>" loc="h3";
net "sp4t<1>" loc="l7";
net "sp4t<2>" loc="k6";
net "sp4t<3>" loc="g3";


net "sp16t<0>" loc="m10";
net "sp16t<1>" loc="n9";
net "sp16t<2>" loc="u11";
net "sp16t<3>" loc="v11";
net "sp16t<4>" loc="j3";
net "sp16t<5>" loc="j1";
net "sp16t<6>" loc="k3";
net "sp16t<7>" loc="k5";
net "sp16t<8>" loc="g1";
net "sp16t<9>" loc="j7";
net "sp16t<10>" loc="j6";
net "sp16t<11>" loc="f2";
net "sp16t<12>" loc="d12";
net "sp16t<13>" loc="c12";
net "sp16t<14>" loc="f12";
net "sp16t<15>" loc="e12";
```

```
net "sw<0>" loc="t10";
net "sw<1>" loc="t9";
net "sw<2>" loc="v9";
net "sw<3>" loc="m8";
net "sw<4>" loc="n8";
net "sw<5>" loc="u8";


net "anodesa<0>"  loc = "p17";
net "anodesa<1>"  loc = "p18";
net "anodesa<2>"  loc = "n15";
net "anodesa<3>"  loc=  "n16";


net "swvga<0>" loc="v8";
net "swvga<1>" loc="t5";
NET "swvga<0>" CLOCK_DEDICATED_ROUTE = FALSE;


net "enc_chara<0>" loc = "t17";
net "enc_chara<1>" loc = "t18";
net "enc_chara<2>" loc = "u17";
net "enc_chara<3>" loc = "u18";
net "enc_chara<4>" loc = "m14";
net "enc_chara<5>" loc = "n14";
net "enc_chara<6>" loc = "l14";




net "vgaRed<0>" loc = "u7";
net "vgaRed<1>" loc = "v7";
net "vgaRed<2>" loc = "n7";

net "vgaGrn<0>" loc = "p8";
net "vgaGrn<1>" loc = "t6";
net "vgaGrn<2>" loc = "v6";

net "vgaBlu<0>" loc = "r7";
net "vgaBlu<1>" loc = "t7";

net "Hsync" loc = "n6";
net "Vsync" loc = "p7";
```

15 Appendix D – Signal Processing Calculations

In the following calculations for signal processing, the start value for θ is -9° and the end value is 9°, and in order to make it symmetrical for sixteen points, an increment of 1.2 was found. The following Table 26 shows each value for angle θ, both in degrees and radians.

Table 26. Values for the Sixteen Angles

	Degrees	Radians
θ_1	-9	-0.1571
θ_2	-7.8	-0.1361
θ_3	-6.6	-0.1152
θ_4	-5.4	-0.0942
θ_5	-4.2	-0.0733
θ_6	-3	-0.0524
θ_7	-1.8	-0.0314
θ_8	-0.6	-0.0105
θ_9	0.6	0.01047
θ_{10}	1.8	0.03142
θ_{11}	3	0.05236
θ_{12}	4.2	0.0733
θ_{13}	5.4	0.09425
θ_{14}	6.6	0.11519
θ_{15}	7.8	0.13614
θ_{16}	9	0.15708

The spacing between phase centers in radians was found to be $d = 6\pi \approx 18.85$. By replacing these values into the equations, the following Table 27 for the basis functions can be found.

Table 27. Basis Functions for the Sixteen Angles

	1*d*sin(θn)	2*d*sin(θn)	3*d*sin(θn)	4*d*sin(θn)	…	16*d*sin(θn)
f(θ1)	-2.9487202	-5.89744039	-8.84616059	-11.7948808	…	-47.1795231
f(θ2)	-2.55817827	-5.11635654	-7.67453482	-10.2327131	…	-40.9308524
f(θ3)	-2.16651425	-4.33302849	-6.49954274	-8.66605698	…	-34.6642279
f(θ4)	-1.77389991	-3.54779983	-5.32169974	-7.09559966	…	-28.3823986
f(θ5)	-1.38050749	-2.76101498	-4.14152248	-5.52202997	…	-22.0881199
f(θ6)	-0.98650953	-1.97301907	-2.9595286	-3.94603814	…	-15.7841525
f(θ7)	-0.59207886	-1.18415772	-1.77623658	-2.36831544	…	-9.47326176
f(θ8)	-0.19738848	-0.39477696	-0.59216544	-0.78955392	…	-3.15821568
f(θ9)	0.19738848	0.39477696	0.59216544	0.78955392	…	3.15821568
f(θ10)	0.59207886	1.18415772	1.77623658	2.36831544	…	9.47326176

f(θ11)	0.98650953	1.97301907	2.9595286	3.94603814	…	15.7841525
f(θ12)	1.38050749	2.76101498	4.14152248	5.52202997	…	22.0881199
f(θ13)	1.77389991	3.54779983	5.32169974	7.09559966	…	28.3823986
f(θ14)	2.16651425	4.33302849	6.49954274	8.66605698	…	34.6642279
f(θ15)	2.55817827	5.11635654	7.67453482	10.2327131	…	40.9308524
f(θ16)	2.9487202	5.89744039	8.84616059	11.7948808	…	47.1795231

In Figure 53, it can be seen how each of these functions for each angle θ is linear with different slopes.

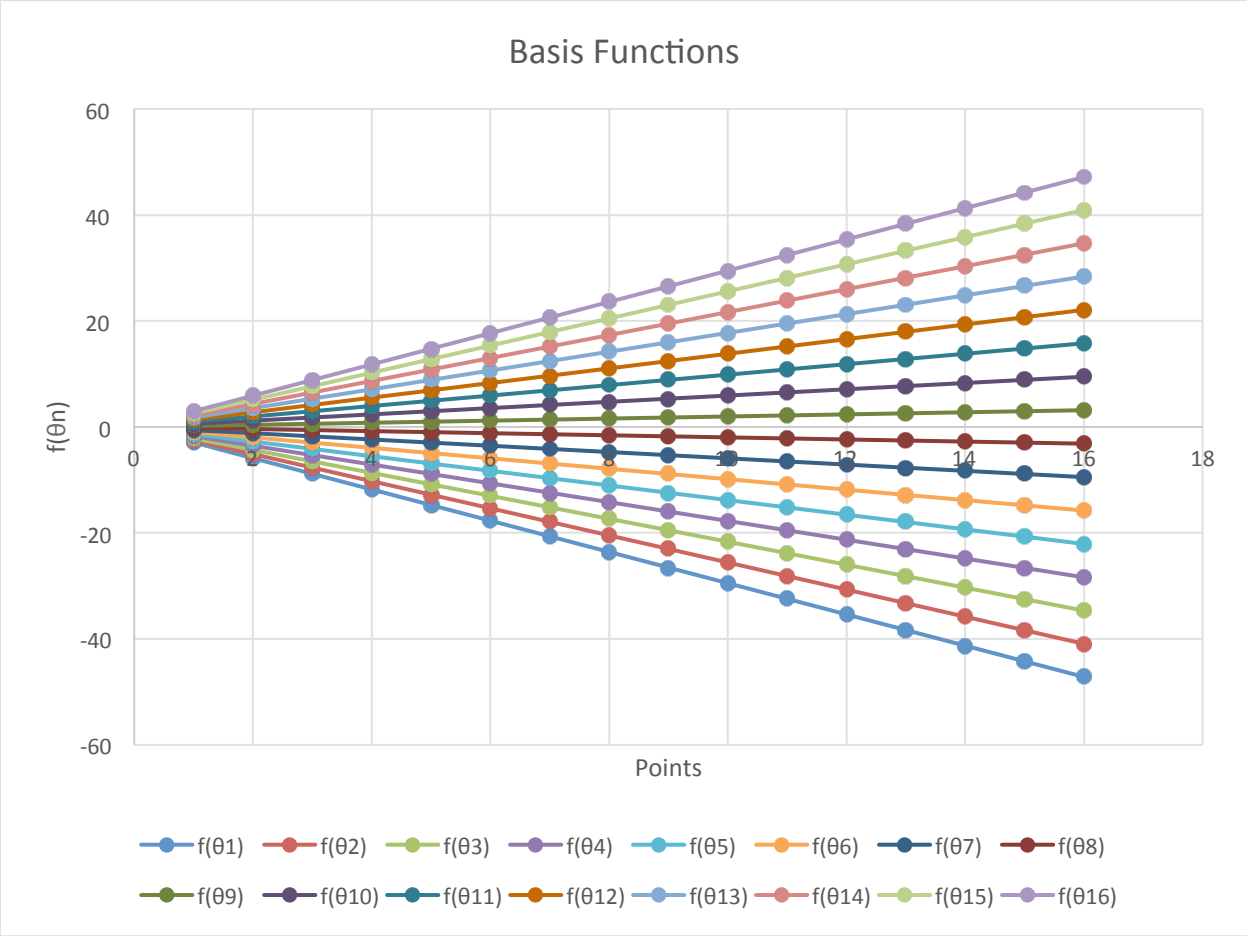


Figure 53. Linear Phase Slope for each function

Each of the functions are then broken into real and imaginary parts. The real part of the basis functions is shown in Table 28, while the imaginary part is shown in Table 29.

Table 28 Real Part of Basis Functions

	cos(1*d*sin(θn))	**cos(2*d*sin(θn))**	**cos(3*d*sin(θn))**	**cos(4*d*sin(θn))**	**…**	**cos(16*d*sin(θn))**
f(realθ_1)	-0.981457696	0.926518416	-0.837219564	0.716872752	…	-0.998452865
f(realθ_2)	-0.834586615	0.393069636	0.178485301	-0.690992523	…	-0.995939433
f(realθ_3)	-0.561103153	-0.370326502	0.97668589	-0.725716563	…	-0.994312023
f(realθ_4)	-0.201710092	-0.918626078	0.572302393	0.687747742	…	-0.994166685
f(realθ_5)	0.189142524	-0.928450211	-0.540361356	0.72403959	…	-0.995301966
f(realθ_6)	0.551604633	-0.391464659	-0.983472071	-0.693510842	…	-0.997099001
f(realθ_7)	0.829782288	0.37707729	-0.203998174	-0.715625434	…	-0.998824891
f(realθ_8)	0.980582064	0.923082369	0.829733965	0.704162119	…	-0.999861841
f(realθ_9)	0.980582064	0.923082369	0.829733965	0.704162119	…	-0.999861841
f(realθ_{10})	0.829782288	0.37707729	-0.203998174	-0.715625434	…	-0.998824891
f(realθ_{11})	0.551604633	-0.391464659	-0.983472071	-0.693510842	…	-0.997099001
f(realθ_{12})	0.189142524	-0.928450211	-0.540361356	0.72403959	…	-0.995301966
f(realθ_{13})	-0.201710092	-0.918626078	0.572302393	0.687747742	…	-0.994166685
f(realθ_{14})	-0.561103153	-0.370326502	0.97668589	-0.725716563	…	-0.994312023
f(realθ_{15})	-0.834586615	0.393069636	0.178485301	-0.690992523	…	-0.995939433
f(realθ_{16})	-0.981457696	0.926518416	-0.837219564	0.716872752	…	-0.998452865

Table 29. Imaginary Part of Basis Functions

	sin(1*d*sin(θn))	**sin(2*d*sin(θn))**	**sin(3*d*sin(θn))**	**sin(4*d*sin(θn))**	**…**	**sin(16*d*sin(θn))**
f(imagθ_1)	-0.191678877	0.376249417	-0.546866895	0.697204028	…	0.055604652
f(imagθ_2)	-0.550876739	0.919508707	-0.983942578	0.722861905	…	0.090025806
f(imagθ_3)	-0.827745886	0.928901653	-0.214673408	-0.687993801	…	0.106506346
f(imagθ_4)	-0.979445271	0.395127991	0.820042664	-0.725949753	…	0.107854544
f(imagθ_5)	-0.981949645	-0.371456868	0.841433066	0.689758416	…	0.096819397
f(imagθ_6)	-0.834105706	-0.920193143	-0.181059895	0.72044619	…	0.076115585
f(imagθ_7)	-0.558087229	-0.926181795	-0.978971269	-0.698484243	…	0.048464803
f(imagθ_8)	-0.196109193	-0.384602315	-0.55815907	-0.710039231	…	0.016622266
f(imag$\theta_{9)}$	0.196109193	0.384602315	0.55815907	0.710039231	…	-0.016622266
f(imagθ_{10})	0.558087229	0.926181795	0.978971269	0.698484243	…	-0.048464803
f(imagθ_{11})	0.834105706	0.920193143	0.181059895	-0.72044619	…	-0.076115585
f(imagθ_{12})	0.981949645	0.371456868	-0.841433066	-0.689758416	…	-0.096819397
f(imagθ_{13})	0.979445271	-0.395127991	-0.820042664	0.725949753	…	-0.107854544
f(imagθ_{14})	0.827745886	-0.928901653	0.214673408	0.687993801	…	-0.106506346
f(imagθ_{15})	0.550876739	-0.919508707	0.983942578	-0.722861905	…	-0.090025806

f(imagθ_{16})	0.191678877	-0.376249417	0.546866895	-0.697204028	…	-0.055604652

In Figure 54 shown below, each row for the sixteen points for each of the sixteen real parts of the basis functions have been plotted out and graphed, and in Figure 55, each row the sixteen points for each of the sixteen imaginary parts of the basis functions have been plotted out and graphed. As can be seen, they are both sinusoidal functions of different frequencies, and the imaginary part is 90° out of phase with the real part.

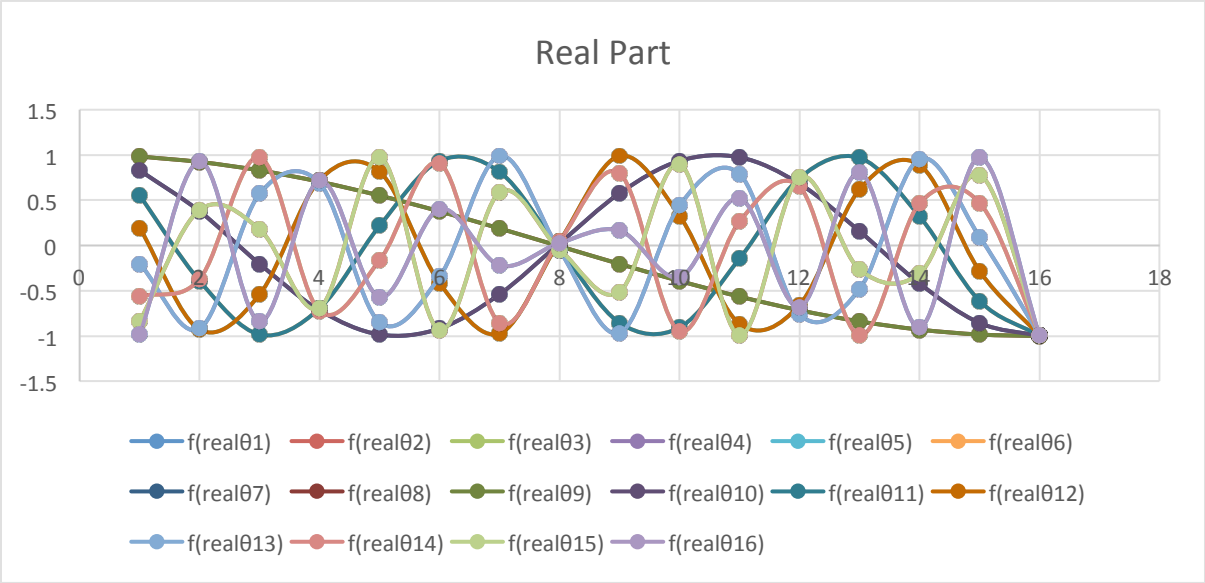


Figure 54. Real Part of the Basis Functions

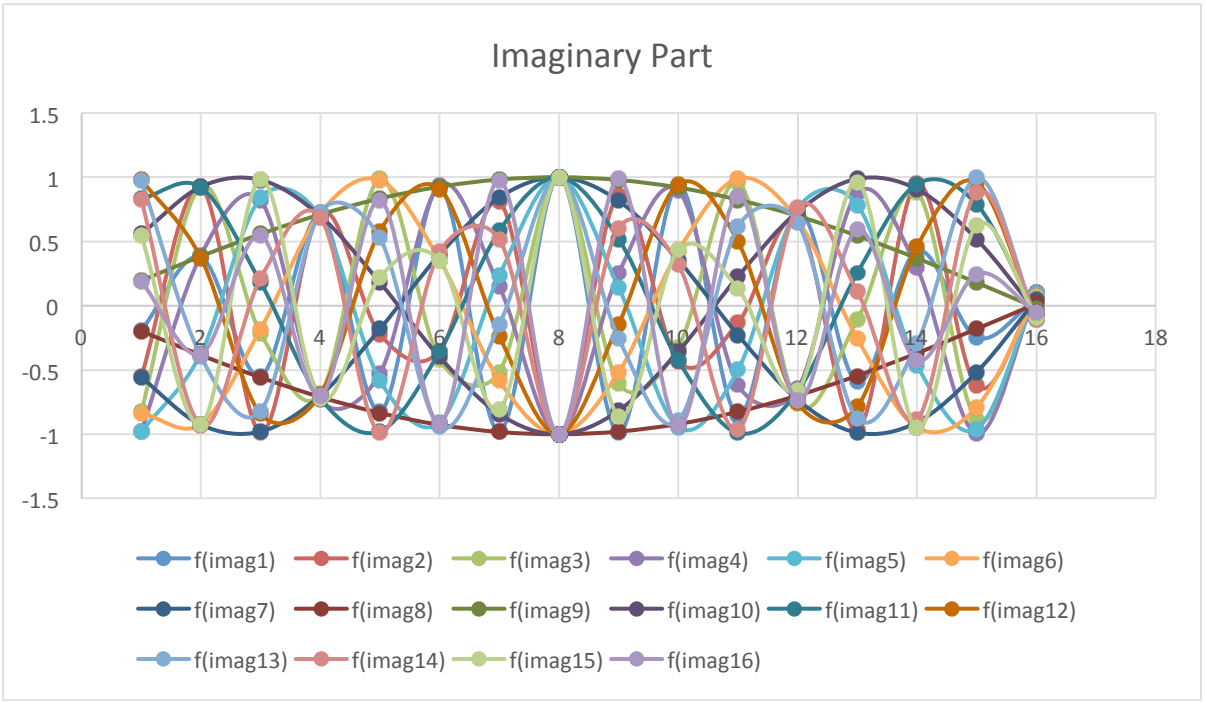


Figure 55. Imaginary Part of Basis Functions

In Table 30 shown below, the calibration data that was calculated from the image processing calibration is used. The error column is the calibration error that was calculated from the image processing calibration. The values for I_{error} are obtained by calculating the cosine of the error, while those of Q_{error} are obtained by calculating the sine of the error. These are calculated in order to get the phase error on the date by taking the error times the ideal phase return. To calculate the values of $I_{combined}$, the following was realized:

$$I_{combined,1} = \left(R_{1,\theta 1} \times I_{error,1}\right) - \left(I_{1,\theta 1} \times Q_{error,1}\right)$$
$$I_{combined,1} = \left[f\left(real\theta_{1,1}\right) \times I_{error,1}\right] - \left[f\left(imag\theta_{1,1}\right) \times Q_{error,1}\right]$$
$$I_{combined,1} = [(-0.981457696) \times (0.97351)] - [(-0.191678877) + (-0.2287)] = -0.9993$$

To calculate the values of $Q_{combined}$, the following was realized:

$$Q_{combined,1} = \left(R_{1,\theta 1} \times Q_{error,1}\right) + \left(I_{1,\theta 1} \times I_{error,1}\right)$$
$$Q_{combined,1} = \left[f\left(real\theta_{1,1}\right) \times Q_{error,1}\right] + \left[f\left(imag\theta_{1,1}\right) \times I_{error,1}\right]$$
$$Q_{combined,1} = [(-0.981457696) \times (-0.2287)] + [(-0.191678877) + (0.97351)] = 0.03782$$

Table 30. I and Q Error Data from Calibration

Error (degrees)	**I_{error} =cos(error)**	**Q_{error} =sin(error)**	**$I_{combined}$**	**$Q_{combined}$**
-13.2183	0.97351	-0.2287	-0.9993	0.03782
-10.0876	0.98454	-0.1752	0.9781	0.20815
-8.41575	0.98923	-0.1464	-0.9082	-0.4184
-7.78614	0.99078	-0.1355	0.80472	0.59366
-7.76778	0.99082	-0.1352	-0.6758	-0.7371
-7.92085	0.99046	-0.1378	0.52423	0.85158
-7.80226	0.99074	-0.1358	-0.3493	-0.937
-6.97141	0.99261	-0.1214	0.14893	0.98885
-3.91578	0.99767	-0.0683	0.09656	-0.9953
-0.78507	0.99991	-0.0137	-0.3375	0.94134
0.88674	0.99988	0.01548	0.53649	-0.8439
1.51636	0.99965	0.02646	-0.6962	0.71781
1.53471	0.99964	0.02678	0.8211	-0.5708
1.38164	0.99971	0.02411	-0.9142	0.40526
1.50024	0.99966	0.02618	0.97539	-0.2205
2.33108	0.99917	0.04067	-0.9999	0.01495

For this example, there is energy coming in from angles θ_4, θ_8, and θ_{13}, so the data from the demodulator would reflect this information. The I data would be the sum of the real part of the basis functions for those angles, which would be the sum of each of the sixteen points of $f(real\theta_4)$, $f(real\theta_8)$, $f(real\theta_{13})$, and the value of $I_{combined,1}$, while the Q data would be the sum of the imaginary part of the basis functions for those angles and the value of $Q_{combined,1}$. Each column of Table 31 shows the I data that sums each of the points for the real part at the specified angles for

the corresponding column, while each column Table 33 shows the Q data that sums each of the points for the imaginary part at the specified angles for the corresponding column. For example, for column 1 in Table 32 below, it shows the following sum for f($I\theta_1$) through f($I\theta_{16}$):

$$f(I\theta_{n,1}) = (\cos(1 * d * \sin(\theta_4))) + (\cos(1 * d * \sin(\theta_8))) + (\cos(1 * d * \sin(\theta_{13}))) + I_{combined,1}$$

$$f(I\theta_{n,1}) = (-0.2017101) + (0.98058206) + (-0.2017101) + (-0.9993) = -0.422123$$

The same is done for column 1 in Table 32 below, which shows the following sum for f($Q\theta_1$) through f($Q\theta_{16}$), except with the imaginary part:

$$f(Q\theta_{n,1}) = (\sin(1 * d * \sin(\theta_4))) + (\sin(1 * d * \sin(\theta_8))) + (\sin(1 * d * \sin(\theta_{13}))) + Q_{combined,1}$$

$$f(Q\theta_{n,1}) = (-0.97944527) + (-0.19610919) + (0.97944527) + (0.03782) = -0.158288$$

Table 31. I data with Energy from θ_4, θ_8, and θ_{13}

	1	2	3	4	…	16
f($I\theta_1$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_2$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_3$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_4$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_5$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_6$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_7$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_8$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_9$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{10}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{11}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{12}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{13}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{14}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{15}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083
f($I\theta_{16}$)	-0.422123	0.063927	1.0660976	2.8843756	…	-3.988083

Table 32. Q data with Energy from θ_4, θ_8, and θ_{13}

	1	2	3	4	…	16
f($Q\theta_1$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f($Q\theta_2$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f($Q\theta_3$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157

f(Qθ$_4$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_5$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_6$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_7$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_8$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_9$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{10}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{11}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{12}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{13}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{14}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{15}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157
f(Qθ$_{16}$)	-0.158288	-0.176452	-0.976606	-0.116382	…	0.03157

Now that there is data for the I channel and the Q channel at the angles specified, they will be used to perform a complex multiplication for each of the points for the sixteen angles. Table 33 shows the results of the complex multiply realized for each point for the real part. For example, for point 1 of f(realcompθ$_1$), which is the complex multiply for the real part of θ$_1$, the following was performed:

$$f(realcomp\theta_{1,1}) = (R_{1,\theta1}\times I_{1d}) + (I_{1,\theta1}\times Q_{1d})$$
$$f(realcomp\theta_{1,1}) = [f(real\theta_{1,1})\times f(I\theta_{1,1})] + [f(imag\theta_{1,1})\times f(Q\theta_{1,1})]$$
$$f(realcomp\theta_{1,1}) = [(-0.981457696)(-0.422123)] + [(-0.19167888)(-0.158288)]$$
$$= 0.44463604$$

Table 33. Real Part after Complex Multiply

	1	2	3	4	…	16
f(realcompθ$_1$)	0.44463604	-0.007160336	-0.358484174	1.986588305	…	3.983668821
f(realcompθ$_2$)	0.439495233	-0.137121243	1.151207091	-2.077210003	…	3.974731723
f(realcompθ$_3$)	0.367876803	-0.187580296	1.250893807	-2.013169082	…	3.968761765
f(realcompθ$_4$)	0.240181082	-0.128446106	-0.190728505	2.068210205	…	3.968224709
f(realcompθ$_5$)	0.075589753	0.006191188	-1.397826607	2.008126692	…	3.972403926
f(realcompθ$_6$)	-0.100815673	0.137344615	-0.871652971	-2.084192635	…	3.97891703
f(realcompθ$_7$)	-0.261931246	0.18753193	0.738587381	-1.982841577	…	3.984927088
f(realcompθ$_8$)	-0.382884119	0.126873709	1.42967892	2.113703737	…	3.988057261
f(realcompθ$_9$)	-0.444967683	-0.008853876	0.339475788	1.94843228	…	3.98700773
f(realcompθ$_{10}$)	-0.438608554	-0.139321065	-1.173551291	-2.145423451	…	3.981867019
f(realcompθ$_{11}$)	-0.364873947	-0.187394963	-1.225301375	-1.916498815	…	3.97411109
f(realcompθ$_{12}$)	-0.23527244	-0.124897321	0.245670763	2.168677509	…	3.966290747
f(realcompθ$_{13}$)	-0.069888284	0.010996029	1.410988871	1.899235353	…	3.961414769

f(realcompθ_{14})	0.105831899	0.140232547	0.831591077	-2.17330916	…	3.962036951
f(realcompθ_{15})	0.265100597	0.187376794	-0.770641603	-1.908953891	…	3.969047491
f(realcompθ_{16})	0.38395501	0.125619481	-1.426631292	2.148872191	…	3.980157941

Table 34 shows the results of the complex multiply realized for each point for the imaginary part. For example, for point 1 of f(realcompθ_1), which is the complex multiply for the real part of θ_1, the following was performed:

$$f(imagcomp\theta_{1,1}) = (-I_{1,\theta1} \times I_{1d}) + (R_{1,\theta1} \times Q_{1d})$$
$$f(imagcomp\theta_{1,1}) = [(-f(imag\theta_{1,1})) \times f(I\theta_{1,1})] + [f(real\theta_{1,1}) \times f(Q\theta_{1,1})]$$
$$f(imagcomp\theta_{1,1}) = [(-(-0.19167888))(-0.422123)] + [(-0.981457696)(-0.158288)]$$
$$= 0.074441231$$

Table 34. Imaginary Part after Complex Multiply

	1	2	3	4	…	16
f(imagcompθ_1)	0.074441231	-0.187538404	1.400647215	-2.094429289	…	0.190234821
f(imagcompθ_2)	-0.100432291	-0.12813933	0.874668942	-2.004586177	…	0.327588605
f(imagcompθ_3)	-0.260594249	0.005962873	-0.724974625	2.068892793	…	0.393365752
f(imagcompθ_4)	-0.381517697	0.136833917	-1.433159503	2.013870325	…	0.398747068
f(imagcompθ_5)	-0.444442228	0.187572899	-0.369329528	-2.073787435	…	0.354702139
f(imagcompθ_6)	-0.439407448	0.127899882	1.153492359	-1.997325261	…	0.272076878
f(imagcompθ_7)	-0.366926052	-0.007327935	1.242904745	2.097976744	…	0.161748763
f(imagcompθ_8)	-0.237996757	-0.138293114	-0.21527125	1.966068068	…	0.034725329
f(imagcompθ_9)	-0.072432492	-0.187466083	-1.405375293	-2.129971546	…	-0.097856637
f(imagcompθ_{10})	0.10423647	-0.125744041	-0.844453013	-1.931405021	…	-0.224814598
f(imagcompθ_{11})	0.264782378	0.010249449	0.767437335	2.158749506	…	-0.33503374
f(imagcompθ_{12})	0.384564148	0.140080629	1.424769946	1.905257201	…	-0.417545536
f(imagcompθ_{13})	0.445374374	0.187352637	0.315331461	-2.17395313	…	-0.461518783
f(imagcompθ_{14})	0.438226328	0.124726725	-1.182700218	-1.899972219	…	-0.456146644
f(imagcompθ_{15})	0.364642809	-0.010576405	-1.223288618	2.16542425	…	-0.390472252
f(imagcompθ_{16})	0.236265222	-0.139433386	0.234620292	1.927567235	…	-0.253277166

The sum column of Table 35 shows the sum of all the points for each of the functions for the real part after the complex multiply, while the amplitude column shows the squared value of the sum column and corresponds to the amplitude at that angle for the real part.

Table 35. Amplitude for the Real Part of the Sixteen Functions

	Sum	**Amplitude**
f(reθ_1)	15.772399	248.76857
f(reθ_2)	-1.006651	1.0133455
f(reθ_3)	-0.327206	0.1070634

f(reθ_4)	15.731508	247.48035
f(reθ_5)	-0.10471	0.0109643
f(reθ_6)	0.0179447	0.000322
f(reθ_7)	0.0911412	0.0083067
f(reθ_8)	16.070567	258.26313
f(reθ_9)	0.1798936	0.0323617
f(reθ_{10})	0.1854129	0.0343779
f(reθ_{11})	0.1733442	0.0300482
f(reθ_{12})	0.1410176	0.019886
f(reθ_{13})	16.091311	258.9303
f(reθ_{14})	0.0916746	0.0084042
f(reθ_{15})	-0.067137	0.0045074
f(reθ_{16})	0.4089471	0.1672378

The sum column of Table 36 shows the sum of all the points for each of the functions for the imaginary part after the complex multiply, while the amplitude column shows the squared value of the sum column and corresponds to the amplitude at that angle for the imaginary part.

Table 36. Amplitude for the Imaginary Part of the Sixteen Functions

	Sum	**Amplitude**
f(imθ_1)	-1.068907	1.1425626
f(imθ_2)	0.3490256	0.1218189
f(imθ_3)	0.1009696	0.0101949
f(imθ_4)	0.3704309	0.137219
f(imθ_5)	0.2885457	0.0832586
f(imθ_6)	0.2944188	0.0866825
f(imθ_7)	0.2184722	0.0477301
f(imθ_8)	0.1627602	0.0264909
f(imθ_9)	0.0823559	0.0067825
f(imθ_{10})	0.0201988	0.000408
f(imθ_{11})	-0.05388	0.002903
f(imθ_{12})	-0.08327	0.0069339
f(imθ_{13})	-0.153013	0.0234131
f(imθ_{14})	-0.109271	0.0119401
f(imθ_{15})	-0.307563	0.0945951
f(imθ_{16})	-0.04602	0.0021179

The following Table 37 shows each amplitude that correspond to each of the corresponding sixteen angles by using Equation 20 in which $real_{\theta n}$ represents the amplitude for the real part and $imag_{\theta n}$ represents the amplitude for the imaginary part.

$$A_n = 20\times\log\left[(real_{\theta n} + imag_{\theta n})^{1/2}\right]$$

Equation 20: Amplitude Calculation for Each Angle

Table 37. Corresponding Amplitudes for each Angle

Amplitude	Theta
23.977856	-9
0.5505877	-7.8
-9.308564	-6.6
23.937815	-5.4
-10.25844	-4.2
-10.60458	-3
-12.51527	-1.8
24.12107	-0.6
-14.07332	0.6
-14.58596	1.8
-14.82128	3
-15.71543	4.2
24.132221	5.4
-16.91556	6.6
-10.03916	7.8
-7.712004	9

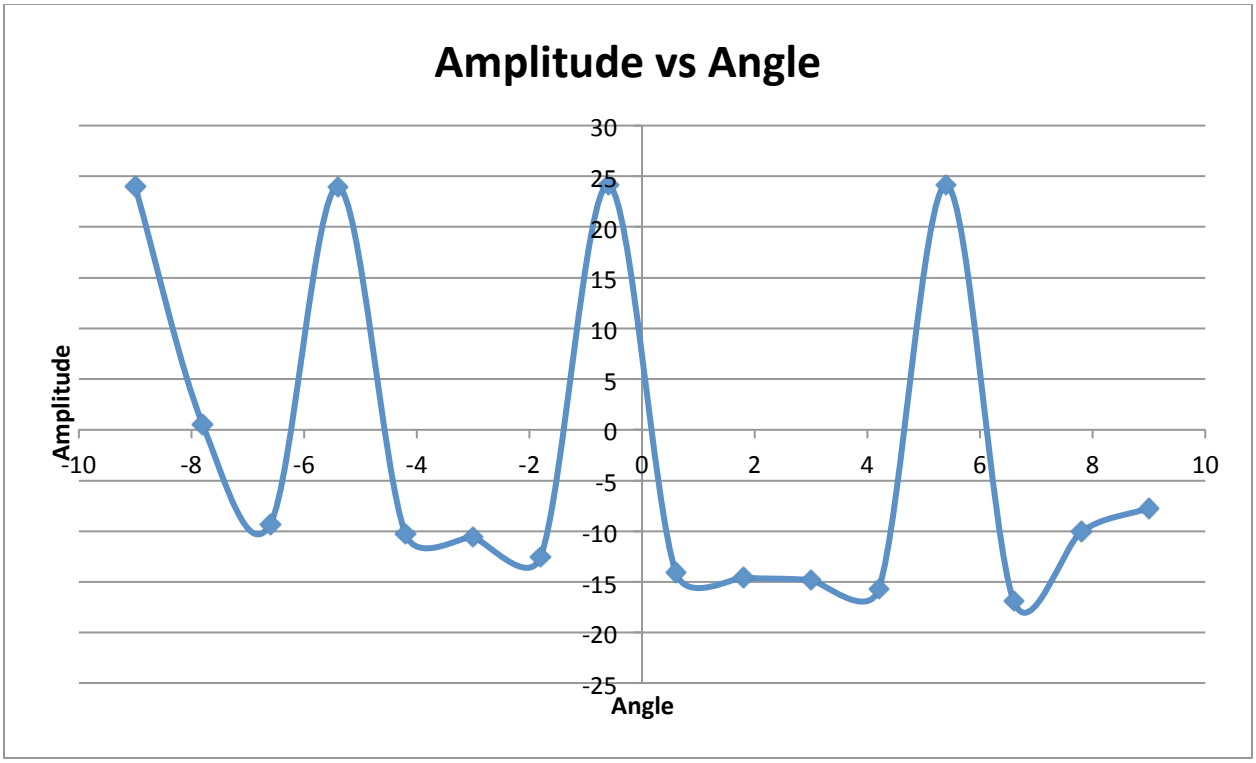
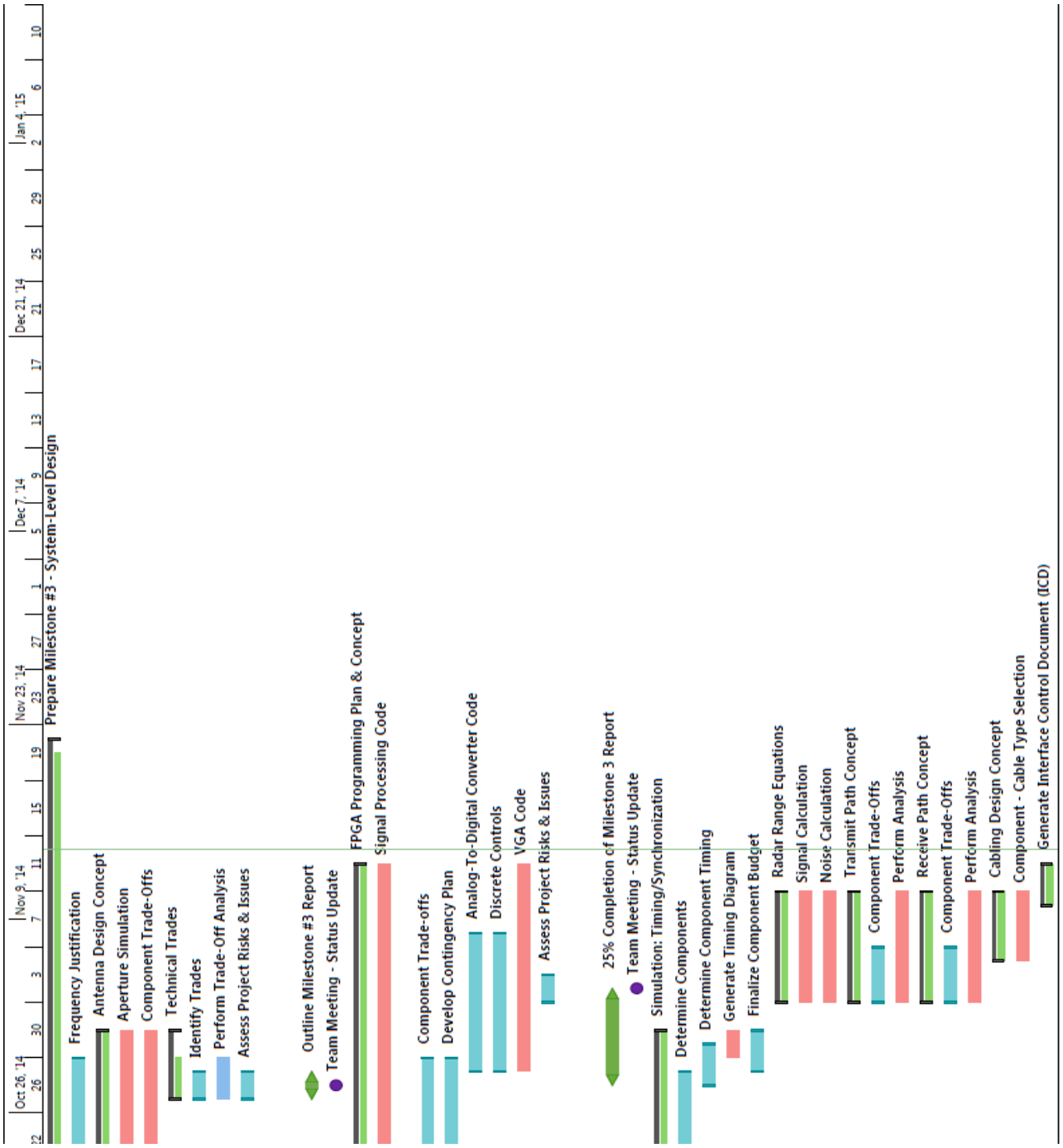


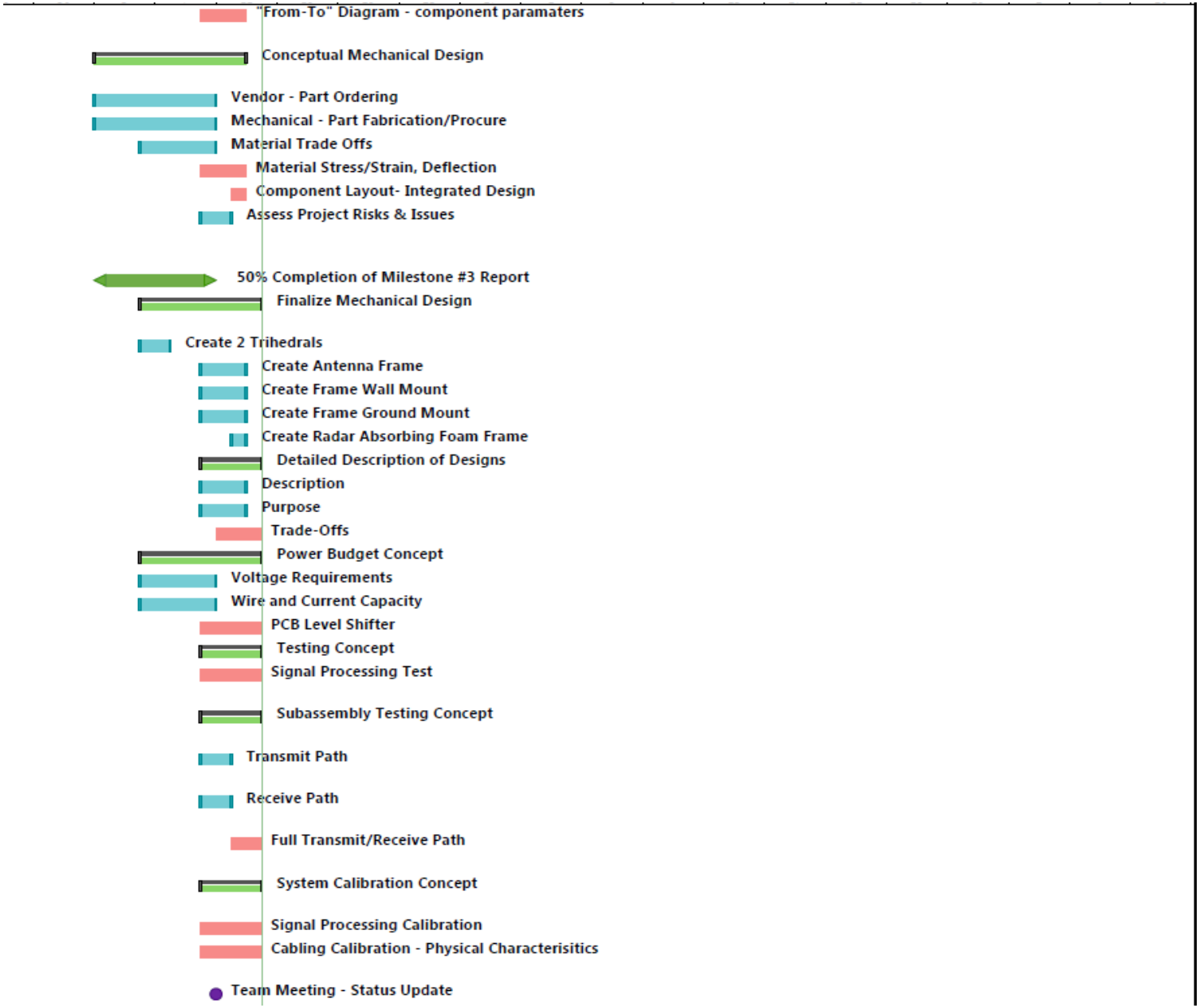
Figure 56. Amplitude vs Angle Graph

Figure 56 shows the graph for the amplitude vs angle that were obtained from all the calculations realized. It is basically the one-dimensional image, which tells the used where the energy is coming in from different angles in the scene. Since there was energy coming in at three different angles for this example, each of the three peaks of the figure represents that information. When forming the image out of the three peaks, the display would have three strikes across it, informing the user that there is energy coming in from those three angles.

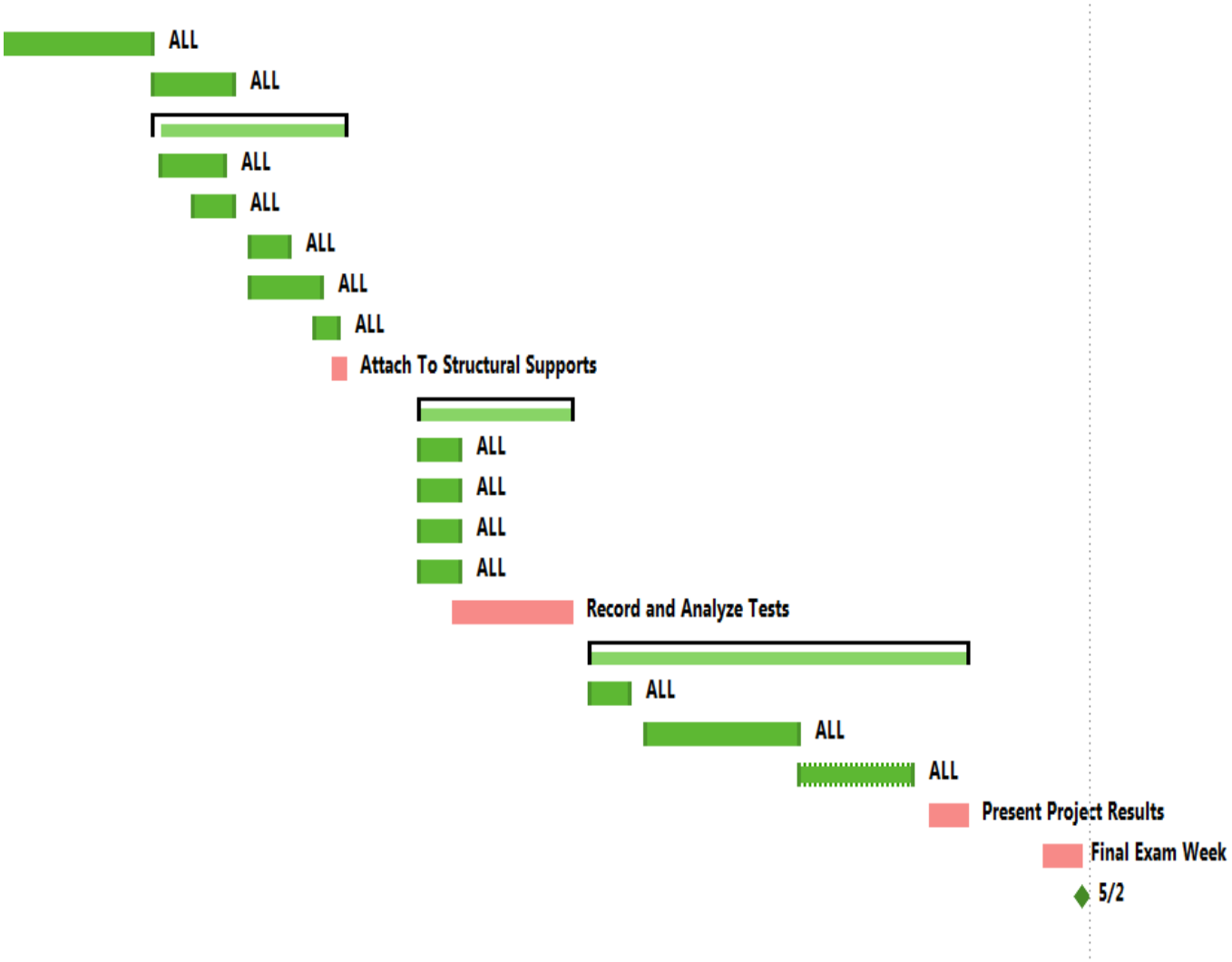
16 Appendix E – Gantt Charts

16.1 Conceptual Design Review Fall 2014 Schedule




"From-To" Diagram - component paramaters
Conceptual Mechanical Design
Vendor - Part Ordering
Mechanical - Part Fabrication/Procure
Material Trade Offs
Material Stress/Strain, Deflection
Component Layout- Integrated Design
Assess Project Risks & Issues
50% Completion of Milestone #3 Report
Finalize Mechanical Design
Create 2 Trihedrals
Create Antenna Frame
Create Frame Wall Mount
Create Frame Ground Mount
Create Radar Absorbing Foam Frame
Detailed Description of Designs
Description
Purpose
Trade-Offs
Power Budget Concept
Voltage Requirements
Wire and Current Capacity
PCB Level Shifter
Testing Concept
Signal Processing Test
Subassembly Testing Concept
Transmit Path
Receive Path
Full Transmit/Receive Path
System Calibration Concept
Signal Processing Calibration
Cabling Calibration - Physical Characterisitics
Team Meeting - Status Update


Final Perfromance Characteristics
100% Completion of Milestone #3 Report
Milestone #3 System-Level Design Final Report Due
Team Meeting - Presentation Prep
Milestone #3 System-Level Design Final Presentation Due
Benjamin Mock
Benjamin Mock
FPGA Board (1 unit)
VCO (1 unit)
Power Amplifier (1 unit)
Wideband Amplifier (1 unit)
Antenna Horns (20 units)
Low Noise Amplifier (1 unit)
Frequency Multiplier (2 units)
SPDT Switch (1 unit)
SP4T Switch (1 unit)
SP16T Switch (1 unit)
Variable Attenuator (3 units)
SA18H-07 (3 units)
SA18H-08 (3 units)
SA18H-09 (3 units)
SA18H-10 (3 units)
IQ Demodulator (1 unit)
Analog-To-Digital Converter (2 units)
Band Pass Filter (2 units)
Isolator (1 unit)
Thanksgiving Break
ALL


ALL
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Attach To Structural Supports
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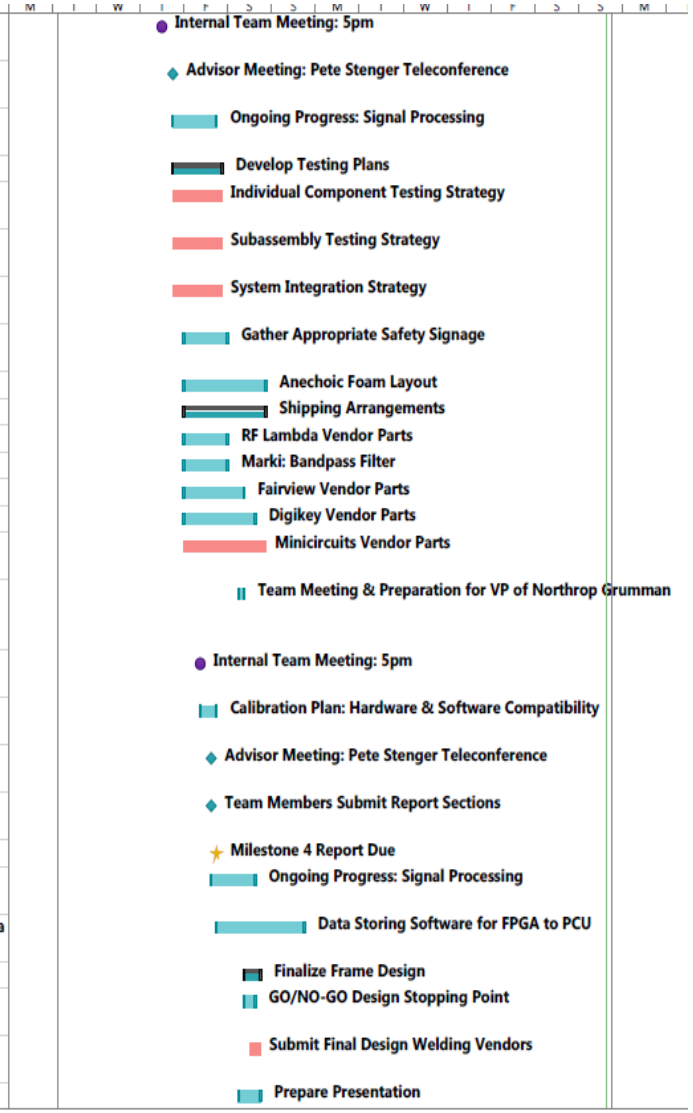
Record and Analyze Tests
ALL
ALL
ALL
Present Project Results
Final Exam Week
5/2

16.2 Final Project Schedule Spring 2015

Begin Spring Semester	0 days	Wed 1/7/15	Wed 1/7/15	**All**
Internal Team Meeting: 5pm	0 days	Mon 1/12/15	Mon 1/12/15	**Jasmine Vanderhorst**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/14/15	Wed 1/14/15	**Pete Stenger,All**
FPGA Programming	9 days	Thu 1/8/15	Tue 1/20/15	**Patrick De La Ilana**
Timing Diagrams	8 days	Thu 1/8/15	Mon 1/19/15	**Patrick De La Ilana**
Waveguide Adapater Selection	10 days	Mon 1/12/15	Fri 1/23/15	**Matthew Cammuse**
Obtain Testing & Storage Facility	15 days	Mon 1/12/15	Fri 1/30/15	**Benjamin Mock,Jasmine Vanderhorst**
Meet with CAPS Safety Coordinator: Michael Coleman	4 days	Mon 1/12/15	Thu 1/15/15	**Benjamin Mock,Jasmine Vanderhorst**
Complete Online Safety Training	7 days	Thu 1/15/15	Fri 1/23/15	**All**
Attend EHS Safety Class	1 day	Fri 1/30/15	Fri 1/30/15	**All**
Identify Problem Items	18 days	Mon 1/12/15	Wed 2/4/15	**Benjamin Mock**
Radar Absorbing Foam	11 days	Mon 1/12/15	Mon 1/26/15	**Matthew Cammuse**
DC Power Supplies	8 days	Mon 1/26/15	Wed 2/4/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 1/19/15	Mon 1/19/15	**Jasmine Vanderhorst**
Frame Design	13 days	Mon 1/19/15	Wed 2/4/15	**Malcolm Harmon,Mark Poindexter**
Stress Analysis	10 days	Mon 1/19/15	Fri 1/30/15	**Malcolm Harmon**
Material Justifications	10 days	Mon 1/19/15	Fri 1/30/15	**Malcolm Harmon**
Component Layout Schematic	5 days	Wed 1/28/15	Tue 2/3/15	**Mark Poindexter**
Obtain Preliminary Frame Welding Price Quote	3 days	Mon 2/2/15	Wed 2/4/15	**Mark Poindexter**
Component Ordering	13 days	Mon 1/19/15	Wed 2/4/15	**Benjamin Mock**
Update Budget	6 days	Mon 1/19/15	Mon 1/26/15	**Benjamin Mock**
Identify Component Risks	7 days	Mon 1/26/15	Tue 2/3/15	**Benjamin Mock**
Level Shift Circuit Design	12 days	Tue 1/20/15	Wed 2/4/15	**Joshua Cushion**
Programming Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La Ilana**
Discrete Code Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La Ilana**
7-Segment Display Descriptions	9 days	Tue 1/20/15	Fri 1/30/15	**Patrick De La Ilana**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 1/21/15	Wed 1/21/15	**Pete Stenger,All**
Ongoing Progress: Signal Processing	6 days	Wed 1/21/15	Wed 1/28/15	**Julia Kim**
Power Supply Design	4 days	Mon 1/26/15	Thu 1/29/15	**Joshua Cushion**

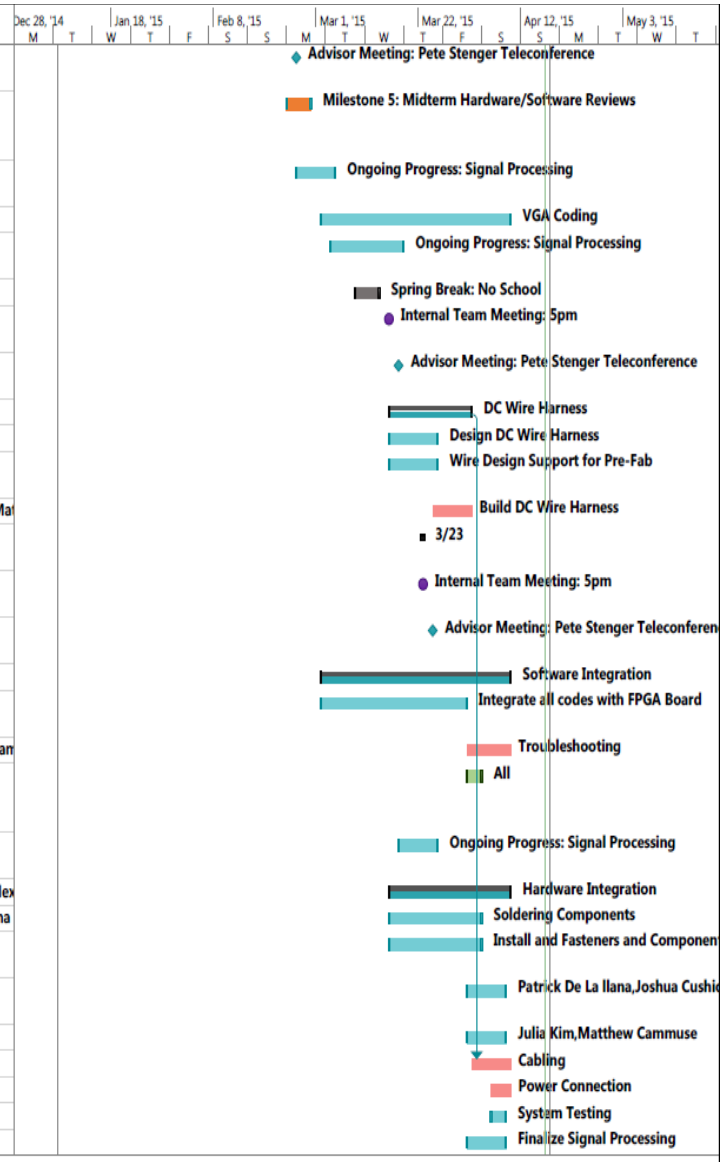
Page 1

rnal Team Meeting: 5pm	0 days	Mon 1/26/15	Mon 1/26/15	Jasmine Vanderhorst	
isor Meeting: Pete nger Teleconference	0 days	Wed 1/28/15	Wed 1/28/15	Pete Stenger,All	
oing Progress: Signal cessing	6 days	Wed 1/28/15	Wed 2/4/15	Julia Kim	
elop Testing Plans	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse	
ndividual Component esting Strategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse	
ubassembly Testing trategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse	
ystem Integration trategy	7 days	Wed 1/28/15	Thu 2/5/15	Matthew Cammuse	
her Appropriate Safety nage	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock	
choic Foam Layout	11 days	Fri 1/30/15	Fri 2/13/15	Matthew Cammuse	
pping Arrangements	11 days	Fri 1/30/15	Fri 2/13/15	Benjamin Mock	
F Lambda Vendor Parts	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock	
Marki: Bandpass Filter	6 days	Fri 1/30/15	Fri 2/6/15	Benjamin Mock	
airview Vendor Parts	7 days	Fri 1/30/15	Mon 2/9/15	Benjamin Mock	
igikey Vendor Parts	9 days	Fri 1/30/15	Wed 2/11/15	Benjamin Mock	
Minicircuits Vendor Parts	11 days	Fri 1/30/15	Fri 2/13/15	Benjamin Mock	
m Meeting & Preparation VP of Northrop Grumman	1 day	Mon 2/9/15	Mon 2/9/15	All	
rnal Team Meeting: 5pm	0 days	Mon 2/2/15	Mon 2/2/15	Jasmine Vanderhorst	
bration Plan: Hardware oftware Compatibility	3 days	Mon 2/2/15	Wed 2/4/15	Joshua Cushion	
isor Meeting: Pete nger Teleconference	0 days	Wed 2/4/15	Wed 2/4/15	Pete Stenger,All	
m Members Submit ort Sections	0 days	Wed 2/4/15	Wed 2/4/15	All	
estone 4 Report Due	0 days	Thu 2/5/15	Thu 2/5/15	All	
oing Progress: Signal cessing	6 days	Wed 2/4/15	Wed 2/11/15	Julia Kim	
a Storing Software for A to PCU	12 days	Thu 2/5/15	Fri 2/20/15	Matthew Cammuse,Patrick De La Ilana	
lize Frame Design	3 days	Tue 2/10/15	Thu 2/12/15	Malcolm Harmon,Mark Poindexter	
iO/NO-GO Design topping Point	2 days	Tue 2/10/15	Wed 2/11/15	Mark Poindexter,Malcolm Harmon,Pete Stenger	
ubmit Final Design Welding Vendors	2 days	Wed 2/11/15	Thu 2/12/15	Malcolm Harmon,Mark Poindexter,Pete Stenger	
pare Presentation	4 days	Mon 2/9/15	Thu 2/12/15	Jasmine Vanderhorst	



Task Name	Duration	Start	Finish	Resource Names
Milestone 4: Detailed Design Review & Test Plan Presentation	5 days	Mon 2/9/15	Fri 2/13/15	**All**
Northrop Grumman VP Visit and Project Update	2 days	Tue 2/10/15	Wed 2/11/15	**Pete Stenger,All**
Programming & Testing	44 days	Mon 2/9/15	Thu 4/9/15	**Patrick De La Ilana**
Analog To Digital Conversion Code	11 days	Mon 2/9/15	Mon 2/23/15	**Patrick De La Ilana**
FPGA Code Simulation and Testing	15 days	Mon 2/16/15	Fri 3/6/15	**Patrick De La Ilana**
Subassembly Testing	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion,Matthew Cammuse**
Transmit Signal and Modulator LO Chain	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion,Matthew Cammuse**
Power Supply Board	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion,Matthew Cammuse**
Data Gathering, Analysis, and Reporting	35 days	Fri 2/20/15	Thu 4/9/15	**Julia Kim**
Miscellaneous Task	35 days	Fri 2/20/15	Thu 4/9/15	**Julia Kim**
Receive Signal Chain	35 days	Fri 2/20/15	Thu 4/9/15	**Joshua Cushion,Matthew Cammuse**
Build Component Box and Attach to Frame	5 days	Mon 2/23/15	Fri 2/27/15	**Mark Poindexter**
Scheduled to Receive Completed Antenna Frame	0 days	Fri 3/6/15	Fri 3/6/15	**Malcolm Harmon**
Actual Structure Received	0 days	Fri 3/20/15	Fri 3/20/15	**Malcolm Harmon,Mark Poindexter**
Transmit and Modulator LO Chain Component Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Matthew Cammuse,Joshua Cushion**
Programming Display Preparation	13 days	Mon 2/9/15	Wed 2/25/15	**Patrick De La Ilana**
Ongoing Progress: Signal Processing	6 days	Wed 2/11/15	Wed 2/18/15	**Julia Kim**
Build Power Supply Board	3 days	Mon 2/16/15	Wed 2/18/15	**Joshua Cushion**
Internal Team Meeting: 5pm	0 days	Mon 2/16/15	Mon 2/16/15	**Jasmine Vanderhorst**
Ongoing Progress: Signal Processing	6 days	Wed 2/18/15	Wed 2/25/15	**Julia Kim**
Advisor Meeting: Pete Stenger Teleconference	0 days	Wed 2/18/15	Wed 2/18/15	**All**
Software Demonstration	5 days	Mon 2/23/15	Fri 2/27/15	**Patrick De La Ilana**
Discrete Code Switch Display	2 days	Mon 2/23/15	Tue 2/24/15	**Patrick De La Ilana**
A-to-D Conversion Display	2 days	Tue 2/24/15	Wed 2/25/15	**Patrick De La Ilana**
Tentative: VGA Imaging Display	2 days	Thu 2/26/15	Fri 2/27/15	**Patrick De La Ilana**
Internal Team Meeting: 5pm	0 days	Mon 2/23/15	Mon 2/23/15	**Jasmine Vanderhorst**

k Name	Duration	Start	Finish	Resource Names
visor Meeting: Pete enger Teleconference	0 days	Wed 2/25/15	Wed 2/25/15	All
lestone 5: Midterm rdware/Software Reviews	5 days	Mon 2/23/15	Fri 2/27/15	All
going Progress: Signal ocessing	6 days	Wed 2/25/15	Wed 3/4/15	Julia Kim
iA Coding	29 days	Mon 3/2/15	Thu 4/9/15	Patrick De La Ilana
going Progress: Signal ocessing	11 days	Wed 3/4/15	Wed 3/18/15	Julia Kim
ring Break: No School	5 days	Mon 3/9/15	Fri 3/13/15	All
ernal Team Meeting: 5pm	0 days	Mon 3/16/15	Mon 3/16/15	Jasmine Vanderhorst
visor Meeting: Pete enger Teleconference	0 days	Wed 3/18/15	Wed 3/18/15	All
Wire Harness	**13 days**	**Mon 3/16/15**	**Wed 4/1/15**	Matthew Cammuse
Design DC Wire Harness	8 days	Mon 3/16/15	Wed 3/25/15	Matthew Cammuse
Wire Design Support for Pre-Fab	8 days	Mon 3/16/15	Wed 3/25/15	Julia Kim
Build DC Wire Harness	6 days	Wed 3/25/15	Wed 4/1/15	Malcolm Harmon,Mark Poindexter,Ma
ceived Fixed Structure om Metal Fabrications	**0 days**	**Mon 3/23/15**	**Mon 3/23/15**	Malcolm Harmon,Mark Poindexter
ernal Team Meeting: 5pm	0 days	Mon 3/23/15	Mon 3/23/15	Jasmine Vanderhorst
visor Meeting: Pete enger Teleconference	0 days	Wed 3/25/15	Wed 3/25/15	All
ftware Integration	29 days	Mon 3/2/15	Thu 4/9/15	Patrick De La Ilana
Integrate all codes with FPGA Board	22 days	Mon 3/2/15	Tue 3/31/15	Patrick De La Ilana
Troubleshooting	7 days	Wed 4/1/15	Thu 4/9/15	Joshua Cushion,Julia Kim,Matthew Can
it From Northrop umman Sponsor: Pete enger	3 days	Wed 4/1/15	Fri 4/3/15	All
going Progress: Signal ocessing	6 days	Wed 3/18/15	Wed 3/25/15	Julia Kim
rdware Integration	19 days	Mon 3/16/15	Thu 4/9/15	Joshua Cushion,Julia Kim,Mark Poindex
Soldering Components	15 days	Mon 3/16/15	Fri 4/3/15	Matthew Cammuse,Patrick De La Ilana
Install and Fasteners and Components	15 days	Mon 3/16/15	Fri 4/3/15	Malcolm Harmon,Mark Poindexter
Sync Hardware with Code	6 days	Wed 4/1/15	Wed 4/8/15	Patrick De La Ilana,Joshua Cushion
Troubleshooting	6 days	Wed 4/1/15	Wed 4/8/15	Julia Kim,Matthew Cammuse
Cabling	6 days	Thu 4/2/15	Thu 4/9/15	Mark Poindexter
Power Connection	4 days	Mon 4/6/15	Thu 4/9/15	Matthew Cammuse,Julia Kim
stem Testing	3 days	Mon 4/6/15	Wed 4/8/15	All
alize Signal Processing	6 days	Wed 4/1/15	Wed 4/8/15	Julia Kim



17 Appendix F – Procurement Procedure Guidelines

17.1 Purpose

The purpose of this document will be to advise future members of Senior Design teams on how to successfully order components through the FAMU Foundation account. This guideline will highlight the proper way of contacting vendors, requesting official quotes, and ensuring that all information is gathered appropriately for use with Donna Butka and FAMU accounting.

17.2 Definitions

A **Purchase Order** is a buyer-generated document that authorizes a purchase transaction. When accepted by the seller, it becomes a contract binding on both parties. A purchase order sets forth the descriptions, quantities, prices, discounts, payment terms, dates of performance or shipment, other associated terms and conditions, and identifies a specific seller.
A **Quote** is a formal price estimate for a good or service.

17.3 Quick Tips

Before you consider requesting a Purchase Order to be formed here are some quick tips that you should consider before you purchase any components through FAMU.

1. Florida Agricultural & Mechanical University will only create purchases for items, or groups of items, exceeding a total cost of $100.00. This **does not** include shipping charges, as shipping is generally done through an external company.

2. In the event that an order does not exceed $100.00 it shall be the responsibility of the Senior Design Team to front the cost of the components and apply for reimbursement from the FAMU Foundation. **The FAMU Foundation will only reimburse out-of-pocket purchases made by a FAMU Student**. Therefore these purchases can only be made on a credit or debit card in the name of a FAMU student; not cash purchases.

3. When taking lead time into account for product procurement, it generally takes 1-2 weeks for paperwork to be submitted from the ECE Department through the FAMU Foundation until an order is officially placed with the vendor.

4. Requests need to be signed by the ECE Department Head and FAMU's Provost before a PO can be formed. The Provost typically only signs these types of requests on Tuesdays, this should be planned for accordingly.

5. Consider contacting companies ahead of time to ensure that they accept PO's or require credit checks. This information can expedite changes that may need to be made.

17.4 Procedure for Procurement via Purchase Order

The following list defines the appropriate way to contact vendors and submit the gathered quote for purchasing to Donna Butka.

1. The team will determine which component that they wish to procure, they will search from known electronics manufacturers to ensure that the provided data sheets meet the required specifications for the design. Once the manufacturer, part number, and quantity of components has been determined, that team member will submit a purchase request to the team's Procurement Engineer. The Procurement Engineer will ensure that the team has double check all data sheets before ordering.

2. The Procurement Engineer will attempt to find all distributors for said manufacturer and submit a Request for Quote (RFQ) to each distributor. Depending on the company there will be different methods to accomplish this, but generally this is done via email. An example email is provided below:

   To Whom It May Concern,

   My name is [Insert Name] and I would like to request a formal quote from [Company Name] concerning the components listed below in the completion of an academic Senior Design capstone research project. Note that Florida Agricultural and Mechanical University will submit the appropriate paperwork to prove tax exemption status and have requested if [Company Name] offers a form of academic discount/pricing. Additionally can you provide any lead times associated with the following components and the available shipping options and the associated costs?

   Does [Company Name] accept purchase orders?

   Bill/Ship to:

   ECE Department
   FAMU-FSU College of Engineering
   2525 Pottsdamer Street
   Tallahassee, FL 32301

   Components and quantities:
   ***Part Number:** XXXX*
   ***Qty:** XX*
   ***Description:** Describe the item, and note any special requests here*

   ***Part Number:** XXXX*
   ***Qty:** XX*
   ***Description:** Describe the item, and note any special requests here*

   Thank you for your time,

   [Your Name]

3. Once a quote has been requested, alert the project manager that that task has been completed.

4. When the quote has been received, ensure that the information you requested is correct. Specifically, ensure that they have the billing and shipping address is correct. It is very

common that they bill to FSU, FAMU will not pay for the item unless the above address is correct. ***If they do not accept PO's then an alternate will need to be devised by the team.***

5. Once all quotes for an item have been gathered, share the results with the team and perform a trade-off analysis to ensure that the optimum choice is selected.

6. Email Donna Butka the quote that the team has agreed upon, indicate in the email exactly what you need to order with the exact quantity. Specify the type of shipping, with appropriate planning typical ground shipping is the common method.

7. Donna Butka prefers to have a singular line of contact, the Procurement Engineer, and will provide to them any necessary shipping information once that order has been placed. Do not hesitate to contact her if you are wondering on the status of any part of the ordering process.

8. If shipping includes a tracking number, then add an extra day to the expected delivery date as FAMU will require another whole day to deliver that shipment to the ECE Department. Donna Butka will email the Procurement Engineer when a part has arrived and is ready for pick-up. Try to pick this up as soon as possible, any team member can sign for the item, but this will allow the Procurement Engineer to discuss any topics that they may need to with Donna.