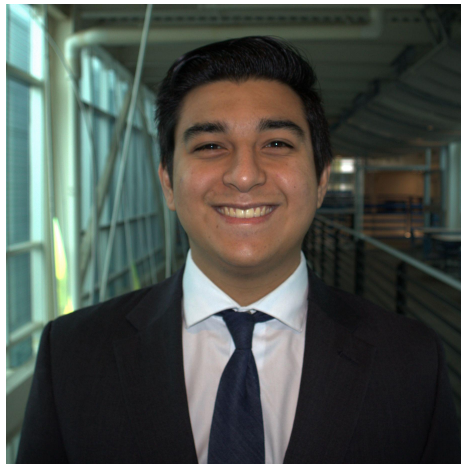
Digital Beamsteering Phased Array

Team 311
Sponsor: L3Harris
March 11th, 2022

Team Introductions

Katheryn Potemken
Financial Advisor / Webmaster

Tiernen Pan
Team Lead / Software Engineer



Christian Balos
Software Engineer

William Snyder
Hardware Engineer

Andrew Cayson
Hardware Lead

Sponsor, Advisors, and Assisting Instructor

Assisting Instructor:
Dr. Arigong

Advisor:
Dr. Uwe Meyer-Baese

Customer:
Dr. Hooker

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Sponsor:
L3Harris

Outline

- Project Background
- Current Progress Update
  - VHDL Coding Implementations
  - PCB design
  - DDS Testing
- Future Work
  - Soldering PCB
  - Intermediate Testing
  - Final Hardware Assembly

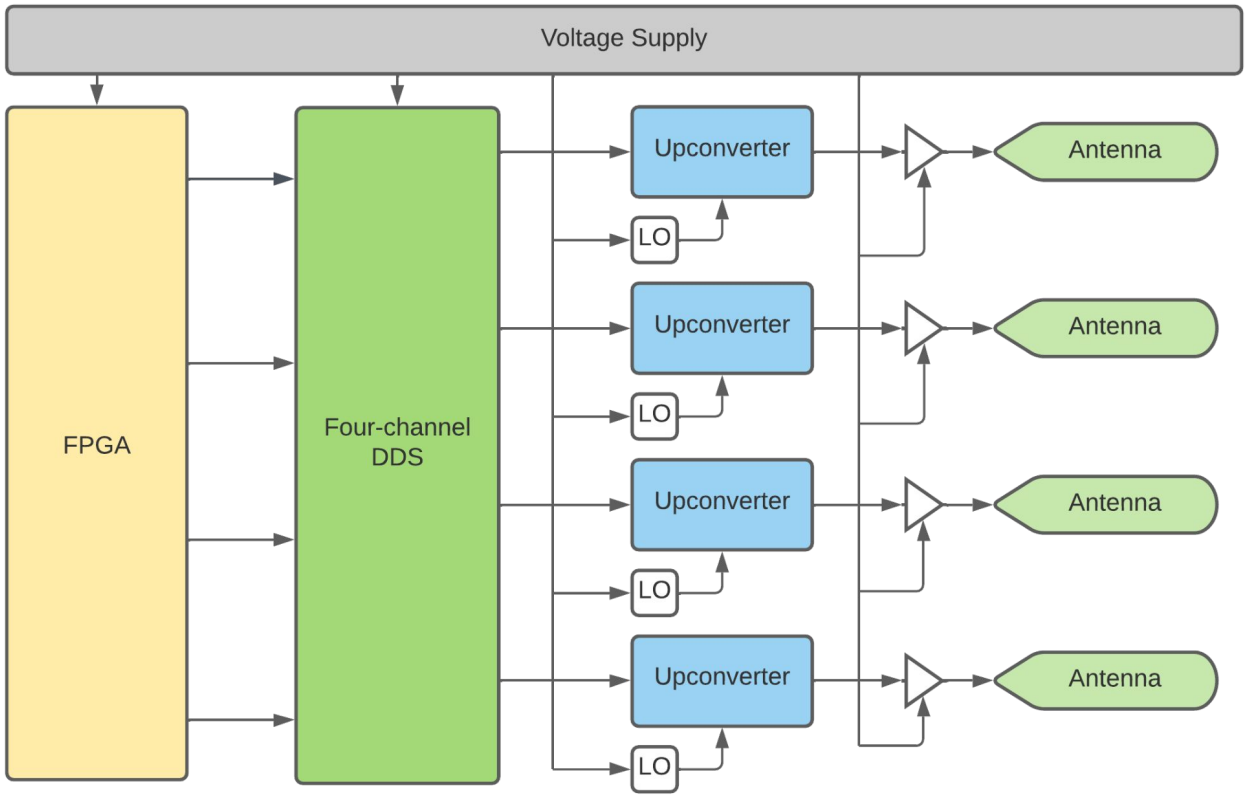
Project Background

- Market
  - Civilian
    - 5G communications
    - Satellite to Ground Communications
  - Military
    - Improving speed and range of Radar Systems
- Purpose of Project
  - Beamsteering allows for high data transmission rates with less errors by focusing the main lobe towards the intended receiver
  - Efficient as the goals above do not need an increase in transmitting power

Project Overview

- The project operates at 2.4 GHz, which is within the ISM band
- Project parts consist of Upconverters, antennas, an FPGA, a DDS, the PCB, Voltage Controlled Oscillators, and Amplifiers
- Through beamsteering, it will allow for the 2.4GHz signal to be transmitted in any given direction inputted by the FPGA.

Components Overview

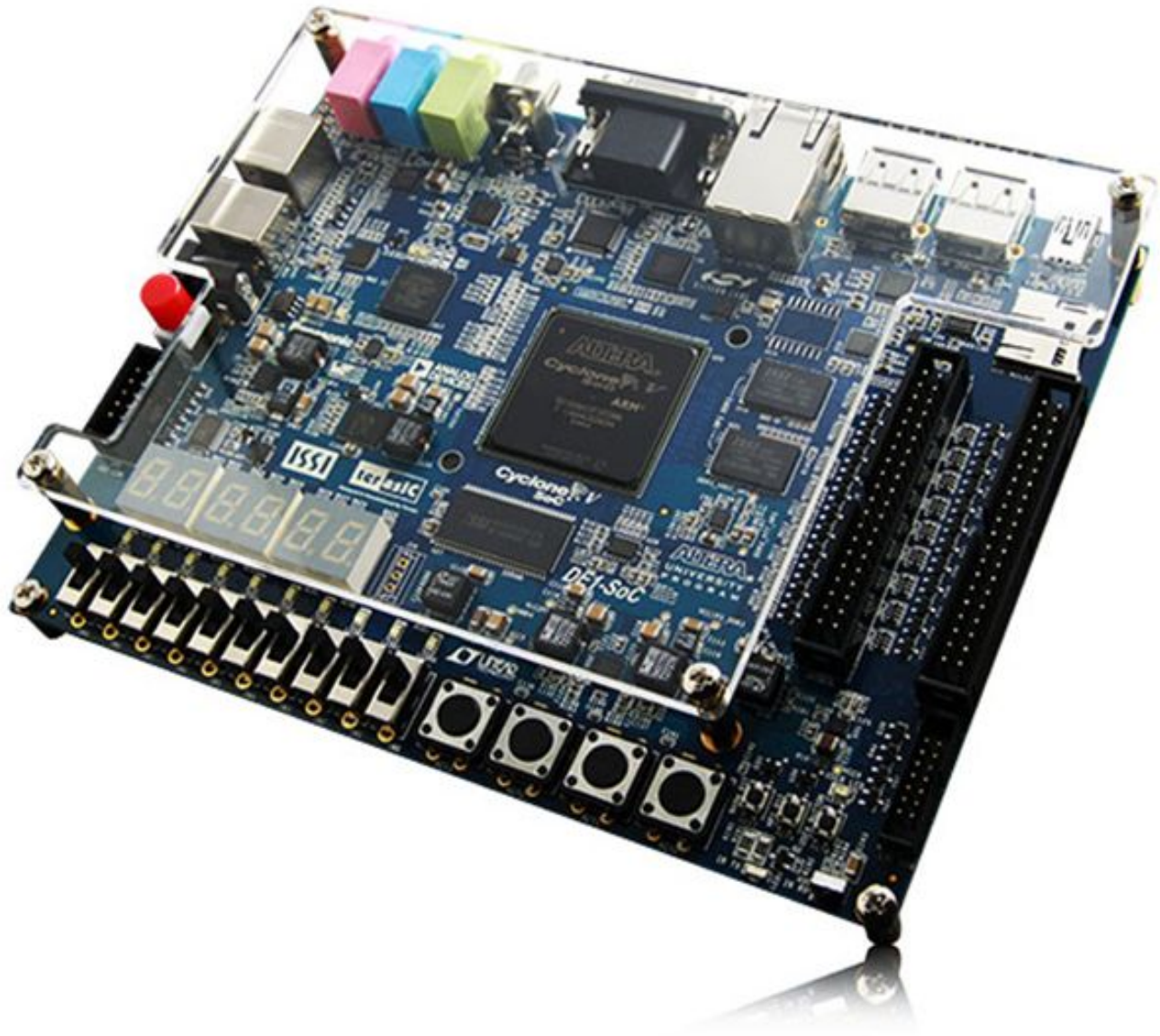


- Buttons on the Cyclone V development board and will serve as inputs for the FPGAs desired beam angle
- The FPGA will then communicate with the DDS via SPI
- The DDS will convert the signal from Digital to Analog and then phase shifted
- Finally, the analog signal will be upconverted to 2.4 GHz and will be transmitted via antenna.

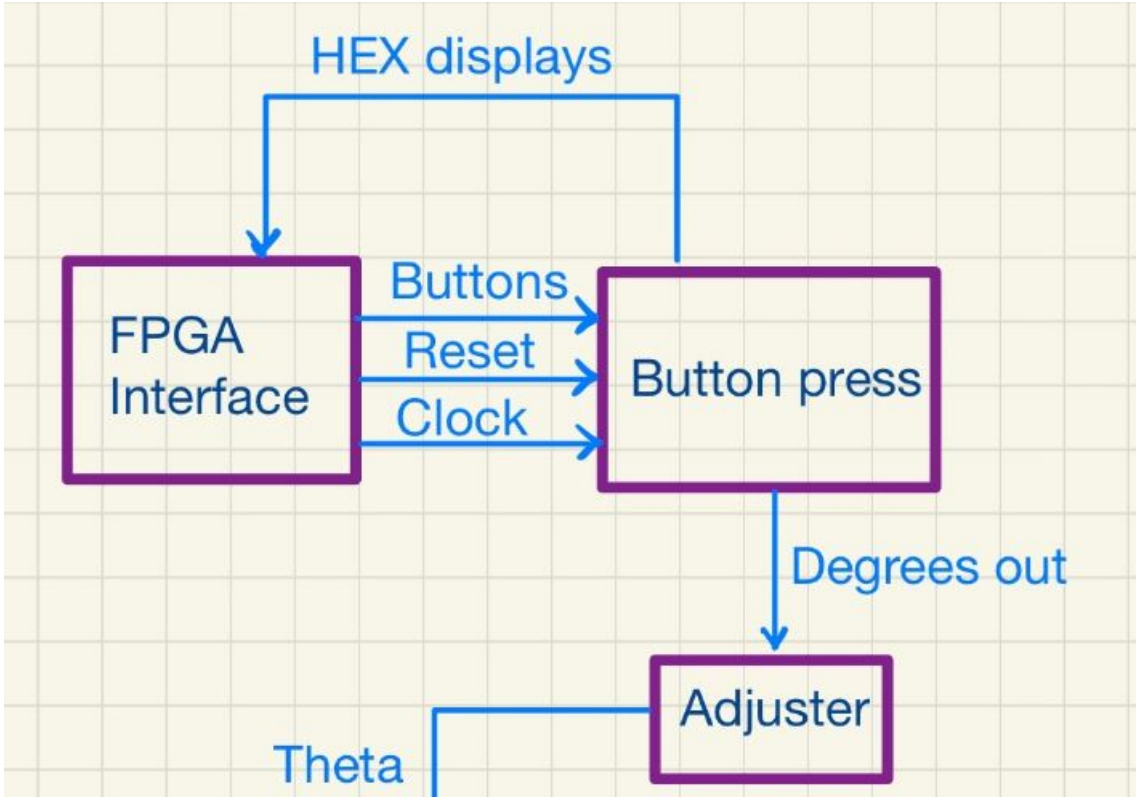
FPGA Interface

Push Buttons and 1 switch

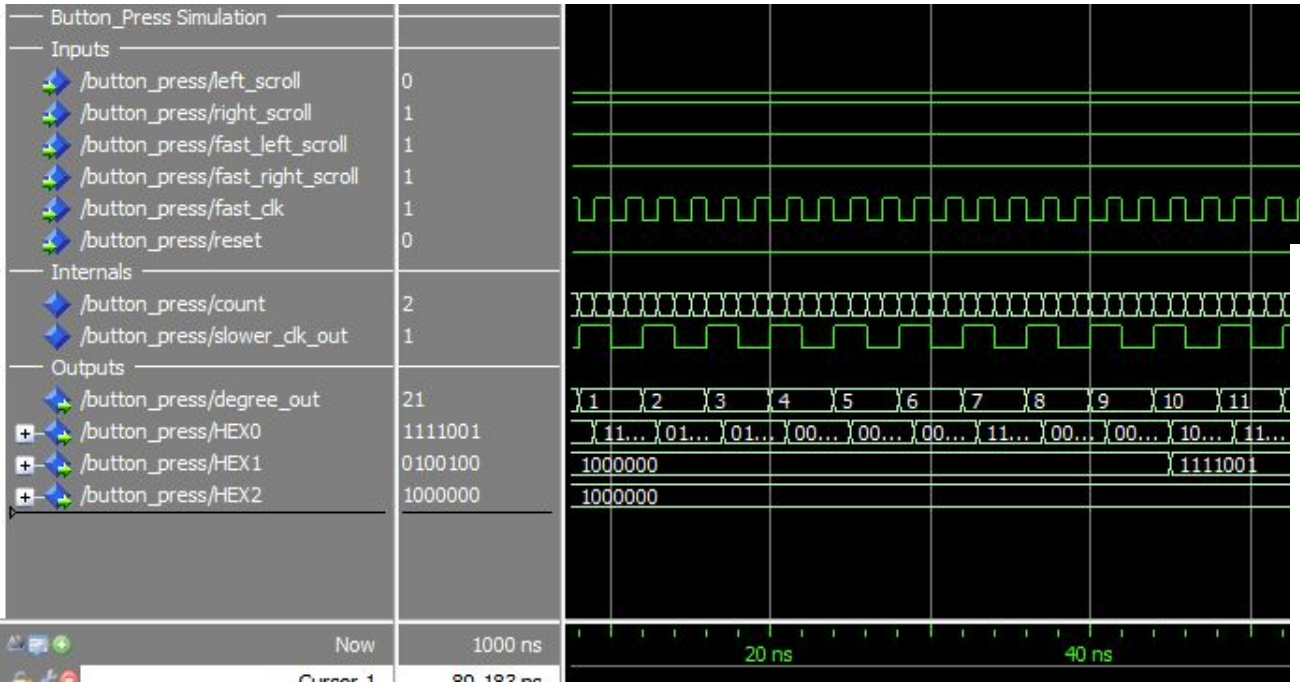
HEX display

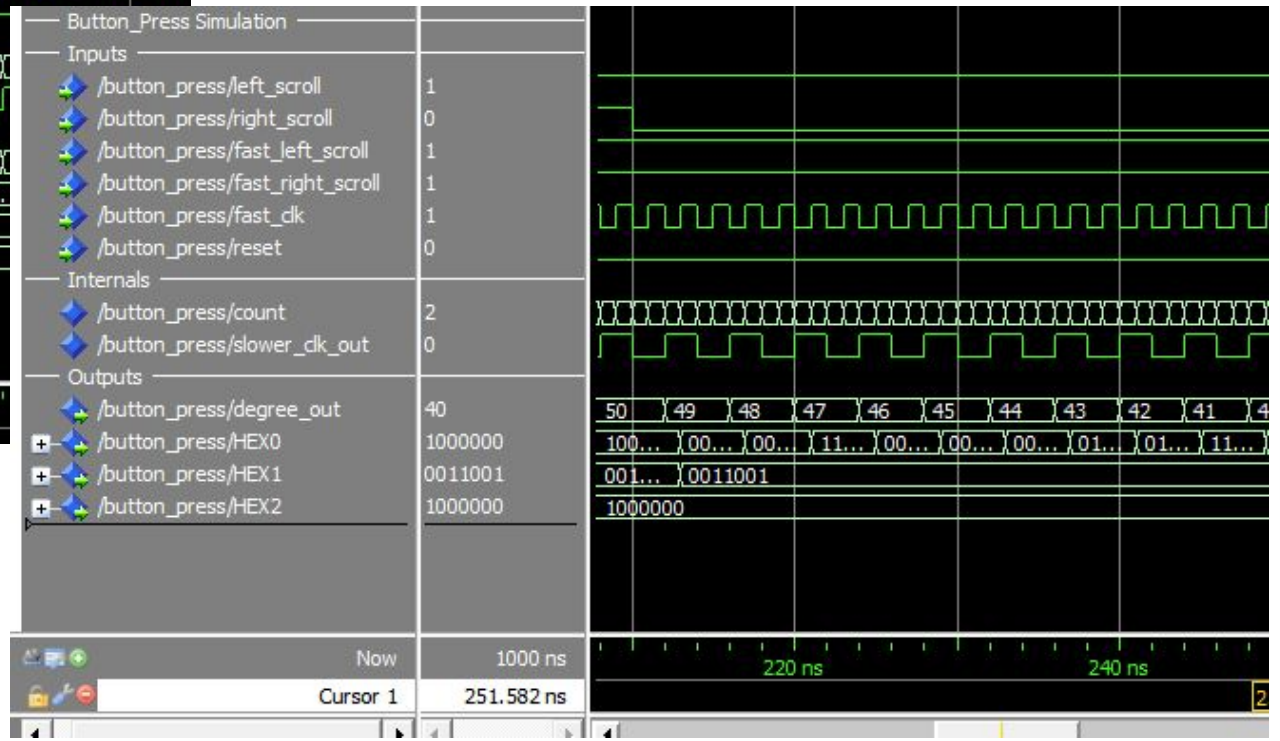


Button Press component

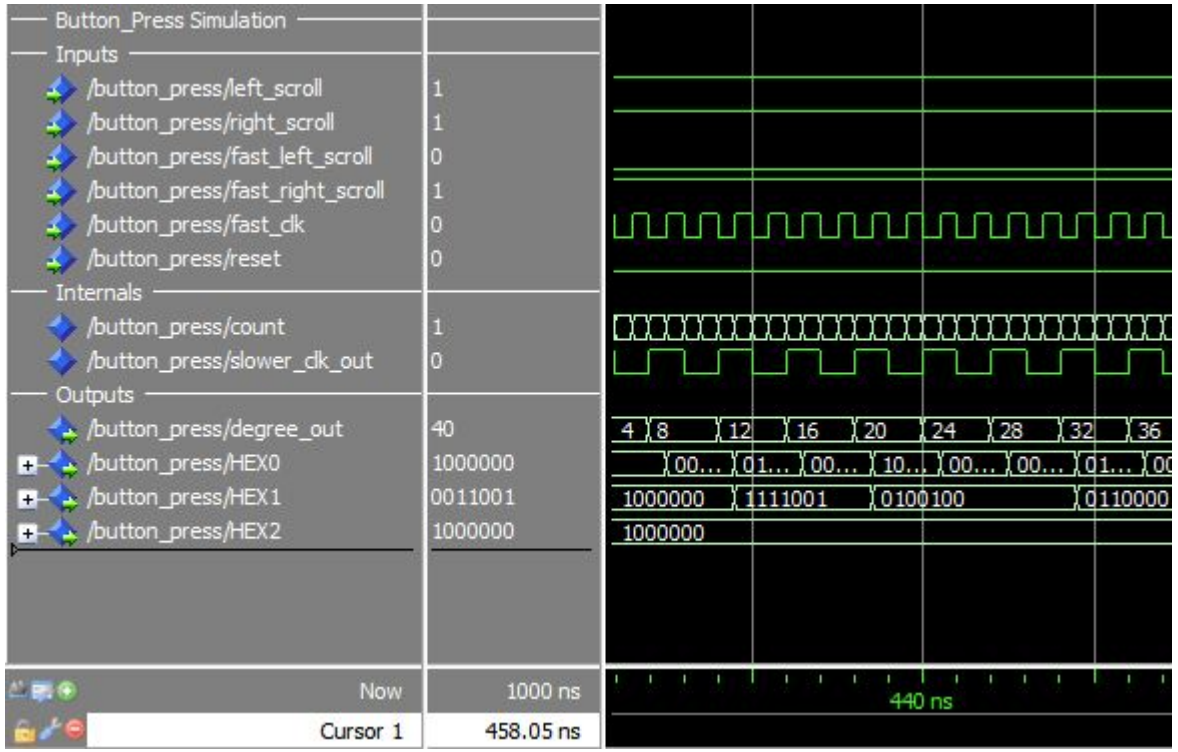


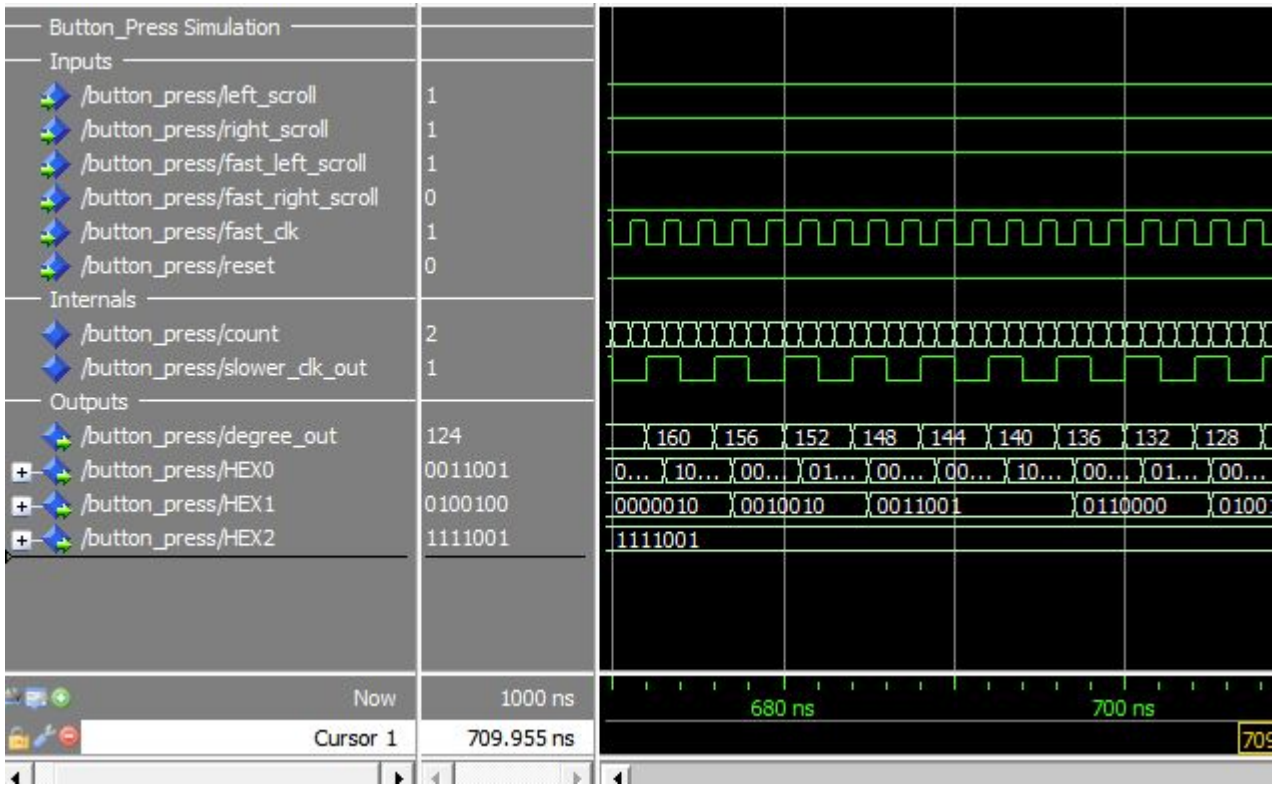
Left Scroll & Right Scroll



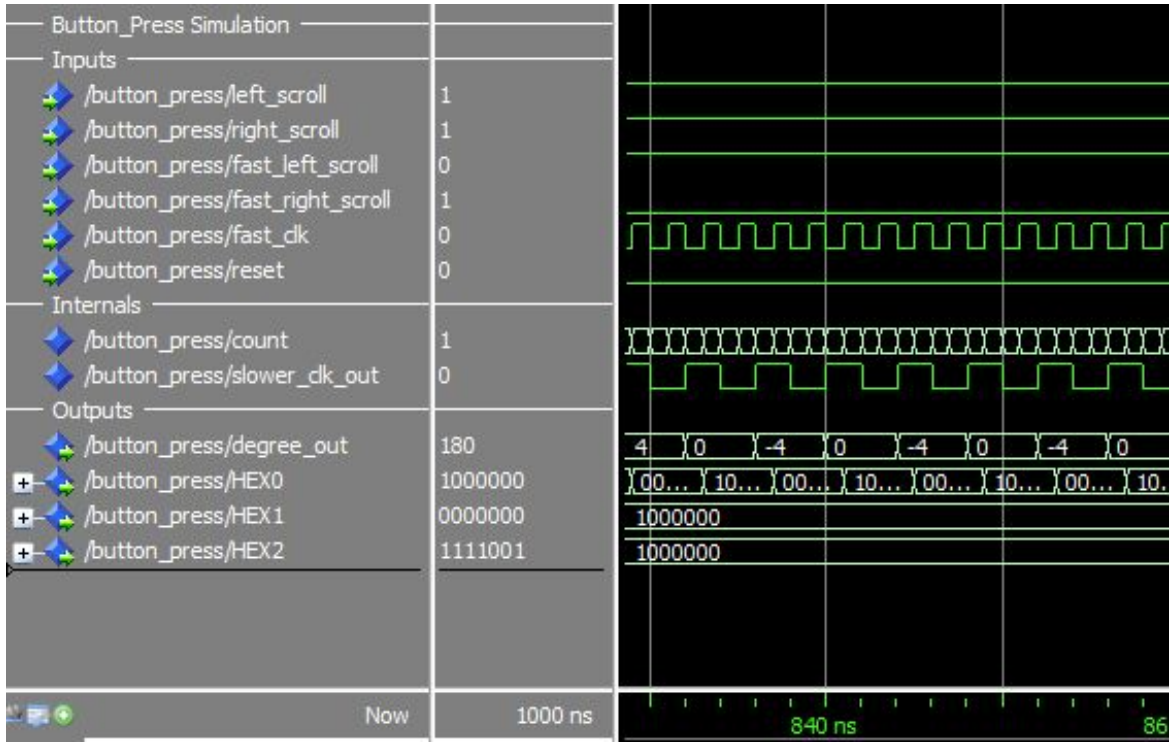


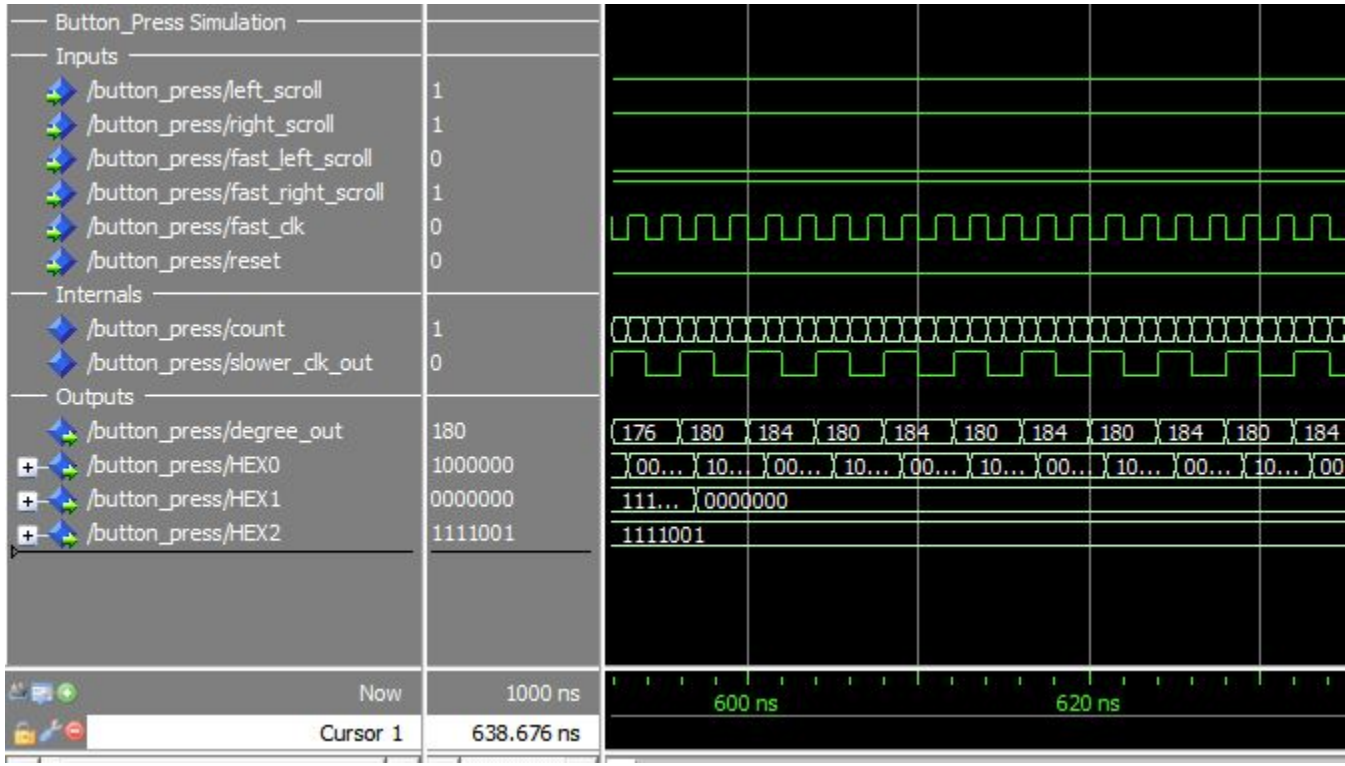
Fast left scroll and fast right scroll



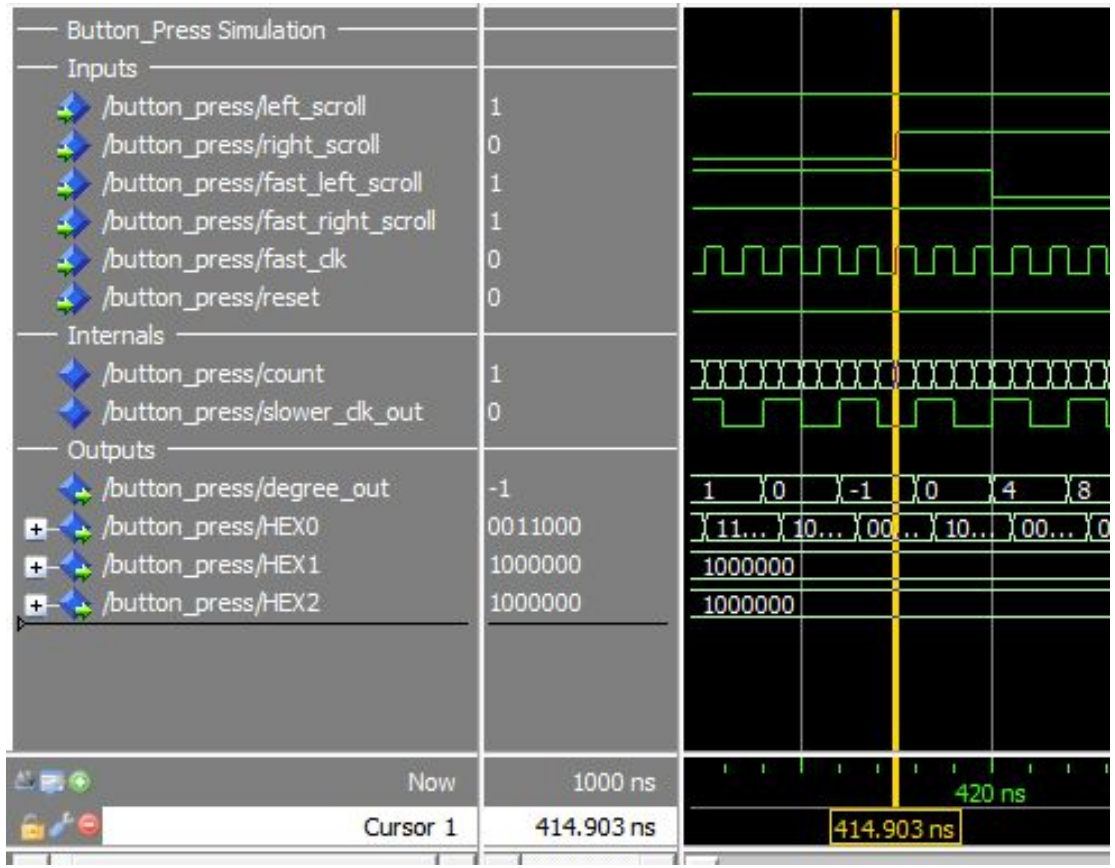


Button Press Component Issues

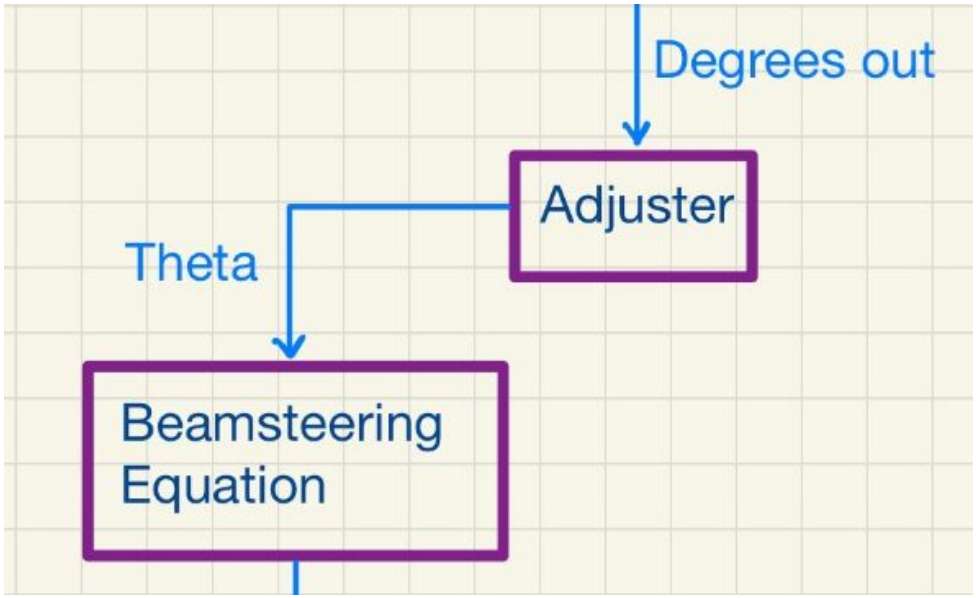


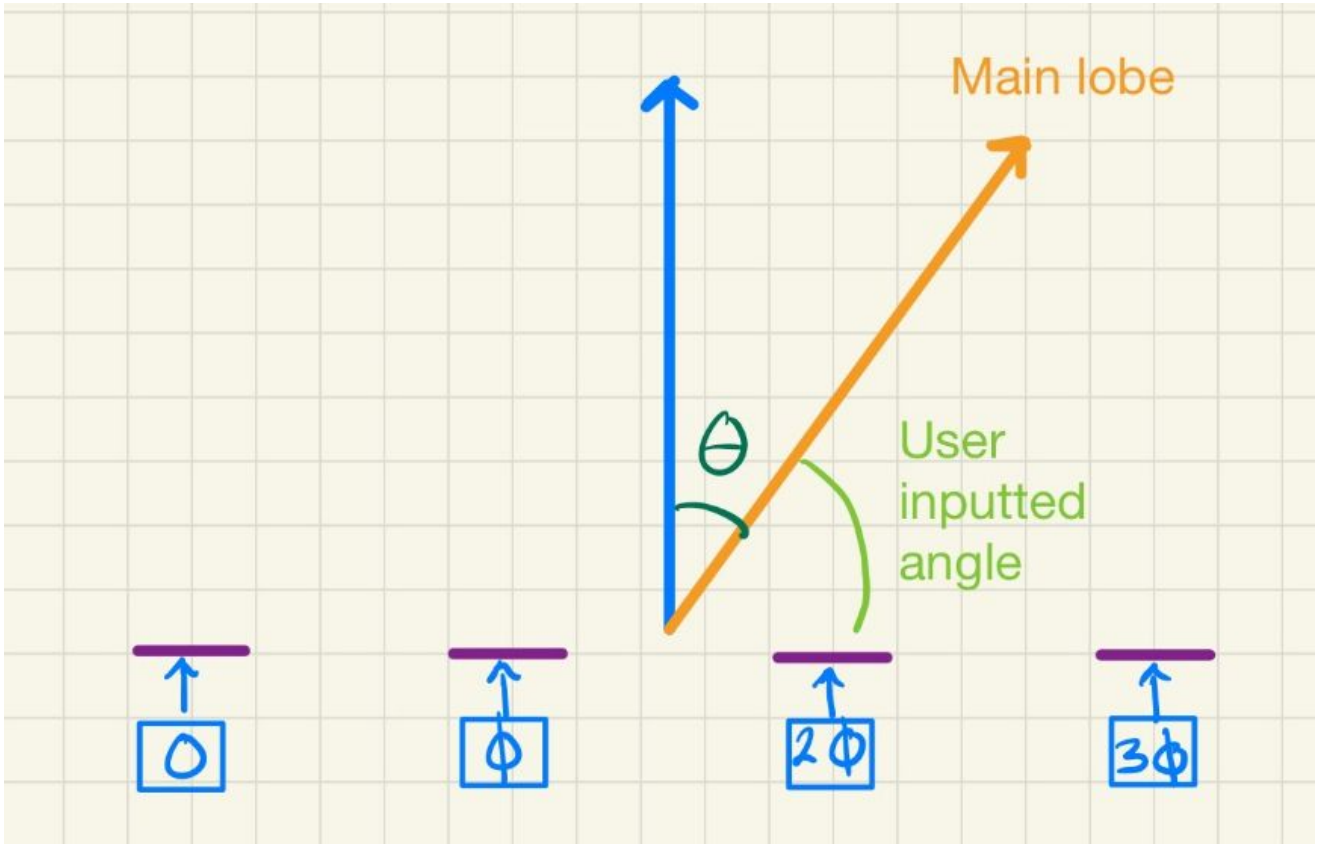


Button Press Component Issues continued

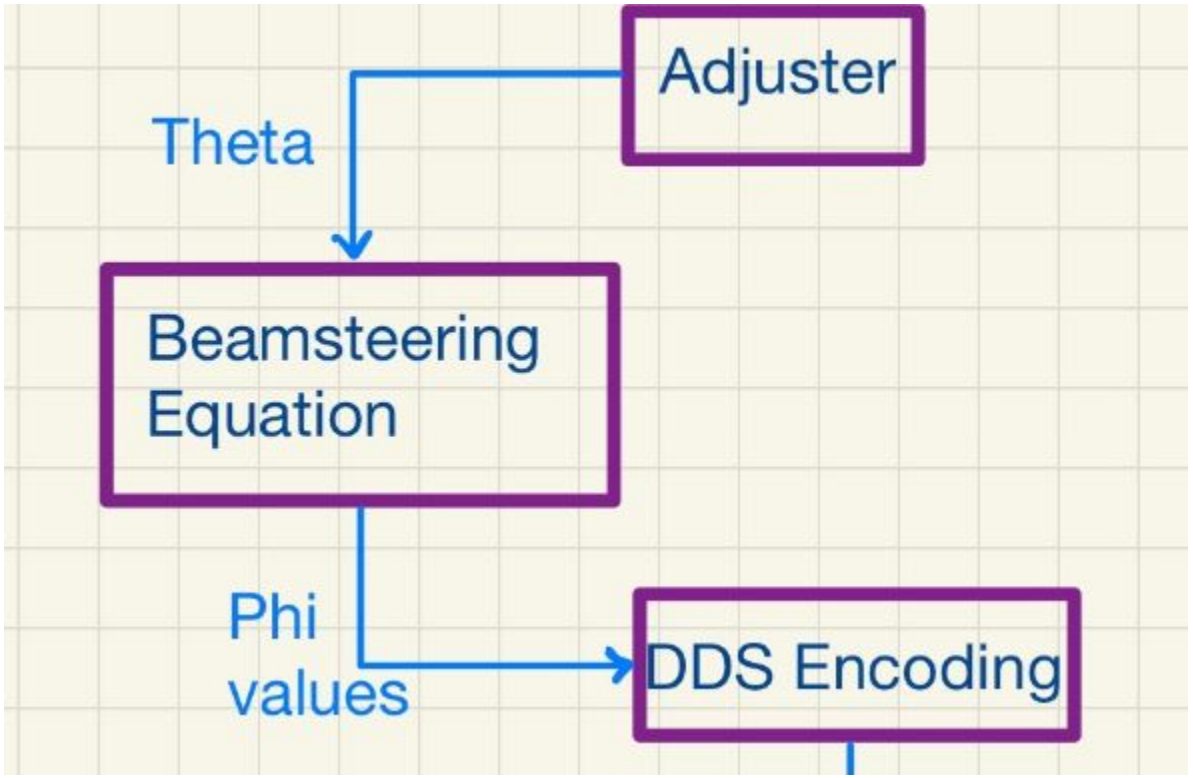


Adjuster component

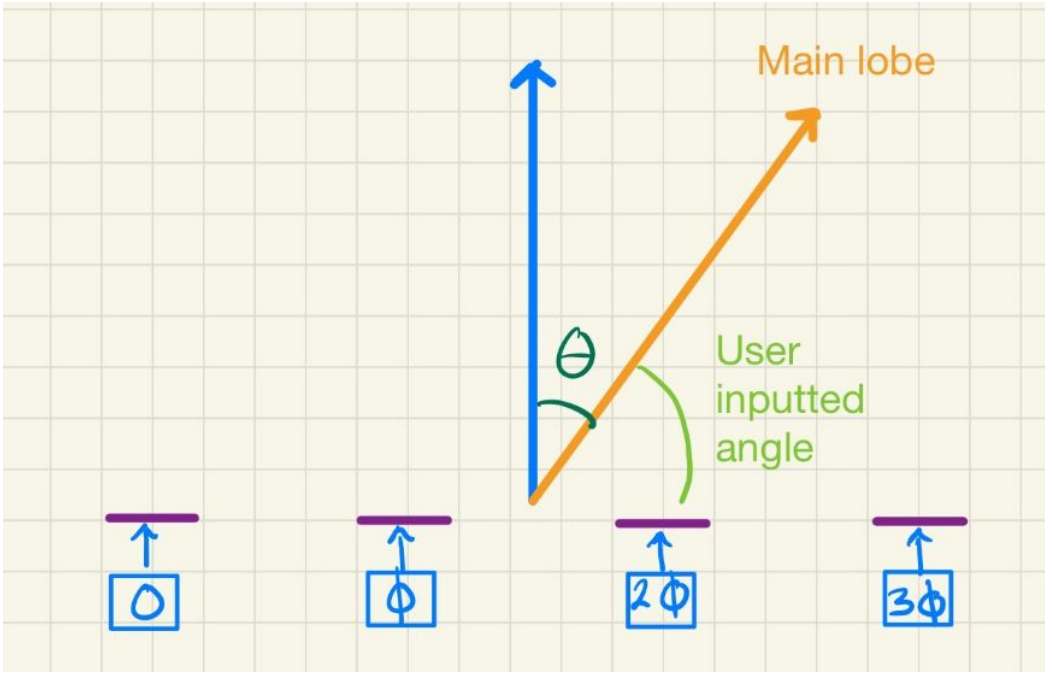




Beamsteering Equation Component



$$\phi = \pi \times \sin(\theta)$$



Beamsteering Equation Simulations

Input interpretation

$\pi \sin(1.5708)$

Result

3.141592654…

Beamsteering Equation Test		
Inputs		
/bean/x_in	-15708	-15708
Internals		
/bean/term_n_value	-15708 -6458 -796 -46 -1 0	-15708 -6458 -796 -46 -1 0
/bean/taylor_output	-10001	-10001
Outputs		
/bean/phi1_out	-31418	-31418
/bean/phi2_out	-62836	-62836
/bean/phi3_out	-94254	-94254

Beamsteering Equation Test		
Inputs		
/bean/x_in	15708	15708
Internals		
/bean/term_n_value	15708 6458 796 46 1 0	15708 6458 796 46 1 0
/bean/taylor_output	10001	10001
Outputs		
/bean/phi1_out	31418	31418
/bean/phi2_out	62836	62836
/bean/phi3_out	94254	94254

continued

Input interpretation

$\pi \sin(1.0472)$

Result

2.72070…

Input

$\pi \sin(0.7854)$

Result

2.22145…

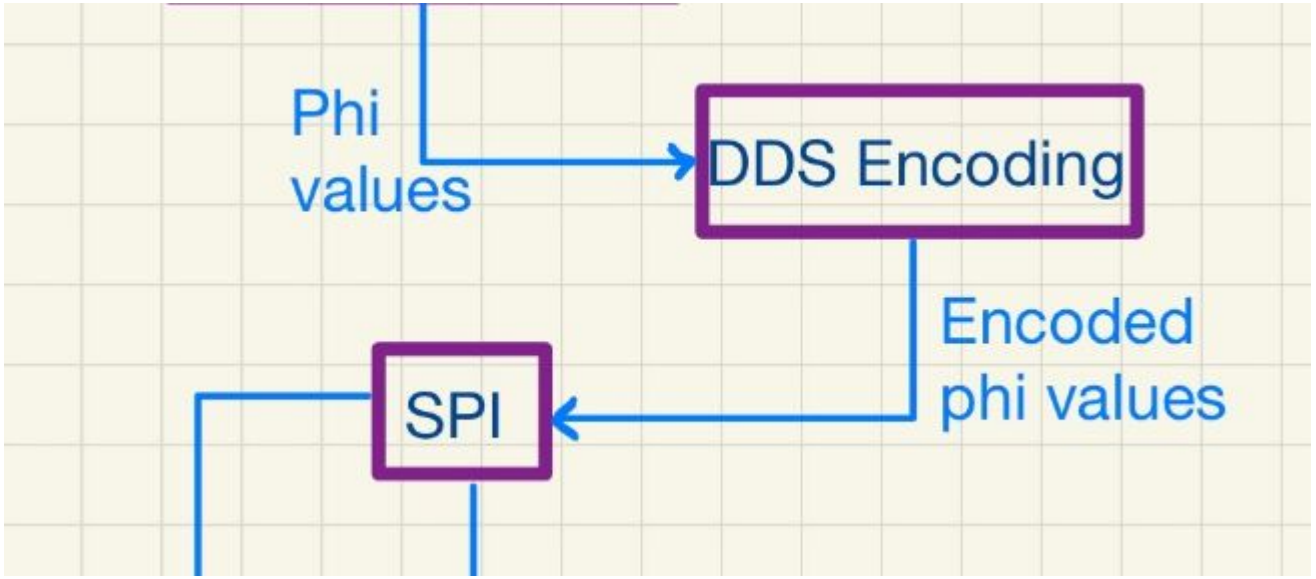
Beamsteering Equation Test		
Inputs		
/bean/x_in	10472	10472
Internals		
/bean/term_n_value	10472 1913 104 2 0 0	10472 1913 104 2 0 0
/bean/taylor_output	8661	8661
Outputs		
/bean/phi1_out	27208	27208
/bean/phi2_out	54417	54417
/bean/phi3_out	81625	81625

Beamsteering Equation Test		
Inputs		
/bean/x_in	7854	7854
Internals		
/bean/term_n_value	7854 807 24 0 0 0	7854 807 24 0 0 0
/bean/taylor_output	7071	7071
Outputs		
/bean/phi1_out	22213	22213
/bean/phi2_out	44427	44427
/bean/phi3_out	66640	66640

Beamsteering implementation issues

Flow Status	Successful - Thu Mar 10 10:27:38 2022
Quartus Prime Version	21.1.0 Build 842 10/21/2021 SJ Lite Edition
Revision Name	bean
Top-level Entity Name	bean
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	9,593 / 56,480 (17 %)
Total registers	0
Total pins	128 / 268 (48 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	46 / 156 (29 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

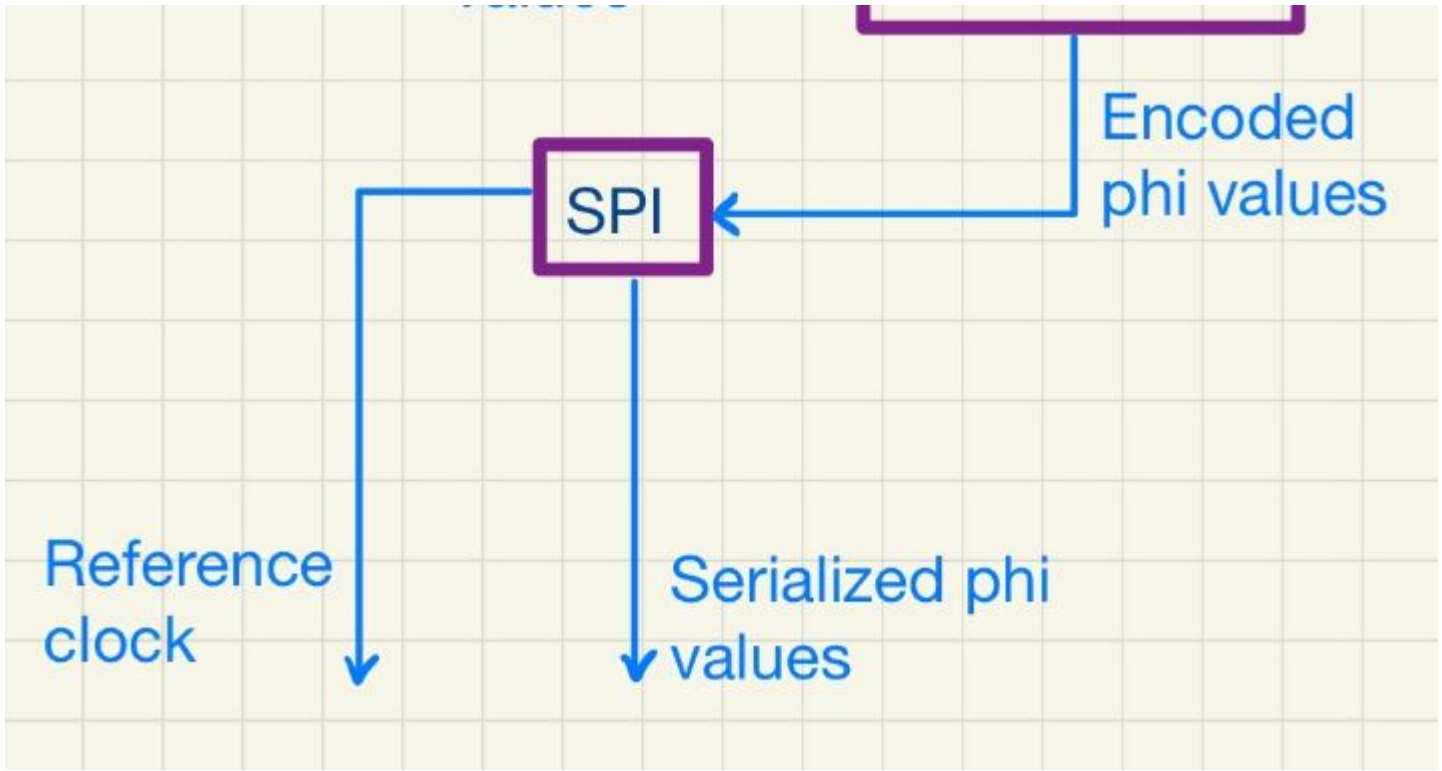
DDS Encoder Block



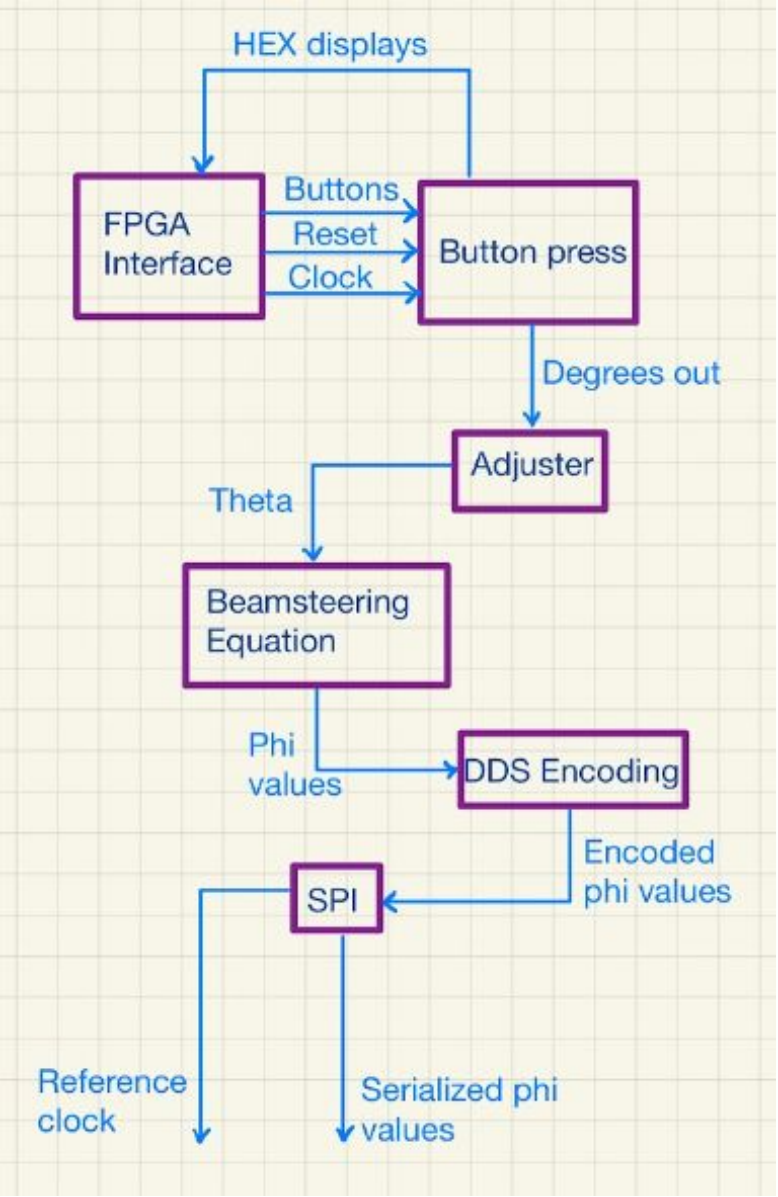
Has a resolution of $0.02197\ degrees$

$$0 = 0, \qquad 1 = 0.02197, \qquad 10 = 2 \times 0.02197, \qquad 11 = 3 \times 0.02197$$

SPI block


Encoded
phi values
SPI
Reference
clock
Serialized phi
values

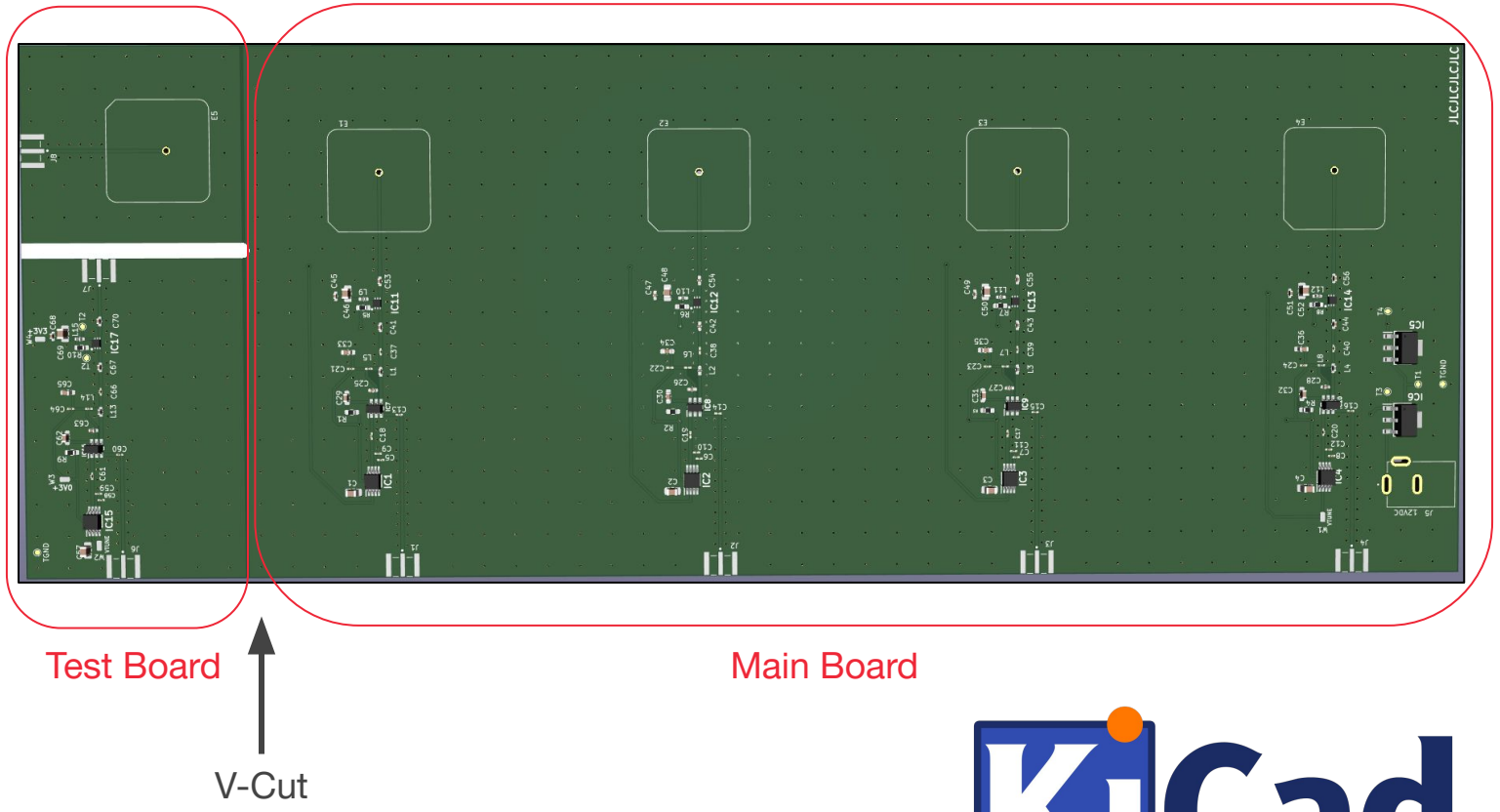
Full Block Diagram



PCB Design - Current Update

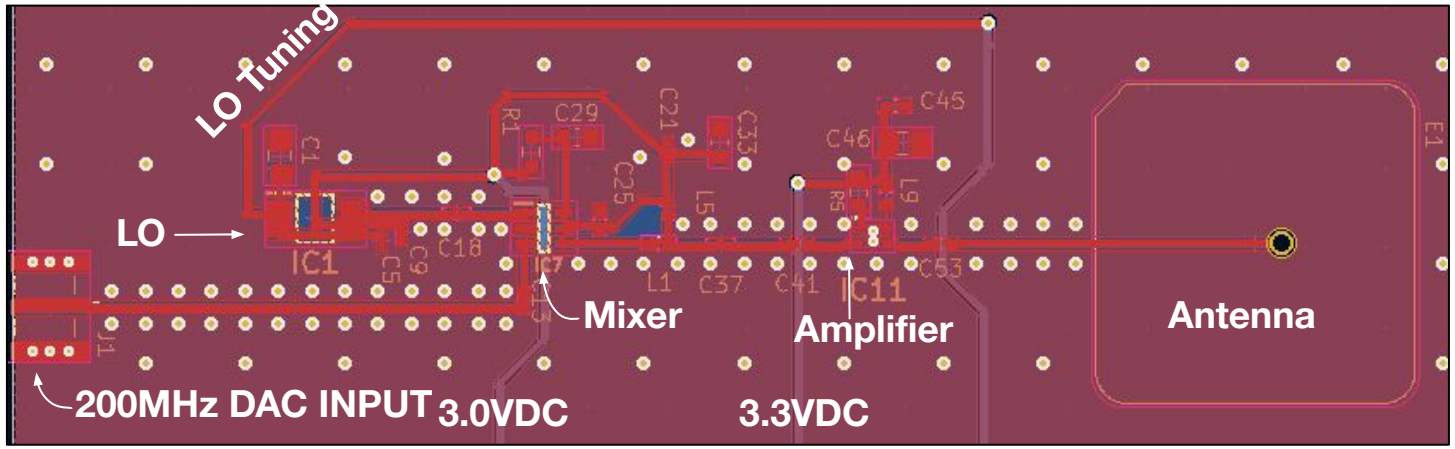
Included Components

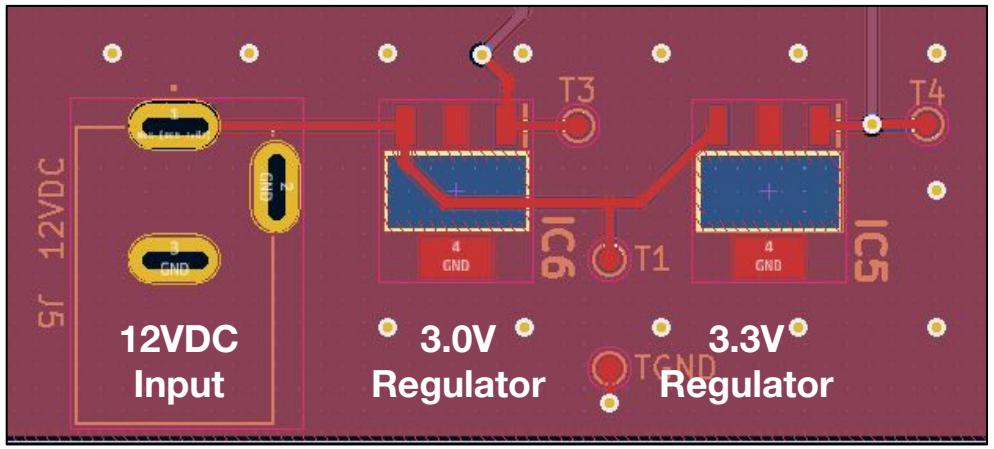
- MAXIM2751EUA+
  - Local Oscillator
- MAXIM2660EUT+
  - Upconverter/Mixer
- GRF2201
  - 20dB Amplifier
- ANT-2.4-CPA
  - 2.4GHz Patch Antenna



PCB Design

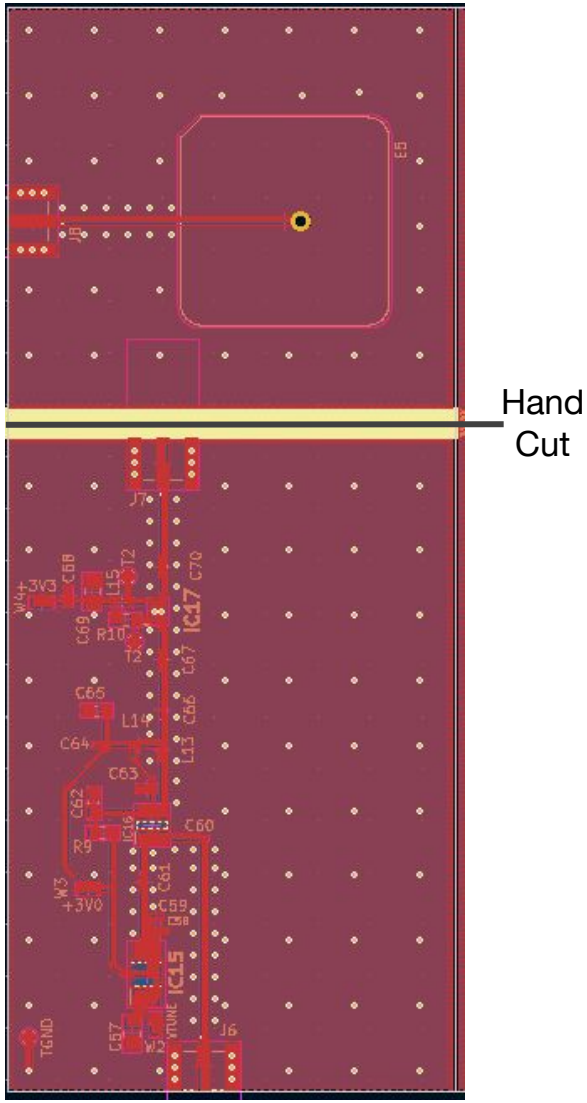
- RF Traces are **0.562mm** thick for **50Ω** line impedance
- Antennas placed λ/2 = **62.5mm** apart
- Vias in grid placed λ/20 = **6.25mm** apart
- Vias along traces placed λ/60 = **2.08mm** apart





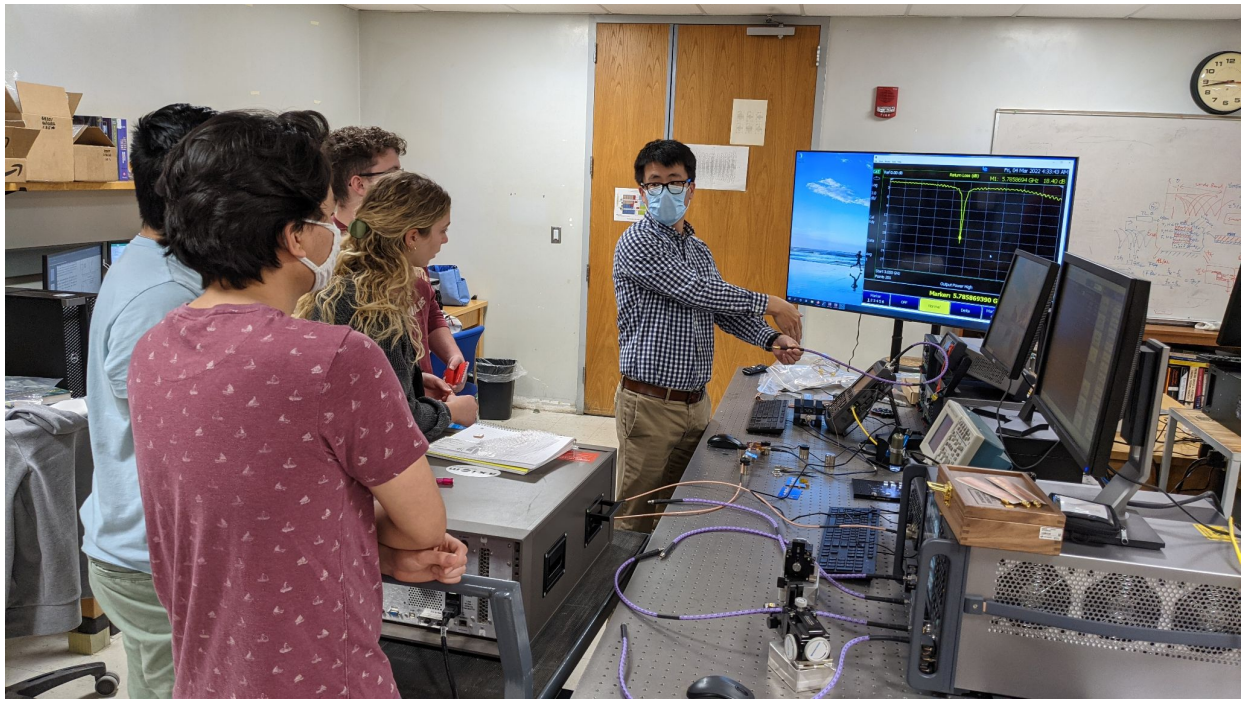
PCB Test Cutout

- Our PCB will have a test cut
  - Within the test cut there will be:
    - Antenna ground plane cut
    - Other components cut
- Practice soldering tiny components
  - Components are tinier than any team member has experience with

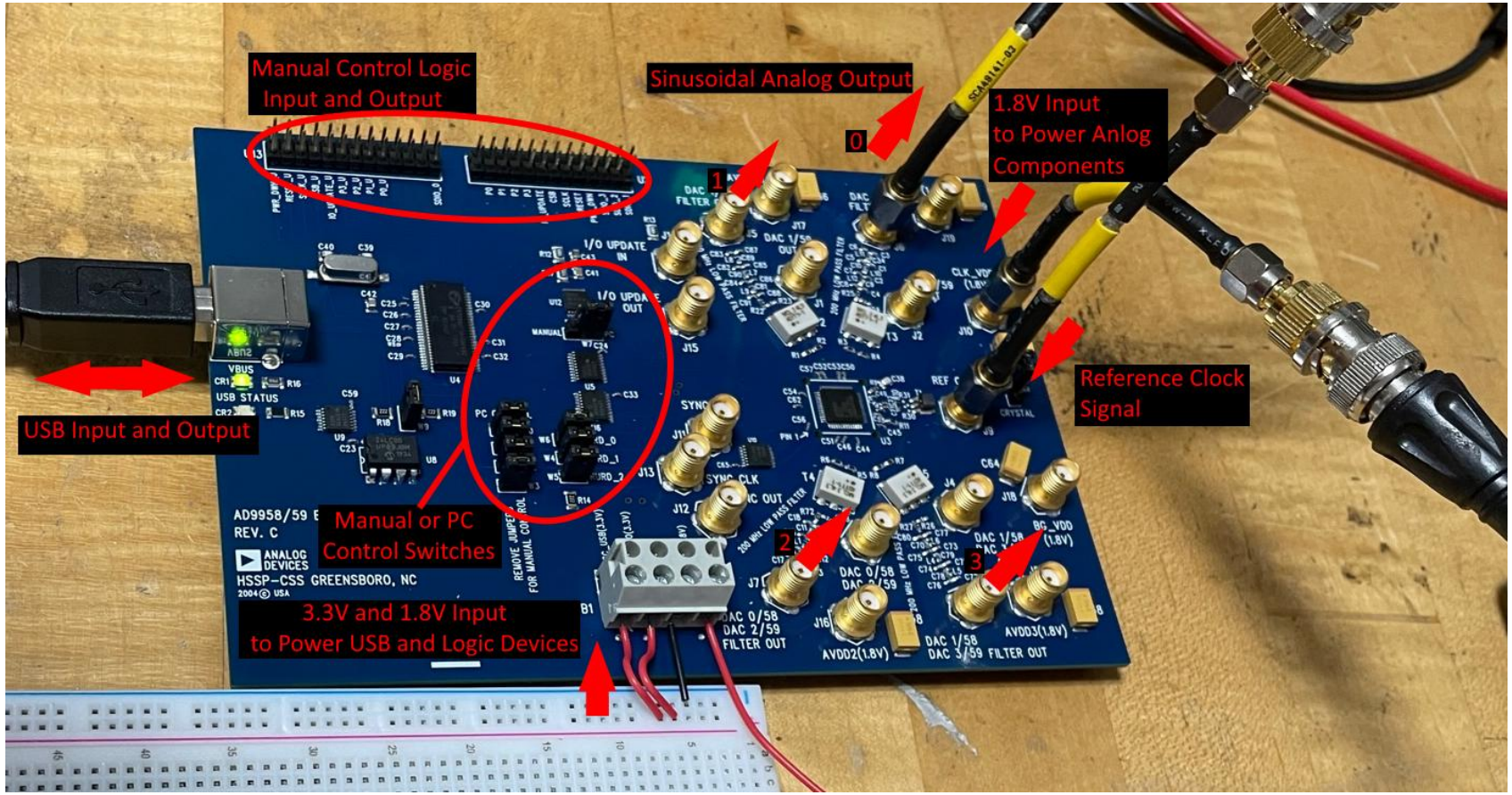


Intermediate Testing

- Antenna ground plane cut allows us to test total return loss and input impedance
  - Can calculate power radiated and gain from these values
- Components cut allows us to test that the signal is propagating through PCB and signal is amplified



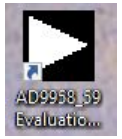
DDS Testing: AD9959

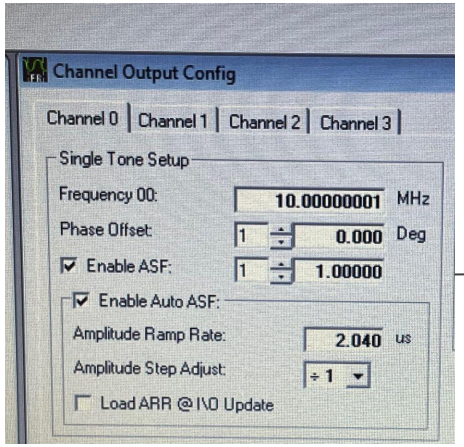


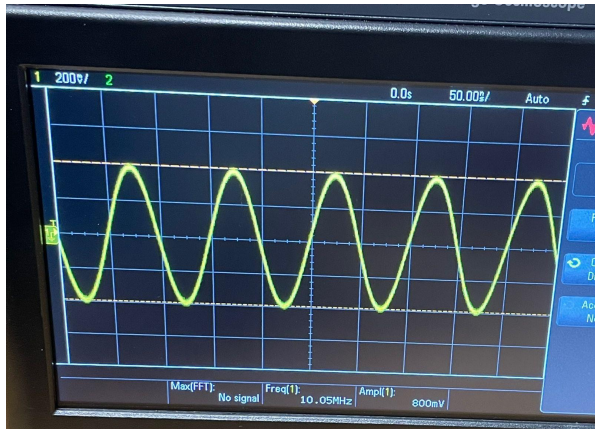
- Changes For Final Design
  - Power supply
  - No USB
  - Manual Mode
  - FPGA Wired to Logic Input and Output
  - Crystal Oscillator
- To Do:
  - Test with FPGA (Spring Break)

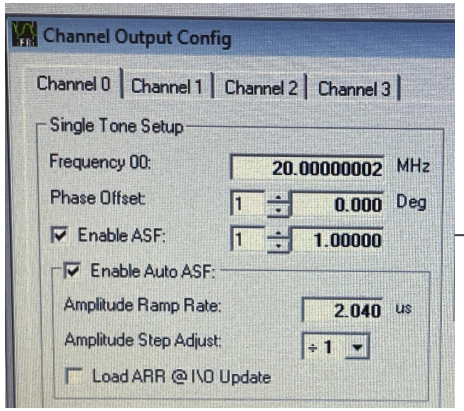
DDS Test Results

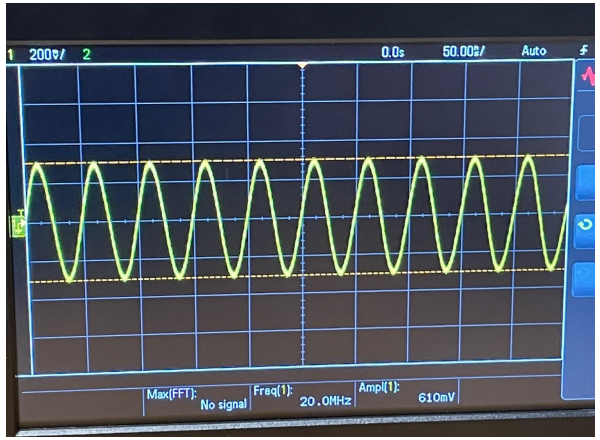
Evaluation Software

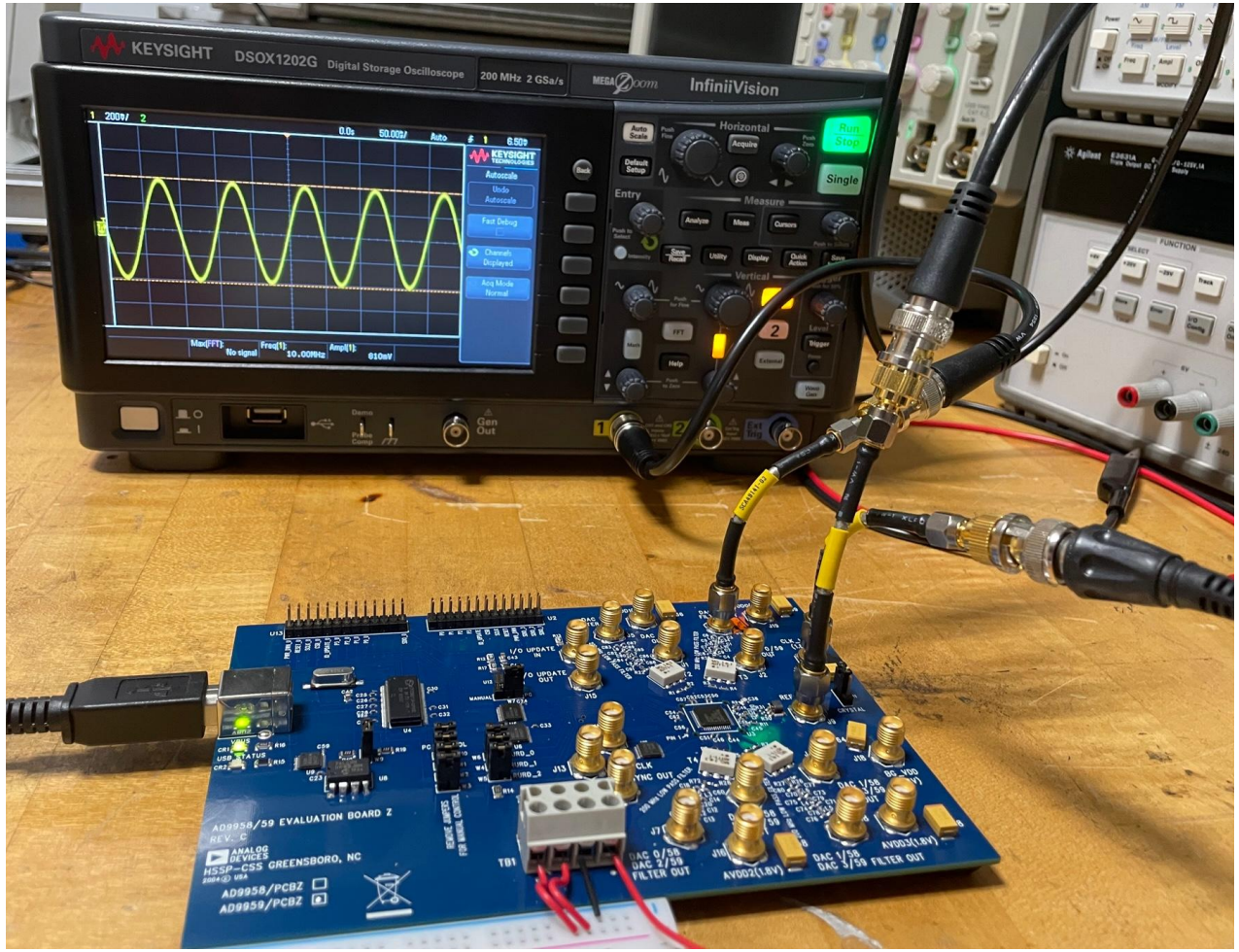




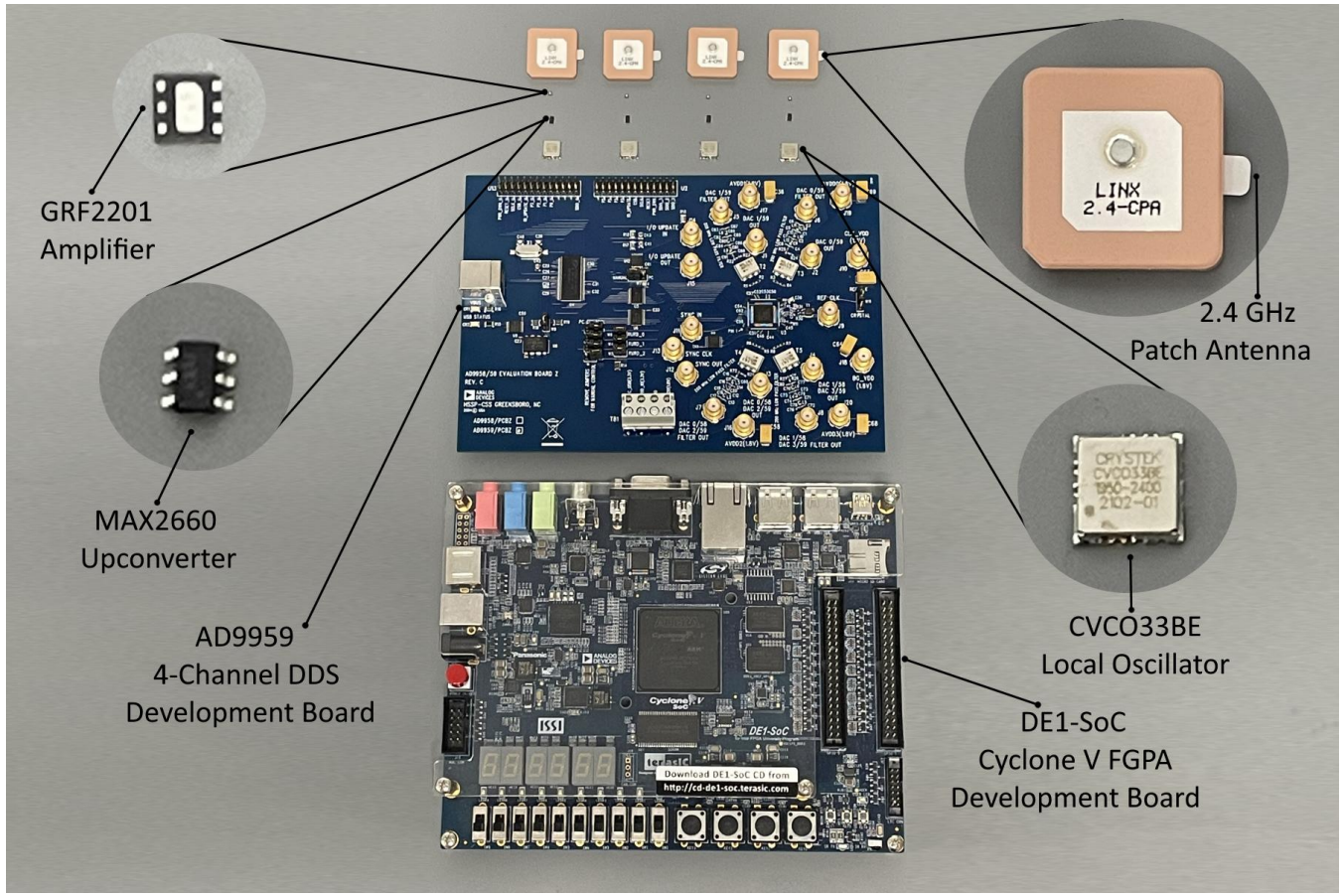








Final Hardware Assembly



- Final Assembly
  - PCB
  - Soldering
    - Impedance Matching Networks: 50 Ohm
- Final testing
  - Dr. Arigong's Lab
    - Spectrum Analyzer

Presentation Recap

- Project Background
- Current Progress Update
  - VHDL coding implementations
  - PCB design
  - Testing
- Future Work
  - Soldering Components
  - Intermediate Testing
  - Final Design

References

- Datasheets:
  - https://www.mouser.com/datasheet/2/256/MAX2750-MAX2752-1512450.pdf
  - https://www.mouser.com/datasheet/2/256/MAX2660-MAX2673-1515397.pdf
  - https://www.mouser.com/datasheet/2/777/GRRF_S_A0010122589_1-2575831.pdf
  - https://www.mouser.com/datasheet/2/238/LNNC_S_A0009494921_1-2551007.pdf

Questions?