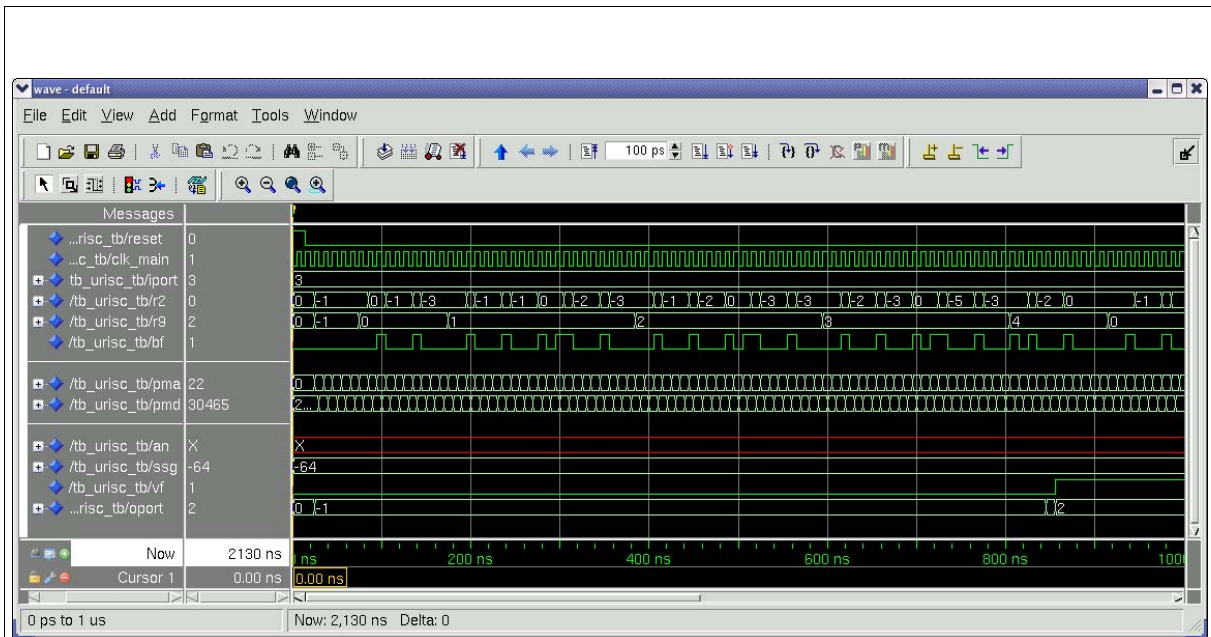


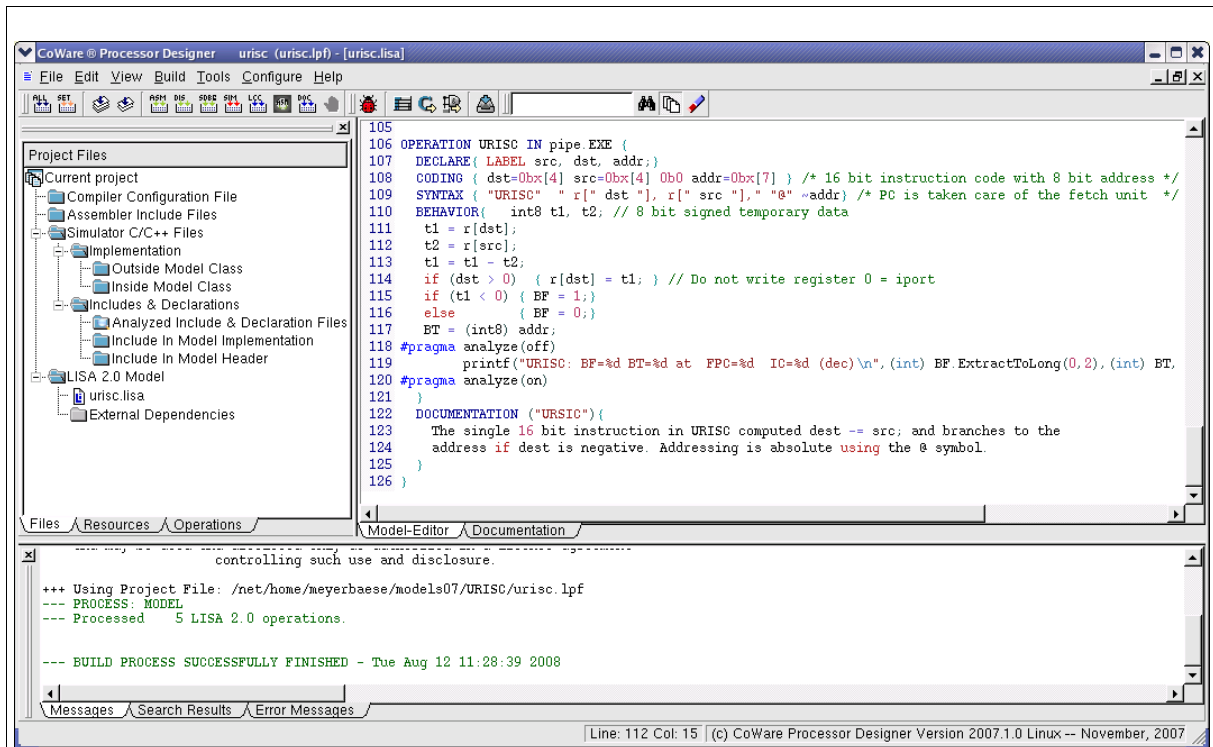
URISC0 simulation with iport load and output to oport: URISCsim0.bmp

#1



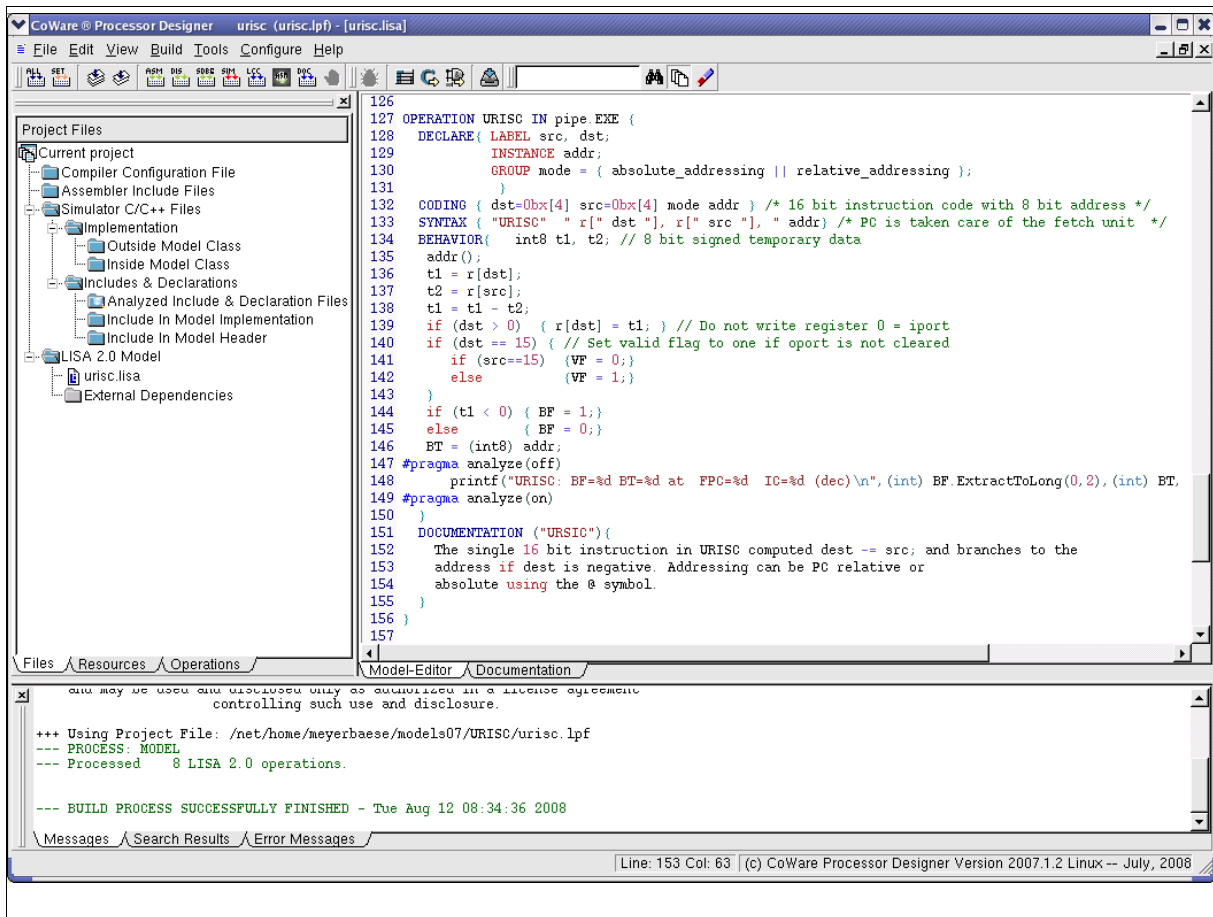
URISC1 Fibonacci simulation with iport=3 and output oport=2: URISCsim1.bmp

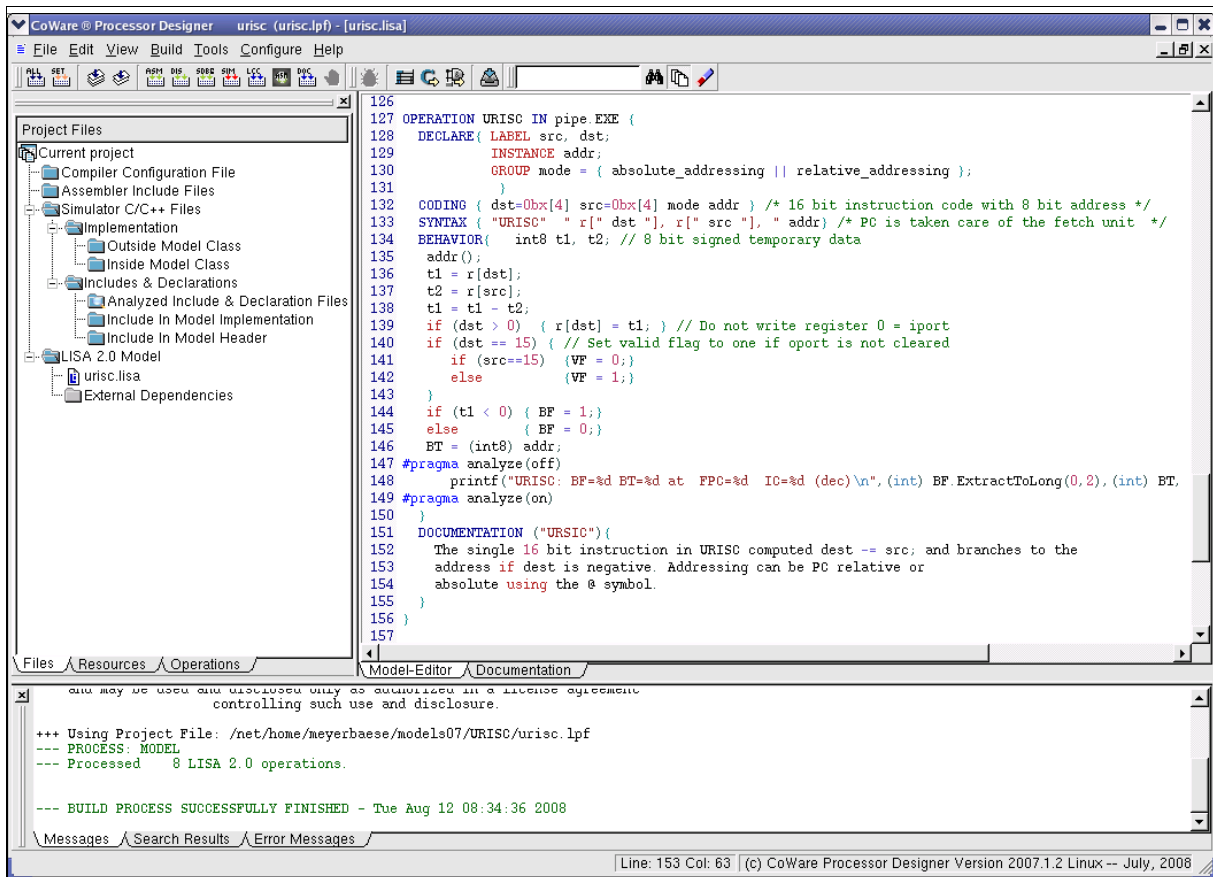
#2



The Processor Designer Window: URISCcode0.bmp

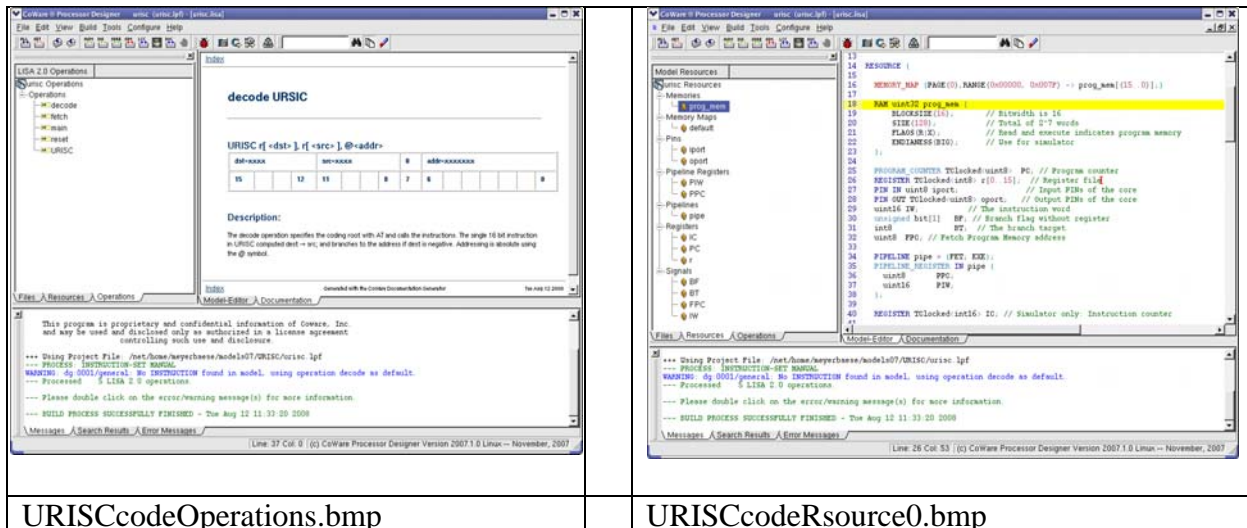
#3





The Processor Designer Window: URISCcode1.bmp

#4



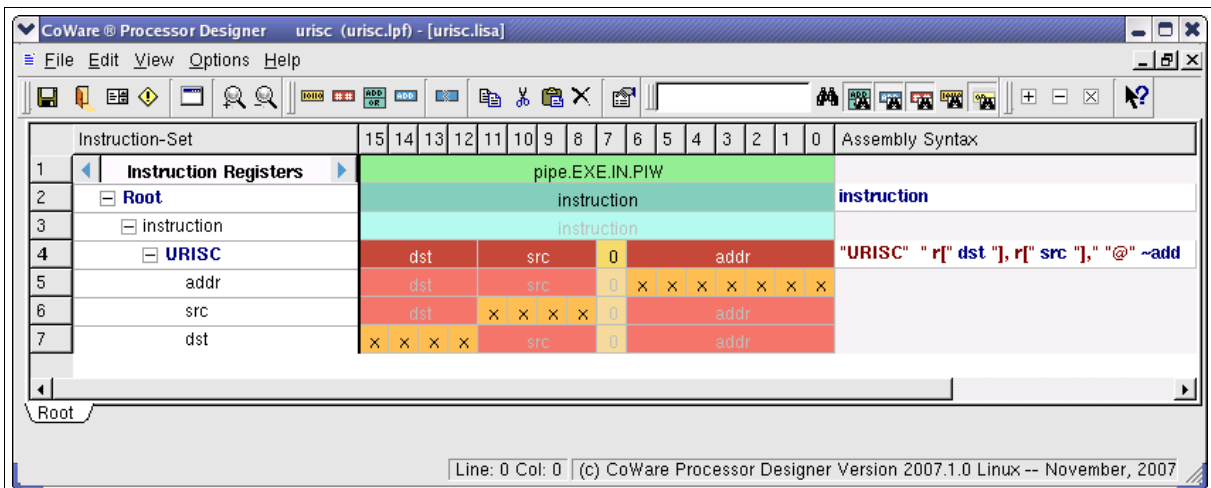
URISCcodeOperations.bmp

URISCcodeRsource0.bmp

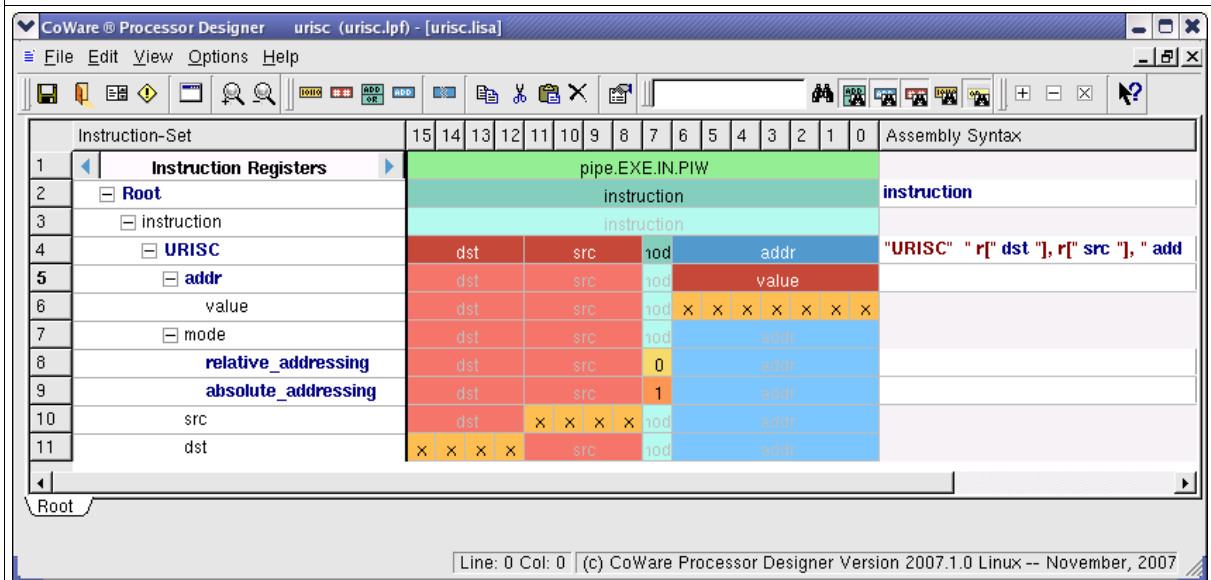
#5

		<p>decode URISC addr</p> <p>URISC [r <dst>], r [<src>], @ <value: unsigned decimal value></p> <table border="1"> <thead> <tr> <th>dst-xxxx</th> <th>src-xxxx</th> <th>mode</th> <th>value-xxxxxxxx</th> </tr> </thead> <tbody> <tr> <td>15</td> <td>12</td> <td>11</td> <td>8 7 6</td> </tr> </tbody> </table> <p>Description: The decode operation specifies the coding root with AT and calls the instructions. The single 16 bit URISC computed dest => src; and branches to the address if dest is negative. Addressing can be absolute using the @ symbol. The PC update in URISC in the assembler coding can be relative (see (using @)).</p> <p>copyright (c) 2001-2007 by covare, inc. ALL RIGHTS RESERVED</p> <p>This program is proprietary and confidential information of Covare, Inc. and may be used and disclosed only as authorized in a license agreement controlling such use and disclosure.</p> <pre> +++ Using Project File: /net/home/seyerbaess/models07/URISC/2007.1.0_linux/workied/urisc.lpf --- PROCESS: MODEL PASS 1 +++ Syntax Check successfully finished --- BUILD PROCESS SUCCESSFULLY FINISHED - Mon Aug 4 16:07:53 2008 </pre>	dst-xxxx	src-xxxx	mode	value-xxxxxxxx	15	12	11	8 7 6
dst-xxxx	src-xxxx	mode	value-xxxxxxxx							
15	12	11	8 7 6							
<p>URISCcodeOperation s.bmp</p>	<p>URISCcodeResource s.bmp</p>	<p>URISCcodeDocu.bmp</p>								

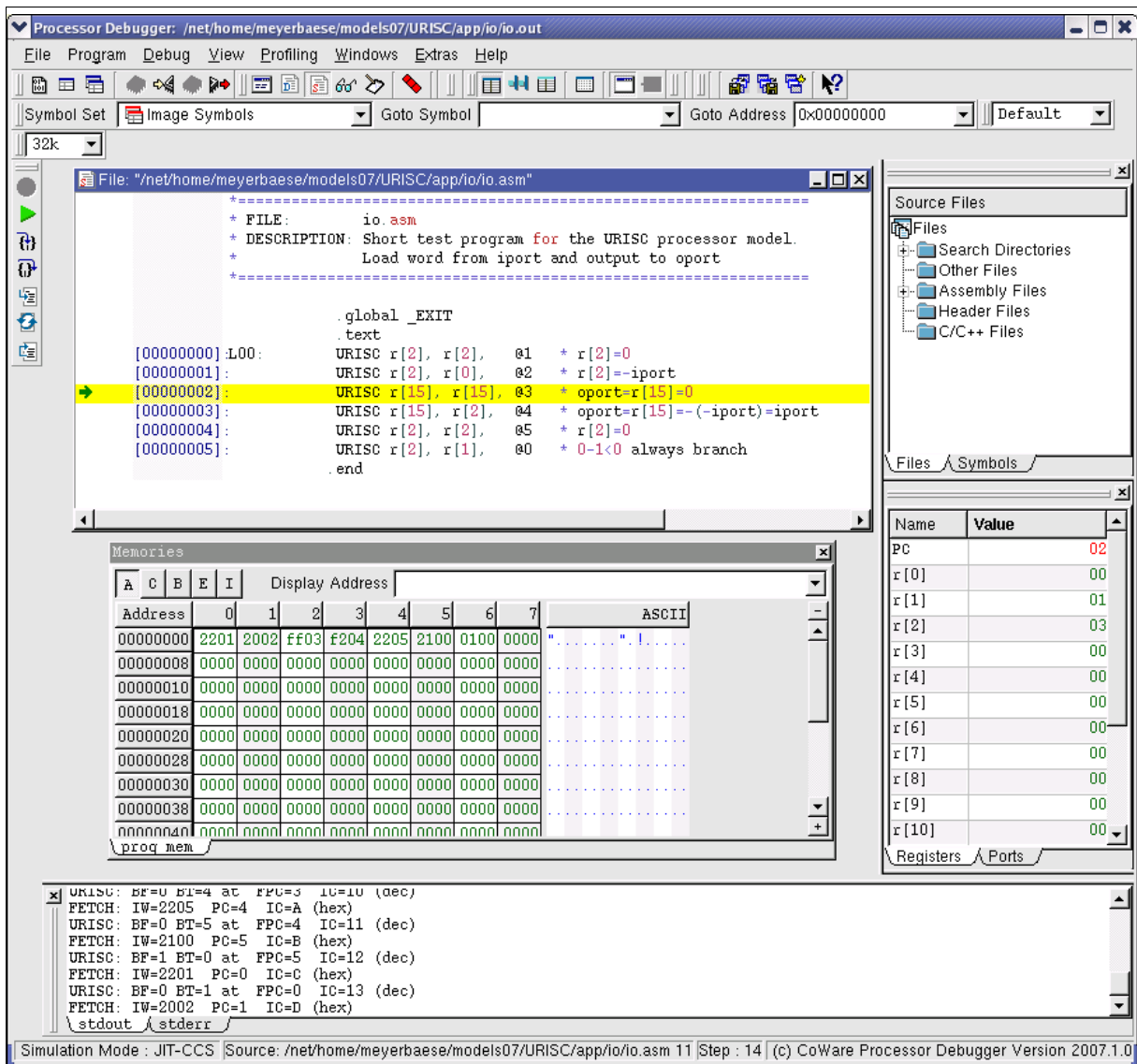
#6 The Processor Designer Documentaton Window.



The URISC instruction set view: URISCisa0.bmp



The URISC instruction set view: URISCisa1.bmp



The URISC debugger: URISCdebug0.bmp

Processor Debugger: /net/home/meyerbaese/models07/URISC/app/fibonacci/fibonacci.out

File: "/net/home/meyerbaese/models07/URISC/app/fibonacci/fibonacci.asm"

```

[00000001]: URISC r[7], r[7], +1 * r[7]=0
[00000002]: URISC r[7], r[1], +1 * fn+1=1
[00000003]: URISC r[9], r[9], +1 * loop-counter=0
*****
***** fn+2=fn+fn+1
[00000004]: L01: URISC r[2], r[2], +1 * r[2]=0
[00000005]: URISC r[2], r[6], +1 * r[2]=fn
[00000006]: URISC r[2], r[7], +1 * r[2]=fn+fn+1
[00000007]: URISC r[8], r[8], +1 * r[8]=0
[00000008]: URISC r[8], r[2], +1 * fn+2=(-fn+fn+1)
*****
***** if loop counter++ >= iport => done
[00000009]: URISC r[2], r[2], +1 * r[2]=0
[0000000a]: URISC r[2], r[0], +1 * r[2]=iport
[0000000b]: URISC r[3], r[3], +1 * r[3]=0
[0000000c]: URISC r[3], r[2], +1 * r[3]=iport
*****
***** inc iport for loop test
***** URISC r[3], r[1], +1 * r[3]++
[0000000d]: URISC r[9], r[1], +1 * loop-counter++=1
[0000000e]: URISC r[3], r[9], @L02 * done if iport<loop-counter
*****
***** Move fn+1 to fn
[0000000f]: URISC r[2], r[2], +1 * r[2]=0
[00000010]: URISC r[2], r[7], +1 * r[2]=fn+1
[00000011]: URISC r[6], r[6], +1 * r[6]=0

```

Registers

Name	Value
PC	01
r[0]	03
r[1]	ff
r[2]	00
r[3]	ff
r[4]	ff
r[5]	ff
r[6]	02
r[7]	03
r[8]	05
r[9]	04
r[10]	ff
r[11]	ff
r[12]	ff
r[13]	ff
r[14]	ff
r[15]	02
VF	f
IC	0055

Memories

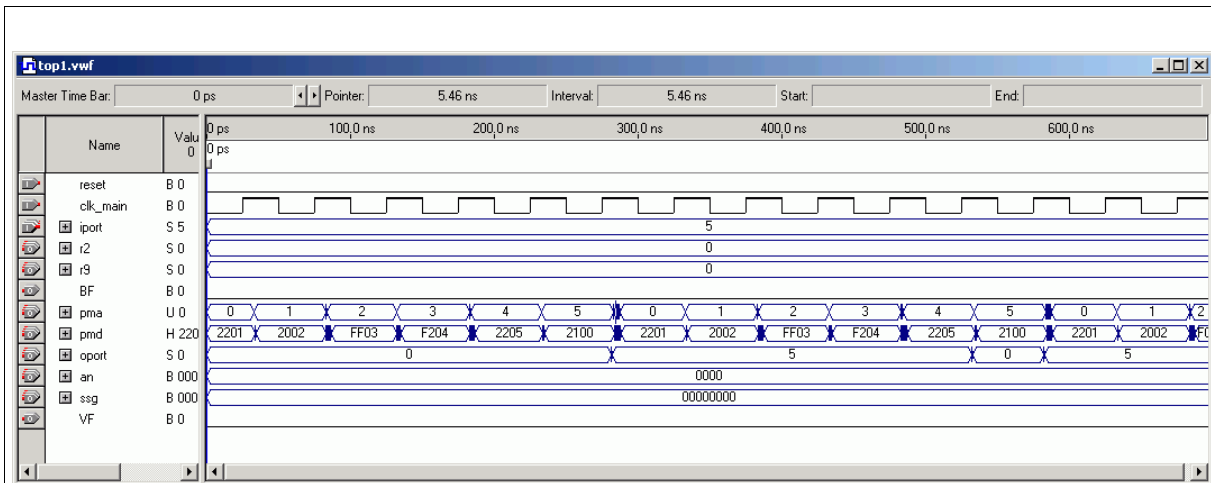
Address	0	1	2	3	4	5	6	7	ASCII
00000000	6601	7701	7101	9901	2201	2601	2701	8801	f.w.q... "&".
00000008	8201	2201	2001	3301	3201	9101	3999	2201	... "3.2...9".
00000010	2701	6601	6201	2201	2801	7701	7201	2201	..f.b." (.w.r.".
00000018	1284	2201	2601	ff01	f201	2201	1280	0001	.. "&....".
00000020	0001	0001	0000	0000	0000	0000	0000	0000
00000028	0000	0000	0000	0000	0000	0000	0000	0000

URISC: BF=0 BT=1 at FPC=27 IC=81 (dec)
 FETCH: IW=F201 PC=1C IC=51 (hex)
 URISC: BF=0 BT=1 at FPC=28 IC=82 (dec)
 FETCH: IW=2201 PC=1D IC=52 (hex)
 URISC: BF=0 BT=1 at FPC=29 IC=83 (dec)
 FETCH: IW=1280 PC=1E IC=53 (hex)
 URISC: BF=1 BT=0 at FPC=30 IC=84 (dec)
 FETCH: IW=6601 PC=0 IC=54 (hex)

Simulation Mode : JIT-CCS | Source: /net/home/meyerbaese/models07/URISC/app/fibonacci/fibonacci.asm | Step : 85 | (c) CoWare Processor Debugger Version 2007.1.0 Linux -- No

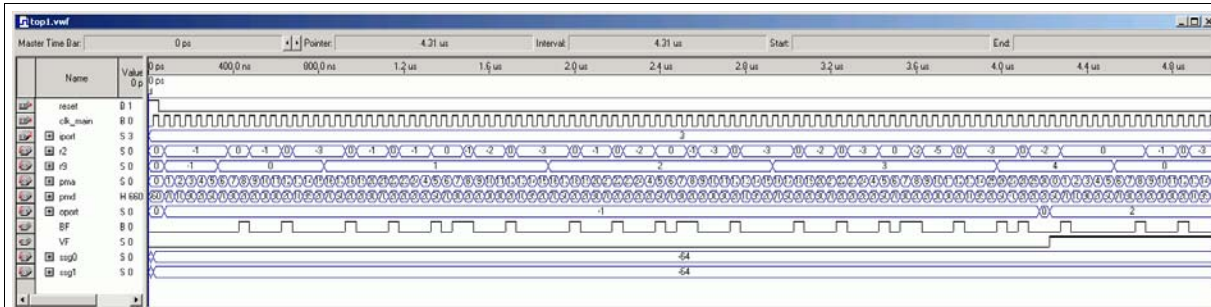
Fibonacci application The URISC debugger: URISCdebug1.bmp

Altera Synthesis Results URSIC



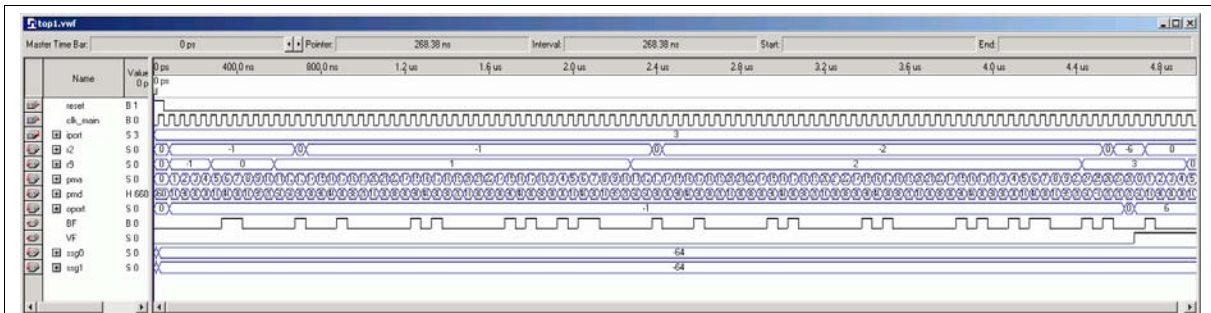
URISC0 simulation with iport load and output to oport=5: aURISCsimio.gif

#10



URISC1 Fibonacci simulation with iport =3 and output oport=2: aURISCsimFibo.gif

#11



URISC1 Factorial simulation with iport =3 and output oport=6: aURISCsimFact.gif

#12