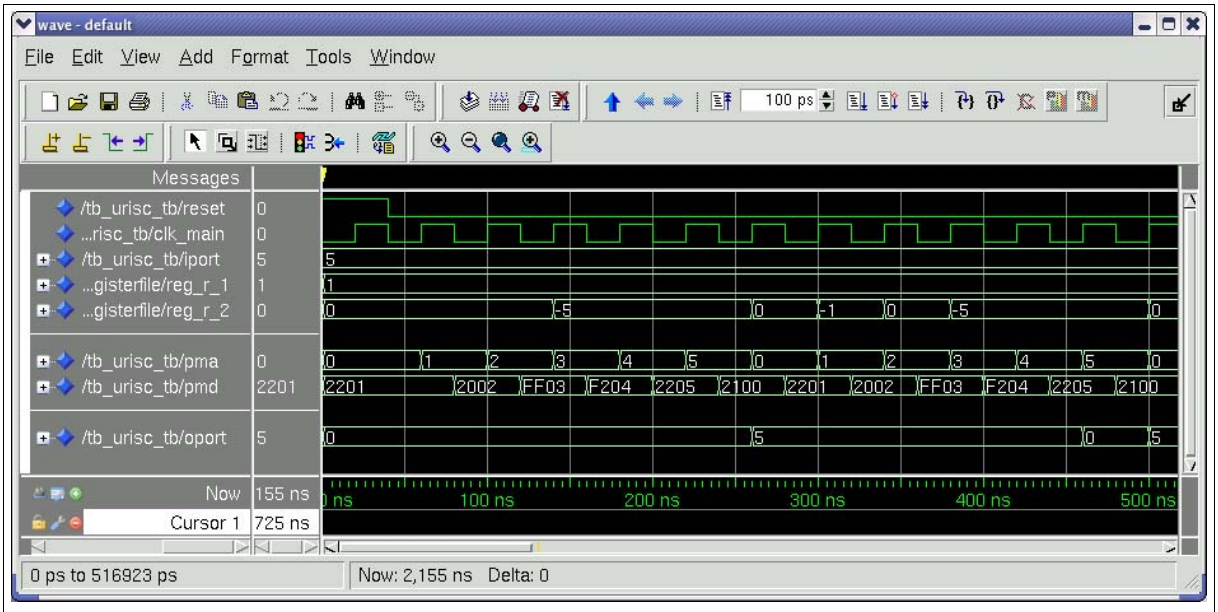
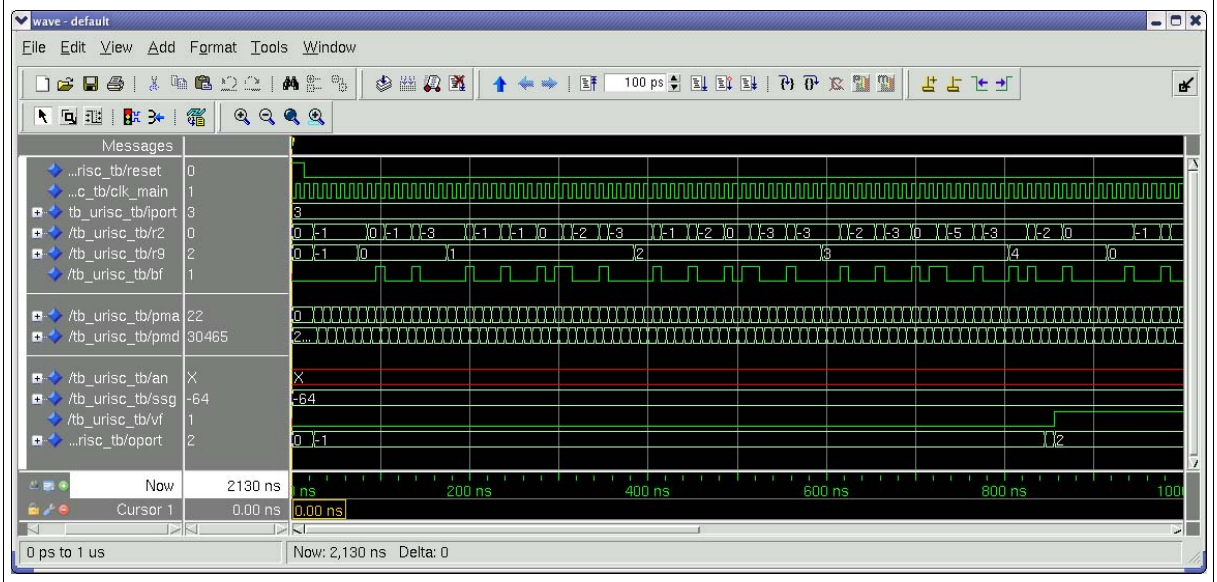


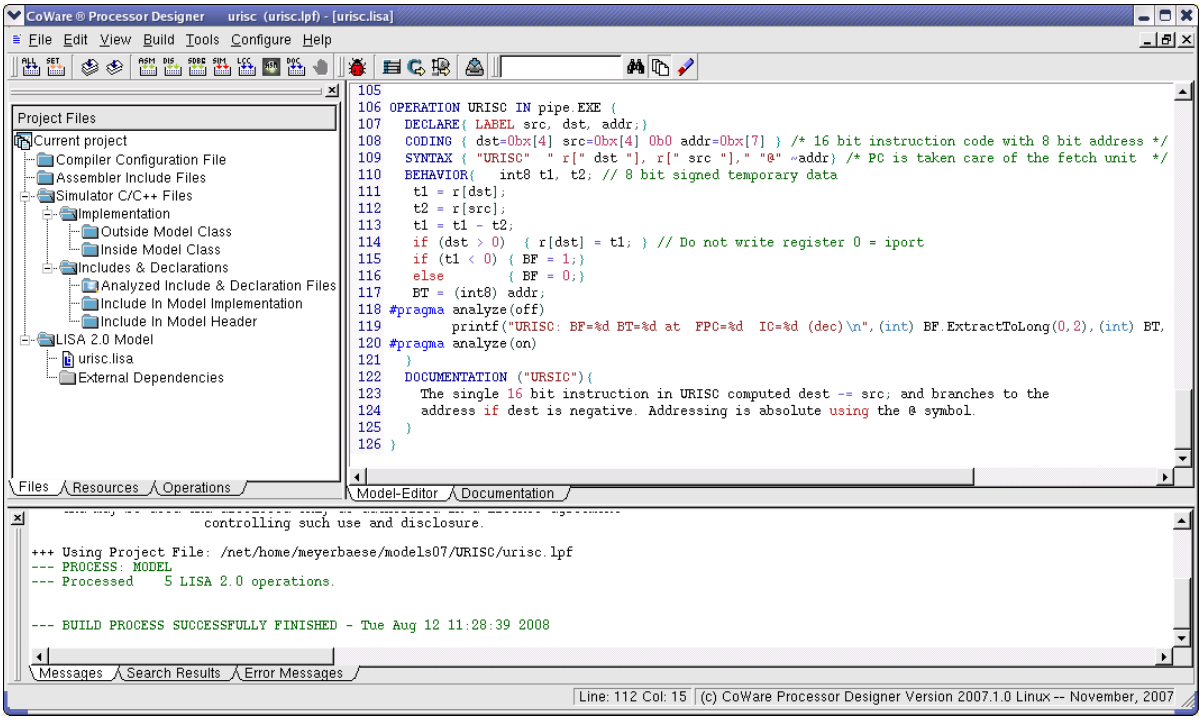
URISC0 simulation with iport load and output to oport: URISCsim0.bmp

#1



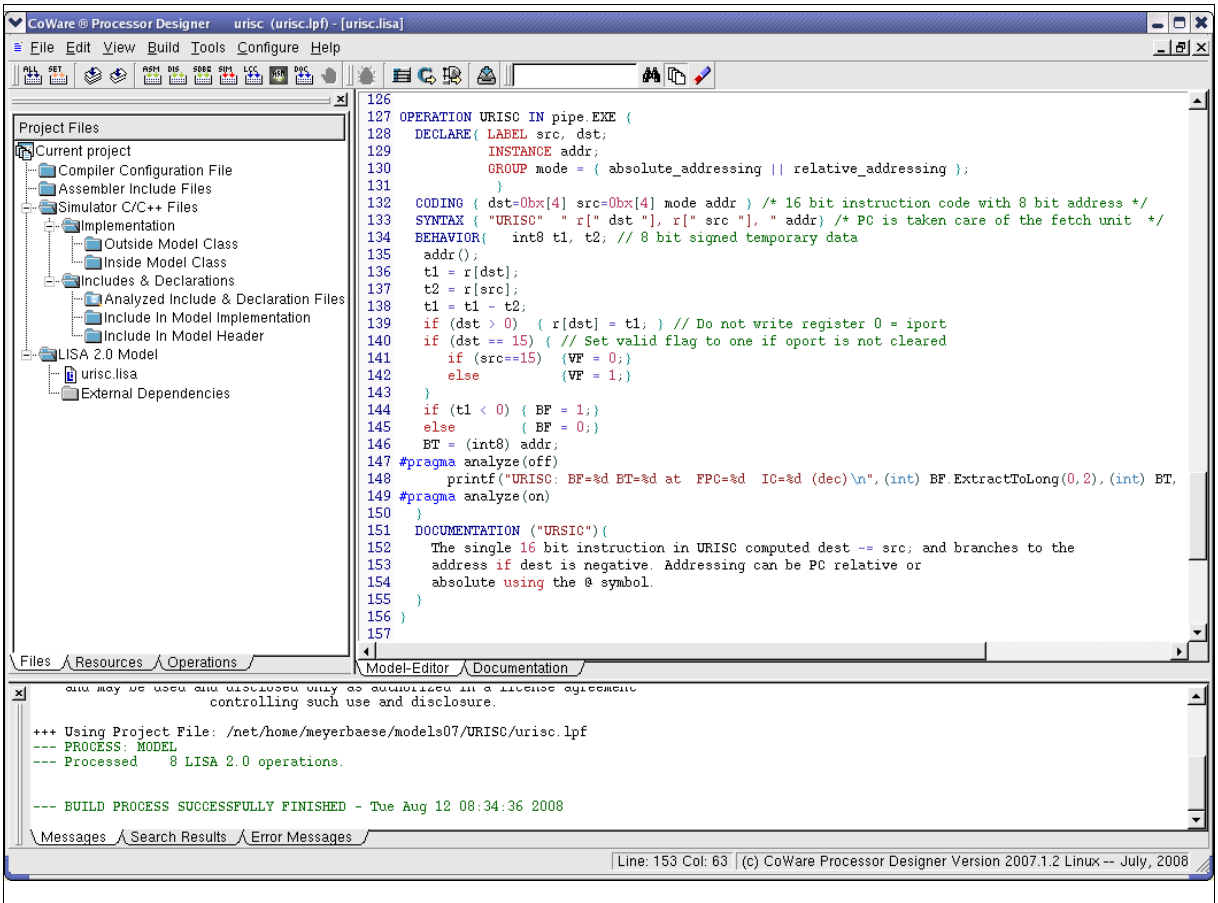
URISC1 Fibonacci simulation with iport =3 and output oport=2: URISCsim1.bmp

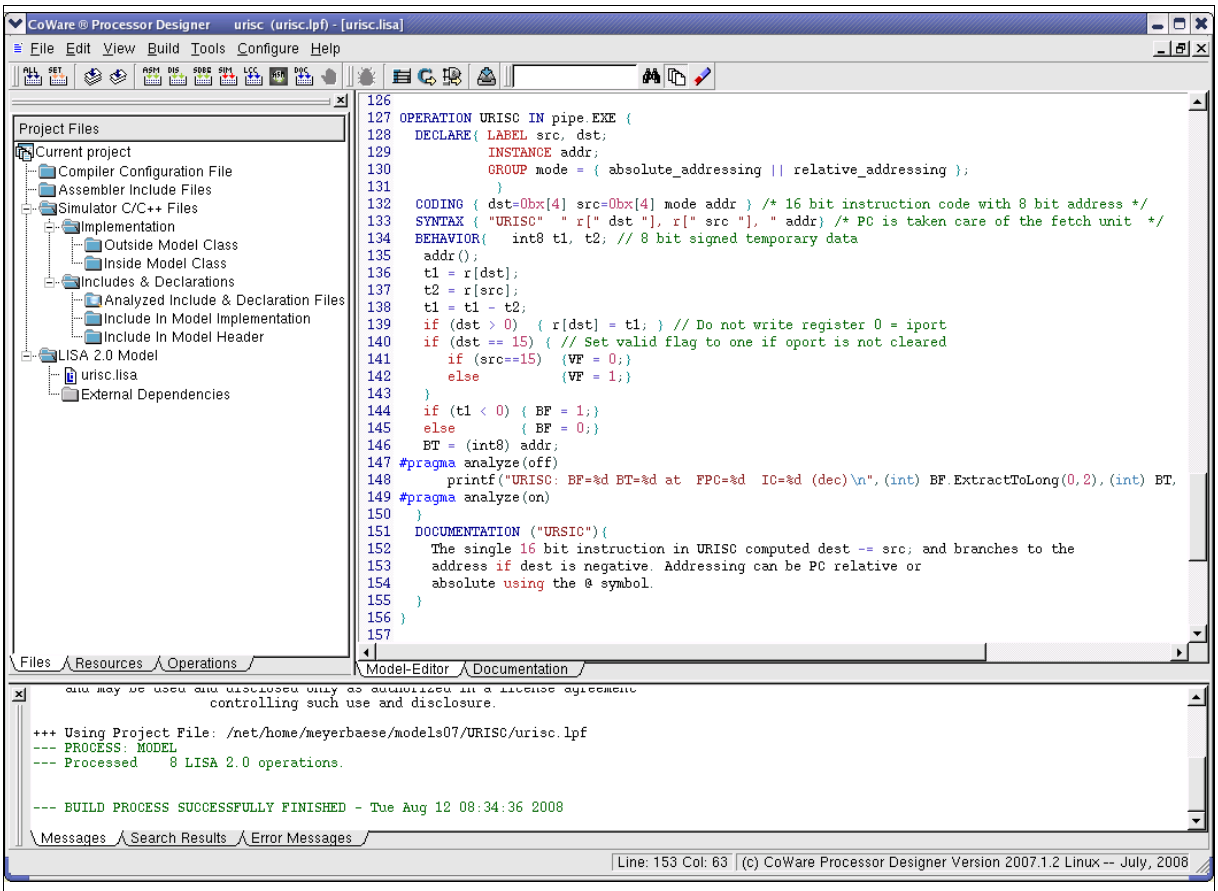
#2



The Processor Designer Window: URISCcode0.bmp

#3

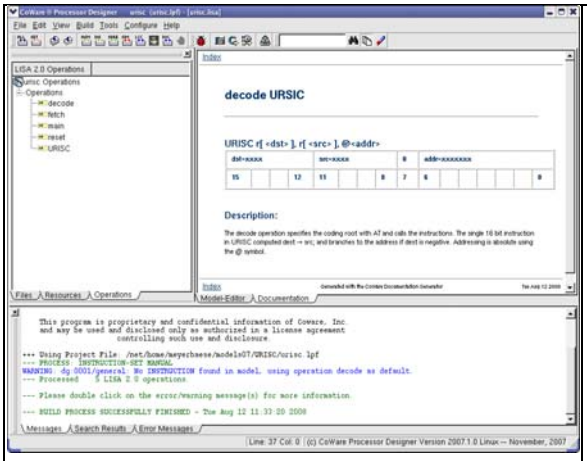




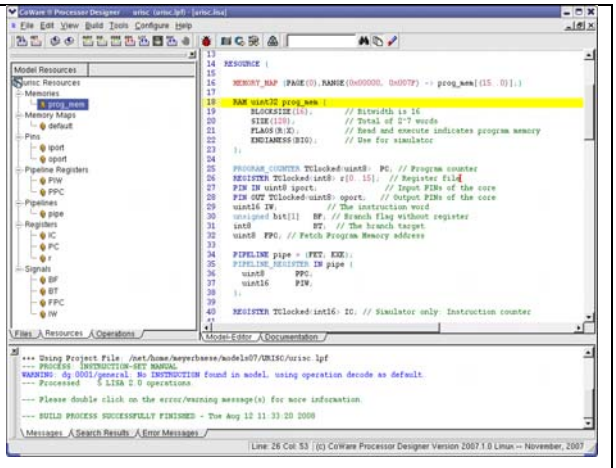

```
126
127 OPERATION URISC IN pipe.EXE {
128   DECLARE{ LABEL src, dst;
129            INSTANCE addr;
130            GROUP mode = { absolute_addressing || relative_addressing };
131            }
132   CODING { dst=0bx[4] src=0bx[4] mode addr } /* 16 bit instruction code with 8 bit address */
133   SYNTAX { "URISC"  " r[" dst "], r[" src "], " addr} /* PC is taken care of the fetch unit  */
134   BEHAVIOR{   int8 t1, t2; // 8 bit signed temporary data
135    addr();
136    t1 = r[dst];
137    t2 = r[src];
138    t1 = t1 - t2;
139    if (dst > 0)  { r[dst] = t1; } // Do not write register 0 = iport
140    if (dst == 15) { // Set valid flag to one if oport is not cleared
141       if (src==15)  {VF = 0;}
142       else          {VF = 1;}
143    }
144    if (t1 < 0) { BF = 1;}
145    else        { BF = 0;}
146    BT = (int8) addr;
147 #pragma analyze(off)
148       printf("URISC: BF=%d BT=%d at  FPC=%d  IC=%d (dec)\n",(int) BF.ExtractToLong(0,2),(int) BT,
149 #pragma analyze(on)
150   }
151   DOCUMENTATION ("URSIC"){
152     The single 16 bit instruction in URISC computed dest -= src; and branches to the
153     address if dest is negative. Addressing can be PC relative or
154     absolute using the @ symbol.
155   }
156 }
157
```

The Processor Designer Window: URISCcode1.bmp

#4

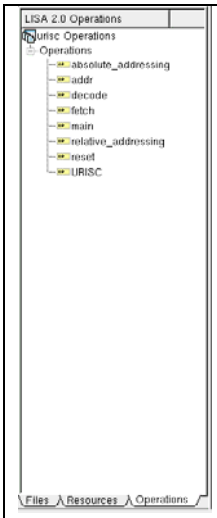
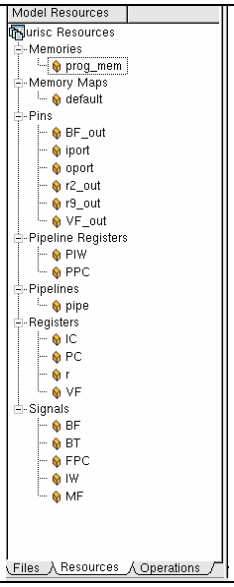
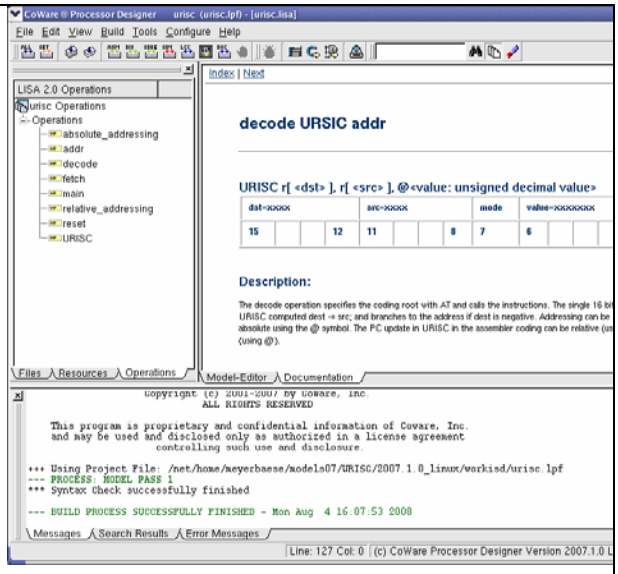


URISCcodeOperations.bmp

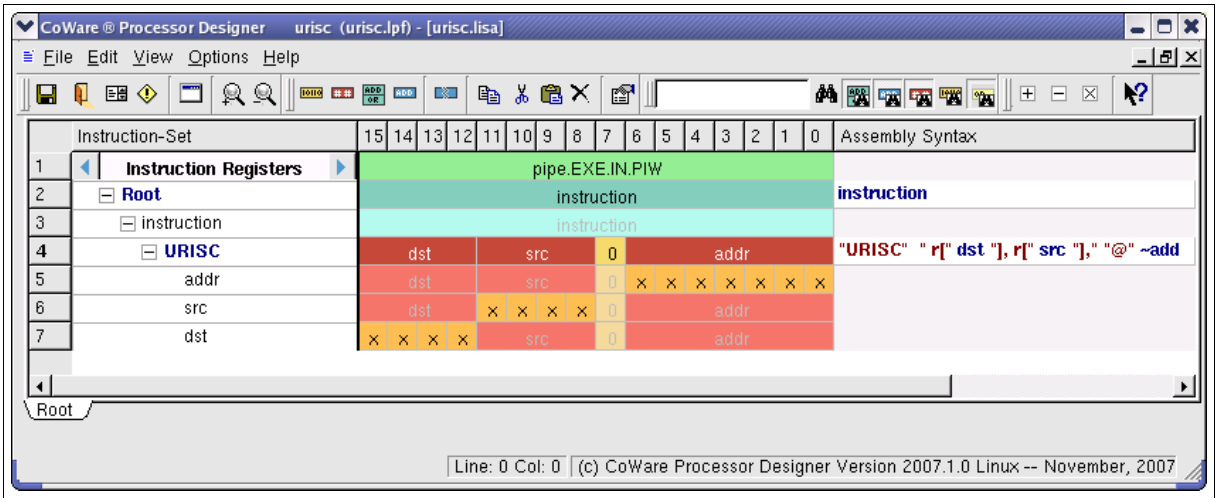


URISCcodeRsource0.bmp

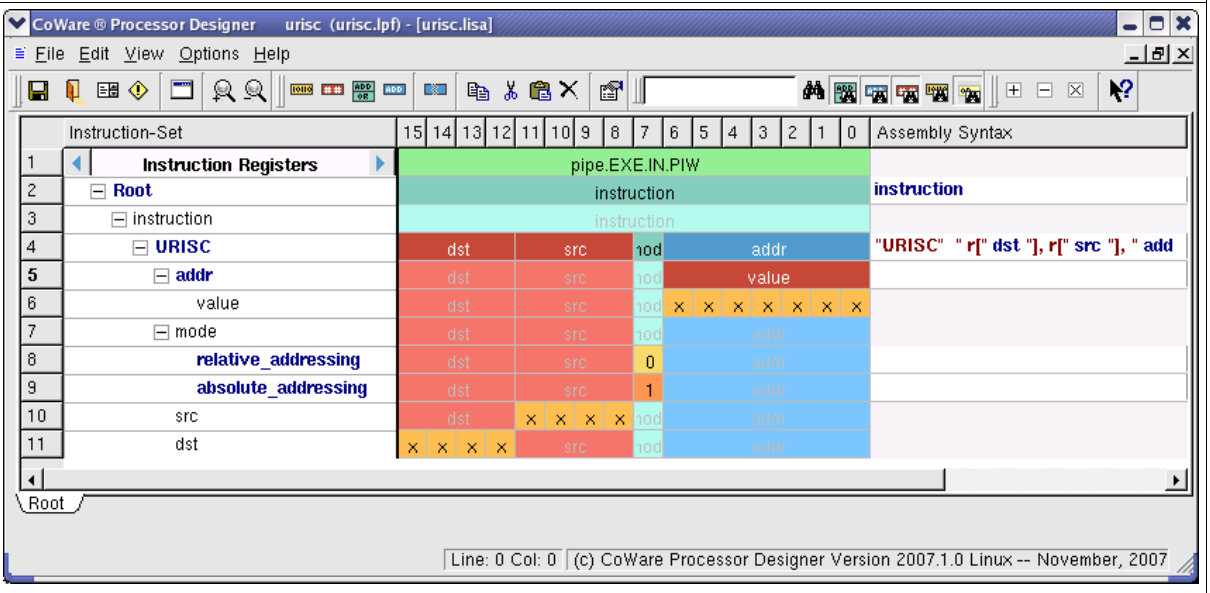
#5

		
URISCcodeOperations.bmp	URISCcodeResources.bmp	URISCcodeDocu.bmp

#6 The Processor Designer Documentaton Window.

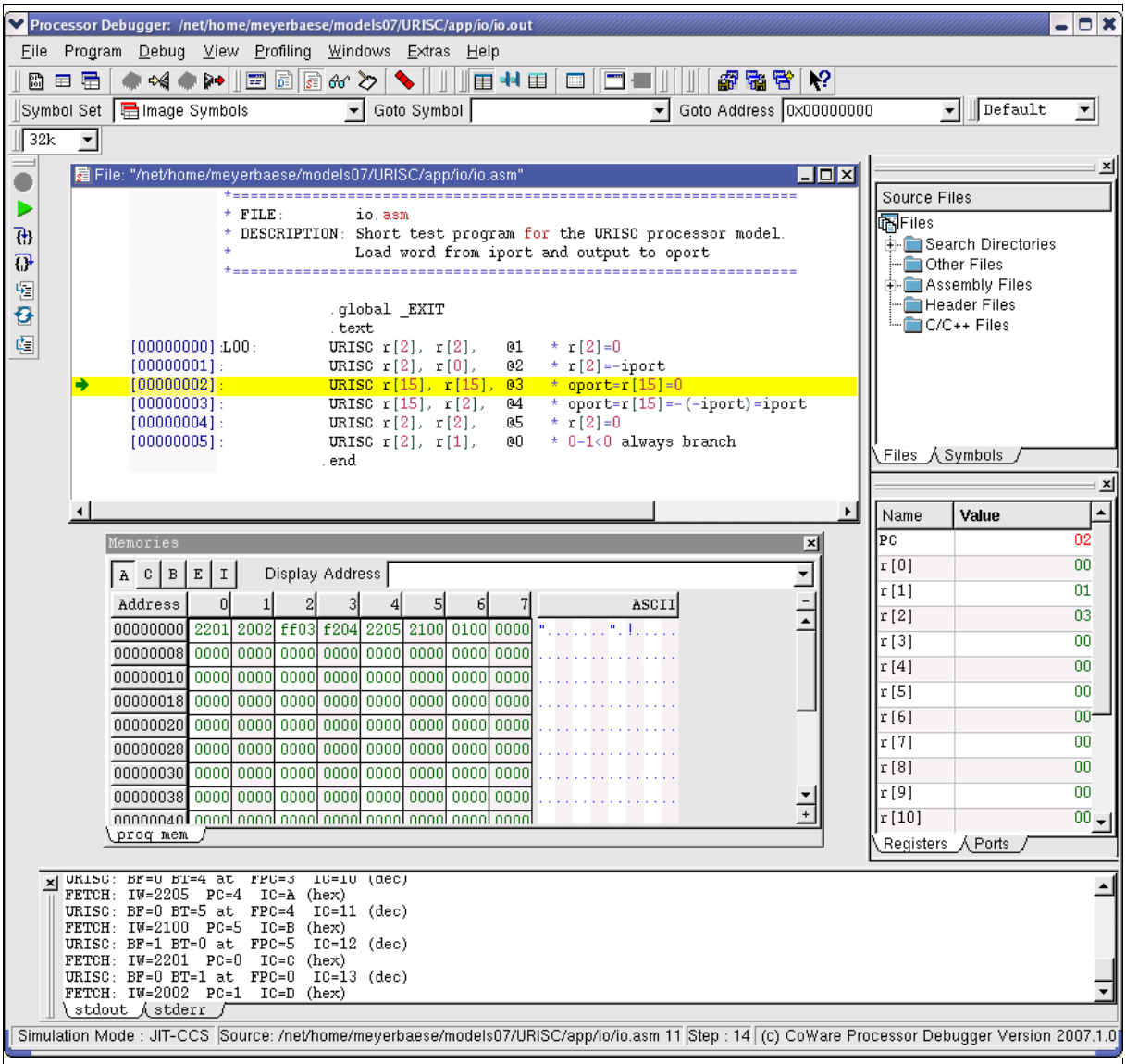


The URISC instruction set view: URISCisa0.bmp



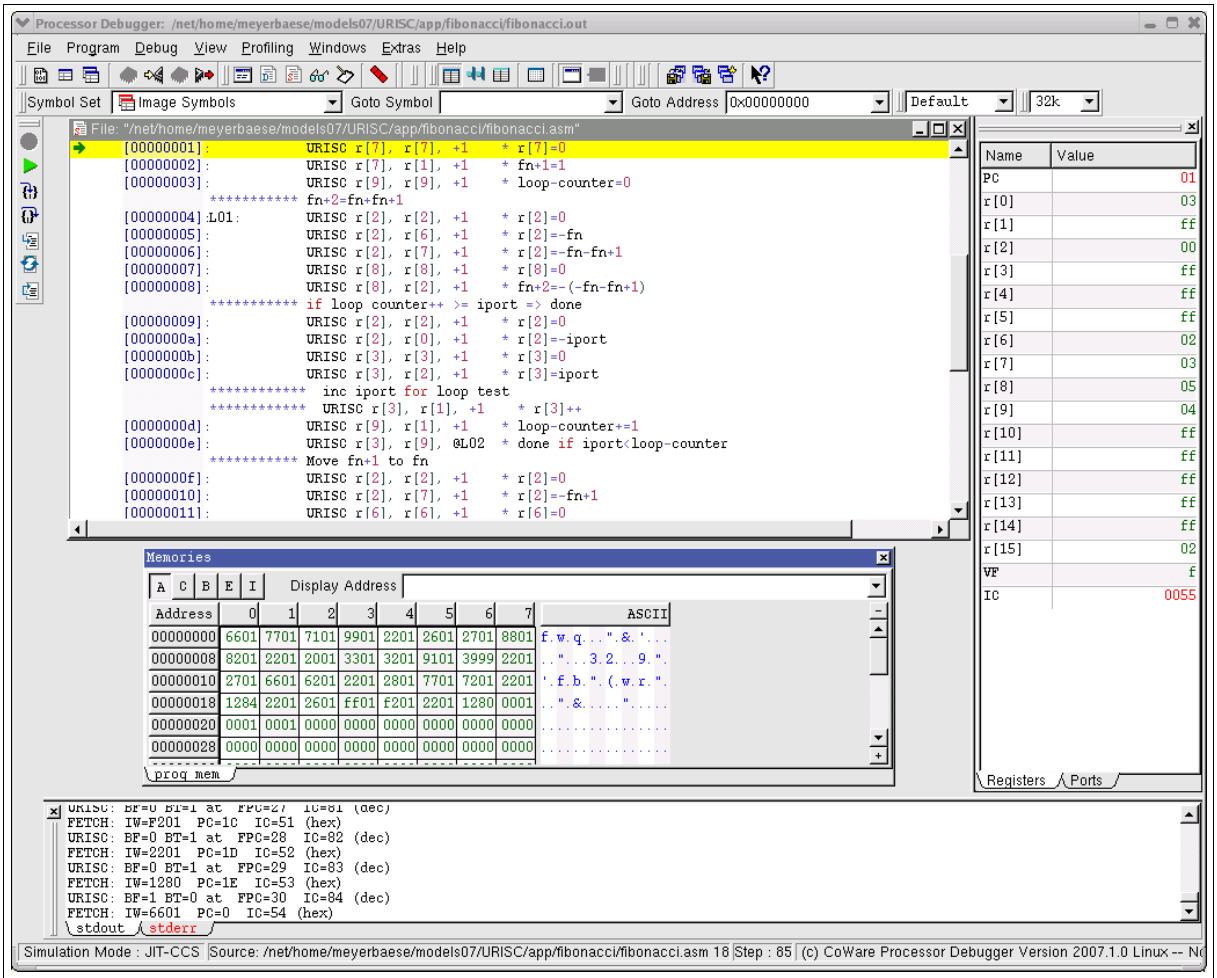
The URISC instruction set view: URISCisa1.bmp

#7



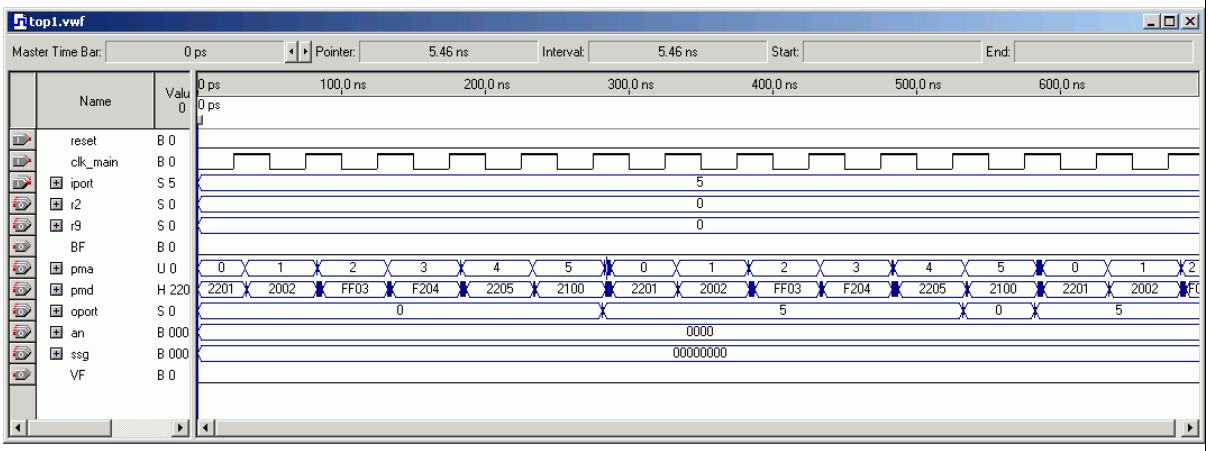
The URISC debugger: URISCdebug0.bmp

#8



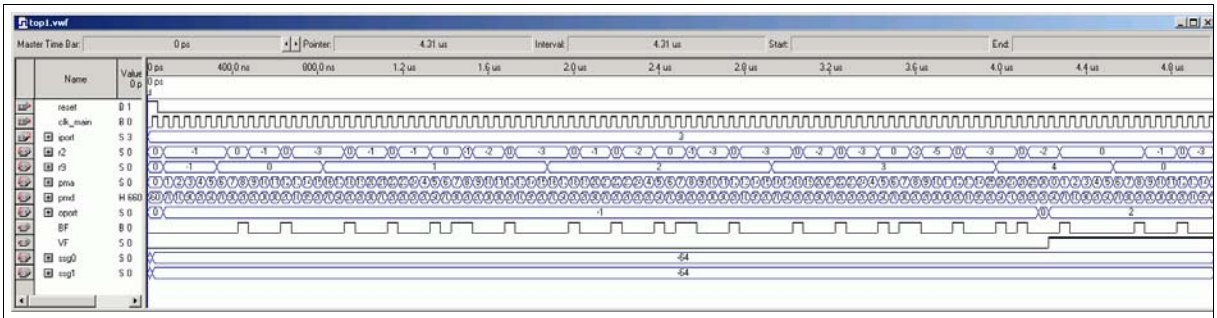
Fibonacci application The URISC debugger: URISCdebug1.bmp

Altera Synthesis Results URSIC



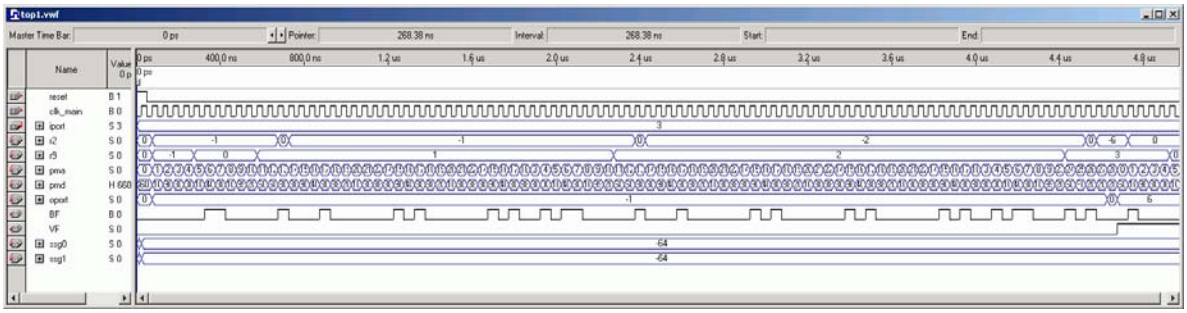
URISC0 simulation with iport load and output to oport=5: aURISCsimio.gif

#10



URISC1 Fibonacci simulation with iport =3 and output oport=2: aURISCsimFibo.gif

#11



URISC1 Factorial simulation with iport =3 and output oport=6: aURISCsimFact.gif

#12