Experimental Comparisons of SiC JFETs and SiC MOSFETs in a PEBB based Converter

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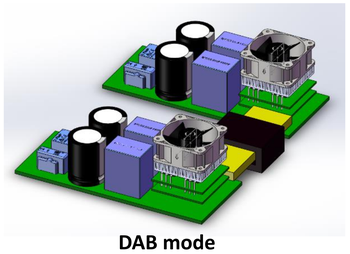
Objectives / Goal

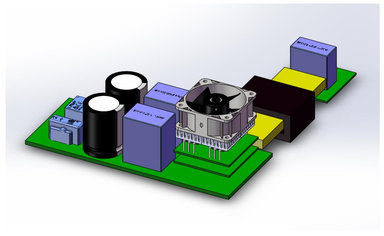
- To compare the performance of latest SiC JFETs and SiC MOSFETs in a power converter operating environment.
- To derive a comparison matrix to evaluate these two devices operated in a converter.
- To design a PEBB based testbed that can be reconfigured to achieve different operation modes of power converters for device evaluations.
- To educate/train a new generation engineers with WBG power electronics designing and testing expertise.

Reconfigurable PEBB based testbed

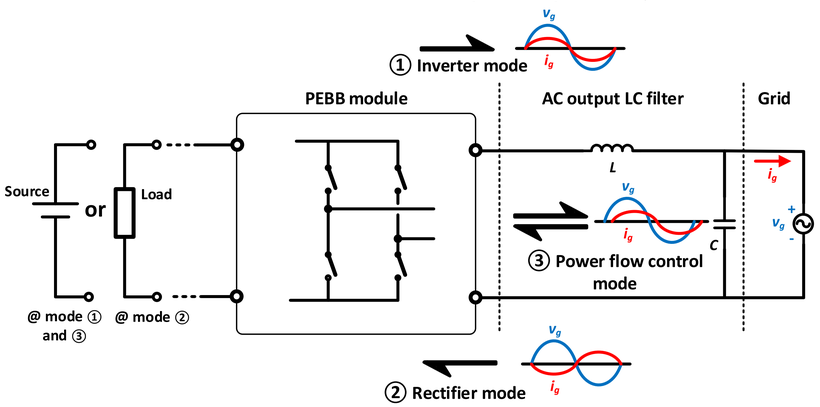
Multiple operation mode of proposed reconfigurable testbed



DAB mode



Inverter /rectifier/reactive power flow mode

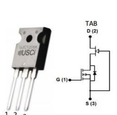


- DAB mode enables soft-switching scenario
- Inverter /rectifier/reactive power flow mode are available for hard-switching scenario

Devices under test

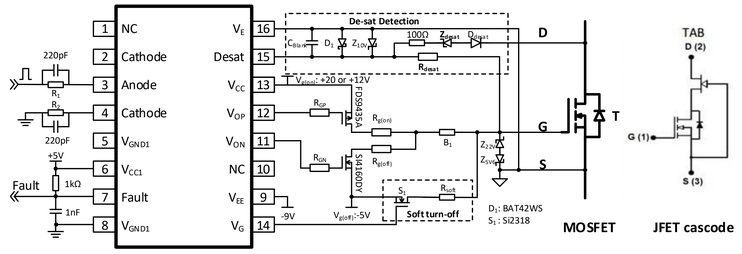
Device	Continuous drain current I_D (T_c)	Maximum operating temperature T_J	Drain-source on-resistance $R_{DS(on)}$ (T_J)	Normalized die area to Wolfspeed MOSFET
Wolfspeed SiC MOSFET (C2M0080120D)	36A (25 °C) 24A (100 °C)	150 °C	80mΩ(25 °C) 128mΩ(150 °C)	1.00
USCi SiC JFET Cascode (UJC1206K)	35A (25 °C) 23A (100 °C)	150 °C	45mΩ(25 °C) 100mΩ(150 °C)	0.90

SiC MOSFET



SiC JFET Cascode

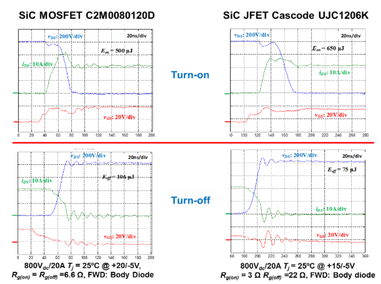
Optimized gate driver design



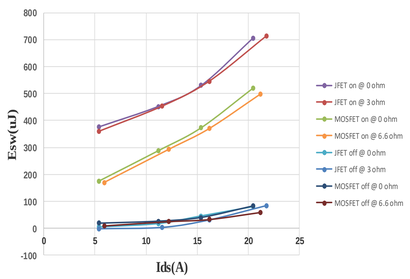
- **Totem-pole gate driver including De-sat short-circuit protection circuit for SiC MOSFET and JFET Cascode**
- **Optimized gate resistance $R_{g(on)}$ and $R_{g(off)}$ are required for the two devices under test, respectively.**
- **Optimized gate driver placement configurations to reduce switching loss are investigated and verified experimentally.**

DPT hardware and experimental results

DPT test board and gate drive circuit for 1200V SiC MOSFETs and JFET Cascode



The experimental waveforms comparison

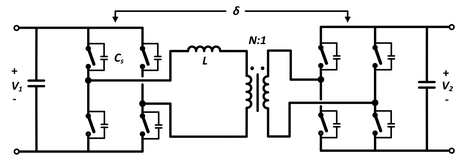


Switching loss comparison

- The turn-on resistor of two devices are similar. The turn-off resistor of JFET cascode is 22 ohm, however, SiC MOSFETs turn-off resistor is only 6 ohm, therefore JFETs cascode device has longer turn-off time.
- The highest dv/dt that JFET cascode can reach is ~40 v/ns, SiC MOSFETs can reach 80v/ns. Under this condition, the switching loss of SiC MOSFETs is about 40% of that of SiC JFET Cascode.

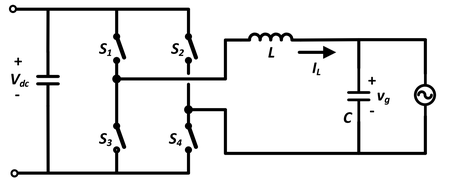
Parametric design for reconfigurable testbed

Symbol	Description	Value
P_n	Nominal power rating	5 kW
V_1 / V_2	Primary / secondary side dc voltage	750 V
$N:1$	Transformer turns ratio	1 : 1
δ	Phase-shift angle	10 °
f_s	Switching frequency	100 kHz
L	Primary referred leakage inductance	28 μH
C_s	Snubber capacitance	200 pF
T_D	Dead time	0.16 μs
$P_{cond.}$	Conduction loss of a full bridge	16.8 W
$P_{sw.}$	Switching loss of a full bridge	12.8 W



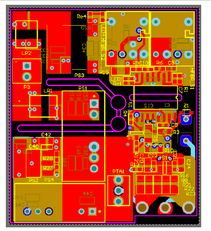
DAB converter

Symbol	Description	Value
P_o	Nominal power rating	5 kW
V_{dc}	Dc voltage	750 V
v_g	Grid voltage	480V_{rms} /60 Hz
f_s	Switching frequency	100 kHz
m_a	Modulation Index	0.905
L	Output filter inductance	76 μH
Δi_L	Peak-to-peak output current ripple	30 %I_L
C	Output filter capacitance	1.26 μF
f_{LC}	Resonant frequency of the LC filter	20 kHz
$P_{cond.}$	Conduction loss	21.2 W
$P_{sw.}$	Switching loss	31.9 W

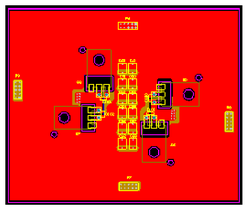


Single-phase inverter

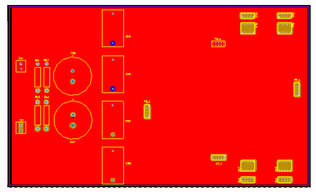
PCB layout design of PEBB module



Gate driver V2



Daughter power board



Mother power board

Main Achievements and conclusions

- A novel reconfigurable PEBB based SiC devices testbed is proposed and the hardware design is finished.
- Preliminary comparison between SiC MOSFETs and JFET Cascodes are conducted on specifically designed DPT setup.
- An optimized gate driver design including short-circuit protection is investigated and verified experimentally.

Next step

- To build and Building and debugging of PEBB based test setup.
- To compare the device performance such as efficiency and thermal performance in a power converter operating environment.
- Various operation modes including hard- and soft-switching scenario.